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A 2.56 Gbps or 10 Gbps 1:16 Deserializer for High-Energy Physics Experiments

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Abstract—Deserializer is used to convert the high-speed serial data into a low-speed parallel data in the downlink direction of data transmission system in high-energy physics experiments. The 2.5Gbps rate can fully meet the downlink data transmission requirements of the current experimental equipment. But as the experimental equipment is upgraded, the amount of data will be greatly increased. In order to meet the demand of current data volume and adapt to upgrade of the equipment in the future, this paper presents the design and simulation results of a 1:16 deserializer ASIC which can be compatible with data rate of 2.56 Gbps and 10 Gbps.

The 2.56 Gbps or 10 Gbps 1:16 deserializer ASIC mainly consists of an equalizer, 1:4 DEMUX module, 4:16 DEMUX module, clock divider by 4, LVDS drivers and an automatic frequency comparator. The 1:4 DEMUX module and 4:16 DEMUX module are implemented by one and four 1:4 DEMUX units, respectively. According to different data rates, there are two different 1:4 DEMUX units (High-speed 1:4 DEMUX unit and Low-speed 1:4 DEMUX unit) with the same overall structure have been designed. The two 1:4 DEMUX units are composed of 7 DFFs, which are sampled by four quadrature phase clocks (CLK0, CLK90, CLK180, CLK270) generated by a clock divider by 4. According to different clock frequency, there also two clock divider by 4 (High-frequency clock divider by 4 and Low-frequency clock divider by 4) have been designed. In order to improve the bandwidth, the high-speed 1:4 DEMUX unit and the high-frequency clock divider by 4 adopt the latches with an optimized compressed CML structure. And the low-speed 1:4 DEMUX unit and the low-frequency clock divider by 4 adopt CMOS latches to save power consumption.

At 10 Gbps data rate, the input data will be compensated first by equalizer for high frequency signal attenuation caused by PCB transmission line and parasitic parameter from bonding wires and input pads. The equalized data will be divided into 4 parallel 2.5 Gbps/Ch data by the first 1:4 DEMUX module with CML structure. The second 4:16 DEMUX module following the first 1:4 DEMUX module divides 4 parallel 2.5 Gbps/Ch data into 16 parallel 625 Mbps/Ch data. The sampling clocks of the first 1:4 DEMUX module and the second 4:16 DEMUX module are provided by a first high-frequency clock divider by 4 and a second low-frequency clock divider by 4, respectively.

At 2.56 Gbps data rate, the input differential data is converted into single firstly, and then send into a third 1:4 DEMUX module with CMOS structure to obtain 4 parallel 640 Mbps/Ch data. The second 4:16 DEMUX module following the third 1:4 DEMUX module divides 4 parallel 640 Mbps/Ch data into 16 parallel 160 Mbps/Ch data. The sampling clocks of the third 1:4 DEMUX module and the second 4:16 DEMUX module are provided by third low-frequency clock divider by 4 and second low-frequency clock divider by 4, respectively.

The second 4:16 DEMUX module at the data rate of 10 Gbps and 2.56 Gbps share the same module, and the second low-frequency clock divider by 4 at the clock frequency of 10 GHz and 2.56 GHz share the same module, too.

In order to cope with the incorrect sampling position caused by phase offset at different process corners, the clock divider by 4 adopts the structure of four cascaded latches to obtain 8 phase clock signals. And a phase selector following the clock divider by 4 selects the clock signal with appropriate phase according to the offset under the different process corners. And a duty cycle correction and clock aligner is added to the low-frequency clock divider by 4 to improve the quality of the sampling clocks. An automatic frequency comparator is designed into the ASIC to switch the operating rate automatically according to the input clock frequency.

The 2.56 Gbps or 10 Gbps 1:16 deserializer ASIC has been designed in 55 nm CMOS process with core area

of 1120 μm × 600 μm. The simulation results show that the logic of output data at 2.56 Gbps and 10 Gbps are correct in different process corners. And the clean and open output eye diagrams can be obtained at the input data rate of 2.56 Gbps and 10 Gbps, respectively. The power consumption is 217 mW with 1.2 V power supply. The chip has been taped out and the tests are planned to be conducted in this June.

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