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Automated, adaptive, fast reset circuit for wide-energy range detector front-end

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In this paper, we present a precise and fast reset circuit that restores the charge sensitive amplifier (CSA) output baseline voltage from a pulse level. The circuit is self-clocking, and its operation speed can be adjusted with the delay line configuration. This method is especially promising for wide-energy range CMOS detectors, as it adapts the discharge speed to the pulse amplitude. Additionally, the proposed method strongly mitigates the parasitics influence on its operation.

Working with high-intensity wide-energy radiation, fast discharging of the feedback capacitor after pulse processing is especially important whenever high count-rate performance is expected. A common solution is to use Krummenacher feedback with a high polarisation current [1]. However, since this approach discharges the capacitor right after the event, precise ADC-based energy measurement is extremely difficult or even impossible.

The possible solution is to apply Krummenacher feedback with a larger time constant, but equipped with additional circuitry responsible for baseline restoration whenever the amplitude measurement is done. The simplest approach consists in shorting both capacitor plates using a switch [2]. Such a solution may result in either high overshoot or temporary oscillations, disenabling pulses amplitude measurement or even their detection.

An interesting method is the so-called click-clack circuit, which works with two parallel capacitors and is based on switching the plates' connections to antiparallel to perform discharging [3]. Importantly, in this method, all capacitances must be precisely matched, and sharp discharging with no overshoot can be obtained only for a narrow range of pulse amplitudes.

We propose a self-clocking and automated reset circuit based on additional and simple circuitry to perform feedback for restoring the CSA baseline (Fig. 1.). This is realized by current sources that inject current pulses into the CSA input node, compensating the capacitor charge. Each step is followed by a comparison of the CSA output voltage and the reference voltage level, and a decision is made if further discharge is needed. The discharge process is divided into two phases –coarse and fine. During the latter, only I1 feeds current to the capacitor, making it quite slow, but reducing the overshoot. The coarse phase checks the MSB of the ADC conversion result. If it is set, all sources I1-I3 work, if not, only I1-I2. The transition from coarse to fine phase is controlled by the inverter-based comparator that monitors the CSA output.

The proposed solution allows for working with both high count-rate and wide-energy pulses, keeping the Krummenacher feedback equivalent resistance very high, thus enabling fast and precise photon energy measurement. Due to the adaptation of the discharge speed to the pulse amplitude, a fast reset without significant overshoot can be achieved for a wide energy range (Fig. 2.). The solution is implemented in 28 nm CMOS technology and will be manufactured soon.

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