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Small pixel ultra-fast photon-counting prototype IC for synchrotron applications

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Single-photon counting Hybrid Pixel Detectors (HPD) become increasingly popular in various 2-D X-ray imaging techniques and scientific experiments, mainly in solid-state physics, material science and medicine. Current research and development of HPDs are following several different directions [1] and one of them is the possibility of operation with high intensity of X-ray beam [2]. This paper presents the design and preliminary measurements results of a prototype SPHIRD chip designed in the CMOS 40 nm process. The chip is dedicated for ultra-high count rate and high spatial resolution operation at ESRF-EBS synchrotron. The core of the prototype IC is the matrix of 64x32 pixels of 50 µm pitch. Each pixel contains a Charge Sensitive Amplifier (CSA) with a fast discharge block and detector leakage current compensation circuit. The CSA is connected to set of discriminators with offset trimming possibility. The priority of the design is ultra-fast signal processing in the analog front-end electronics up to 30 Mcps/pixel. Therefore, the pulse time width at the CSA output is only 22 ns, keeping at the same time the equivalent noise charge at the level of 120 el. rms with a power consumption equal to 32 µW/pixel. Additionally, the set of discriminators equipped with extra blocks allows compensation for the effect of pulse pile-up in the voltage or time domain. The chip is optimized for the operation with a monochromatic X-ray beam with an energy up to 30 keV. Furthermore, because of the charge sharing effects, several algorithms of interpixel communication are implemented in the chip to increase detector resolution below pixel pitch.

[1] R. Ballabriga, et al.,"Photon counting detectors for X-ray imaging with emphasis on CT,"IEEE Trans. Radiation and Plasma Medical Science, vol. 5, no. 4, p. 422–440, 2021.

[2] R. Kleczek, et. al. "Single photon counting pixel readout chip operating up to 1.2 Gcps/mm2 for digital X-ray imaging systems" IEEE J. Solid-State Circuits, vol.53, no. 9, pp. 2651–2662, 2018.

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