Edge-TCT evaluation of High Voltage-CMOS test structures with unprecedented breakdown voltage for high radiation tolerance

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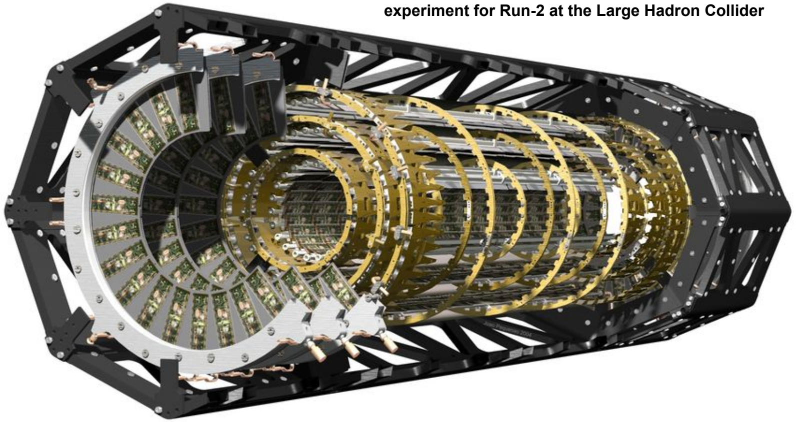
Trackers

- Collision event generates charged particles
- Charged particles curve in magnetic field
- Tracker follows the path
- Curvature determines charge, mass of particle



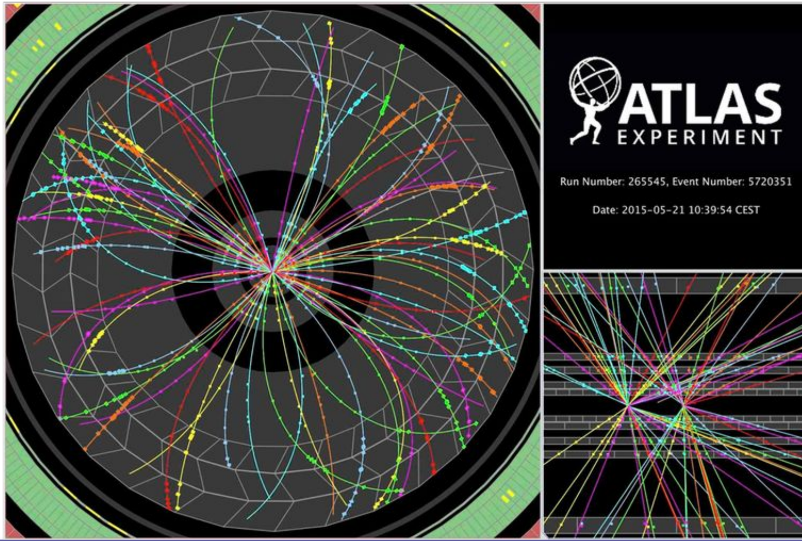
The ATLAS Inner Tracker
G. Mullier: **The upgraded Pixel Detector of the ATLAS experiment for Run-2 at the Large Hadron Collider**

Placed close to collision center → Sensors receive high radiation dose

High rate of events
MHz-GHz rate of bunch crossings → Fine spatial resolution required
Good time resolution

Minimal track disruption → Thin sensors

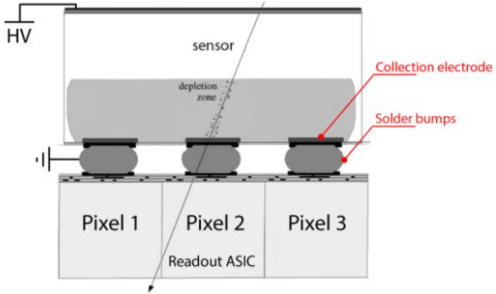
Higher collision energies → More radiation, finer detail needed



Sensors need to be thin, fast, radiation tolerant, and within budget

DISCLAIMER: I do not work for ATLAS, this is just an example

Pixel Sensors

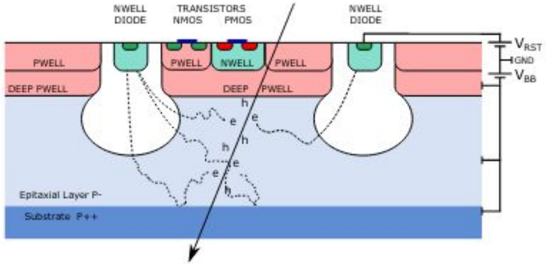


Hybrids

Cross-section of a hybrid pixel design proposed for CLiC

External Readout Circuitry:
- ✔ Fast readout
- ❌ Specialised bump-bonding
- ❌ Increases thickness
- ❌ Limits granularity

High Voltage Pixel:
- ✔ More radiation tolerant
- ✔ Fast charge collection (Drift)

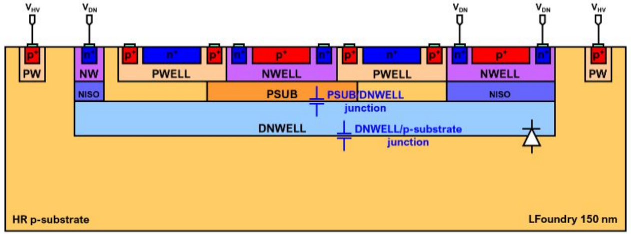


CMOS

Cross-section of standard CMOS pixel ALPIDE used in ALICE

Integrated Readout Circuitry:
- ✔ Thin sensors
- ✔ Industrial standard
- ✔ Cost effective

Low Voltage Pixel:
- ❌ Less radiation tolerant
- ❌ Slow charge collection (Diffusion)



HV-CMOS

Cross-section of a typical HV-CMOS pixel

Integrated Readout Circuitry:
- ✔ Thin sensors
- ✔ Industrial standard
- ✔ Cost effective

High Voltage Pixel:
- ✔ More radiation tolerant
- ✔ Fast charge collection (Drift)

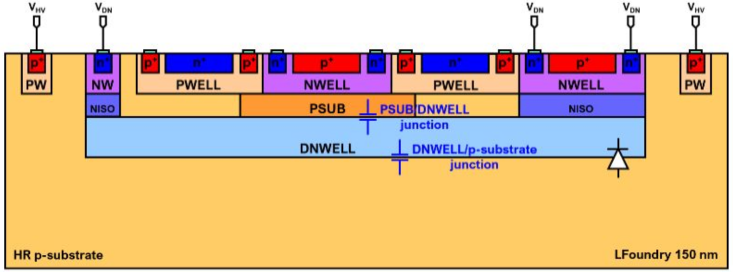
Future Requirements

Industrial Standard Manufacturing Process → No specialised (expensive) processes

High Voltage → Radiation tolerant, Fast time resolution

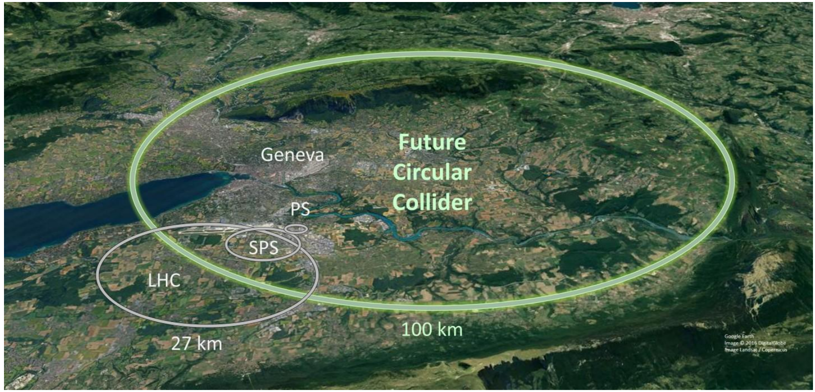
Monolithic → Thin

Cross-section of a typical HV-CMOS pixel



	Pixel Size (μm^2)	System Time Resolution (ns)	Radiation Tolerance (NIEL) (1 MeV $n_{eq} cm^{-2}$ Year $^{-1}$)
HL-LHC	50 x 50	0.03	10^{16}
FCC-hh	25 x 50	0.1	10^{16} to 10^{17}
Current HV-CMOS	50 x 50	3.16	10^{15}

Future tracking detector specifications, and current HV-CMOS capabilities

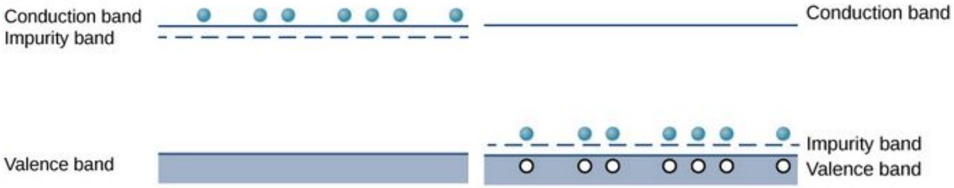


https://cds.cern.ch/record/2653532/files/FCC%20v2.jpg?subformat=icon-1440

Bulk Damage:

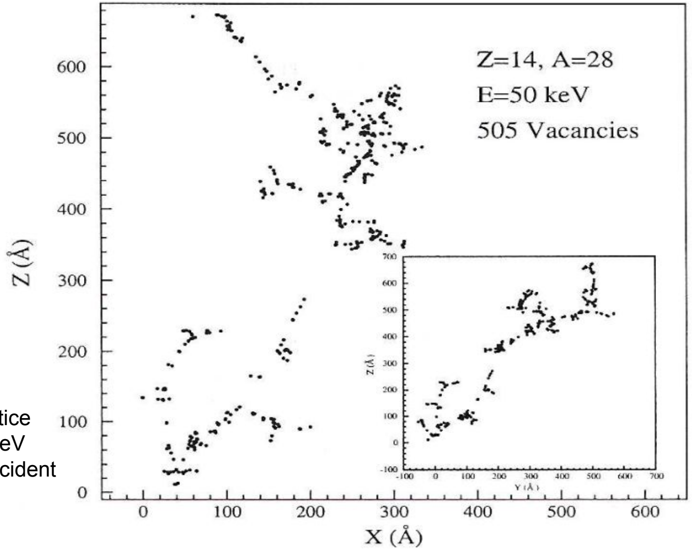
Non Ionising Energy Loss (NIEL)

- Incident radiation knocks an atom out of the lattice, Primary Knock-on Atom (PKA)
- Atom travels knocking more atoms out of the lattice, interstitial-vacancy pairs (Frenkel Pairs)
- Damage introduces acceptor removal, energy levels in the band structure, and charge traps
- **Changes doping profile and resistivity**



Band structure of n and p-type semiconductors (left to right)

S. J. Ling, J. Sanny, and B. Moebs, University Physics Volume 3, 1st ed. Houston, TX: Rice University 2016



Vacancies in a silicon lattice caused by a PKA of 50 keV generated by a 1 MeV incident neutron

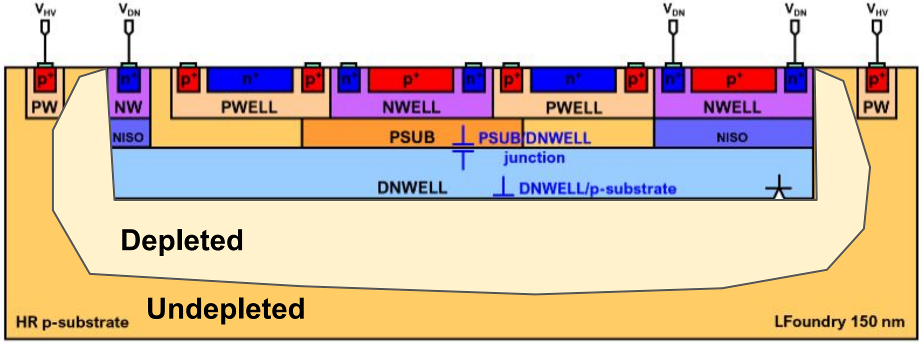
F. H¨onniger, “Radiation damage in silicon. defect analysis and detector properties”, 2008.

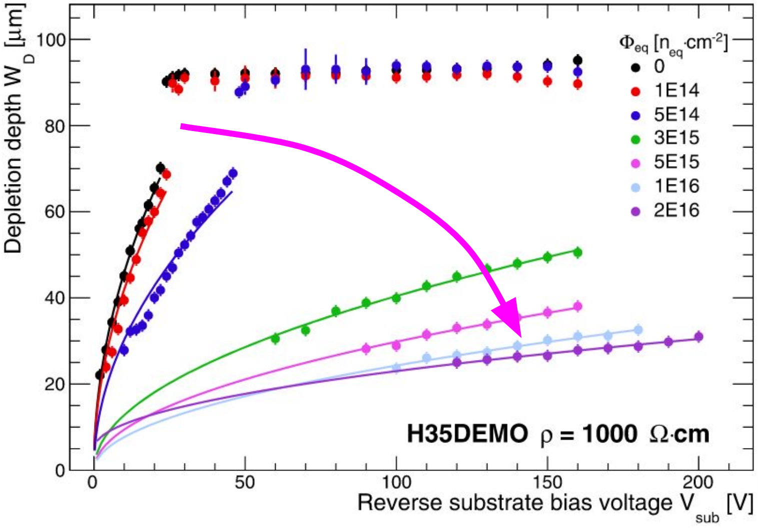
Sensing Region

- Sensing diode increases depletion region with negative biases until diode breaks down
- NIEL reduces depletion region ability to grow
- Counteracted by increasing bias voltage
  - more room for growth
  - Increases charge collection speed
  - Charge traps less effective

$$W = W_0 + \sqrt{\frac{2\epsilon_r\epsilon_0}{qN_A}V_{bias}}$$

W = Depletion depth of semiconductor
W_0 = Depletion depth at 0 V
ϵ_r = Relative permittivity of silicon
ϵ_0 = Permittivity of free space
q = Charge of an electron
N_A = Doping concentration of acceptor atoms
V_{bias} = Reverse bias voltage

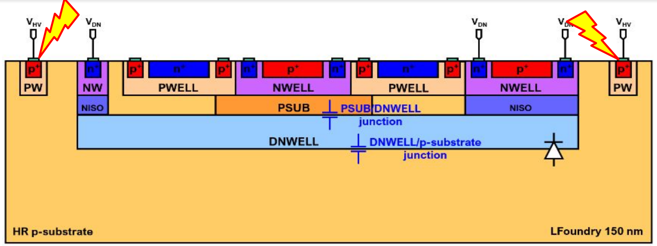




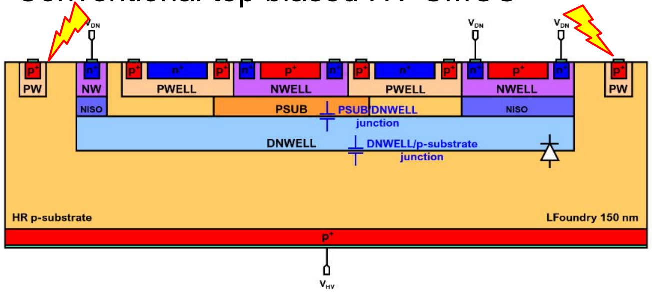
Biasing Scheme

- Increase breakdown voltage
- Top side p-well identifies as low resistivity current path, reduces breakdown

- Simulation show no topside p-wells and backside biasing improves breakdown ~ 1000 V

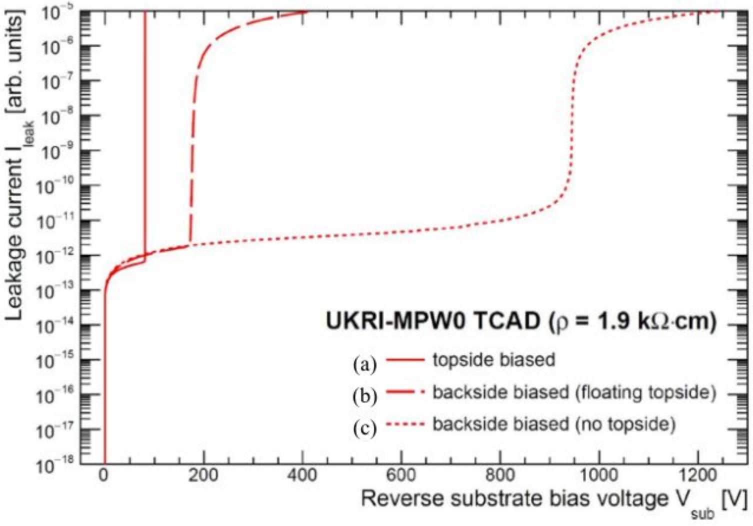


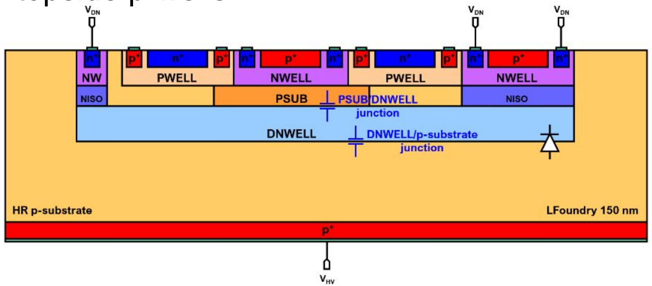
Conventional top biased HV-CMOS



Backside biased HV-CMOS with floating topside p-wells

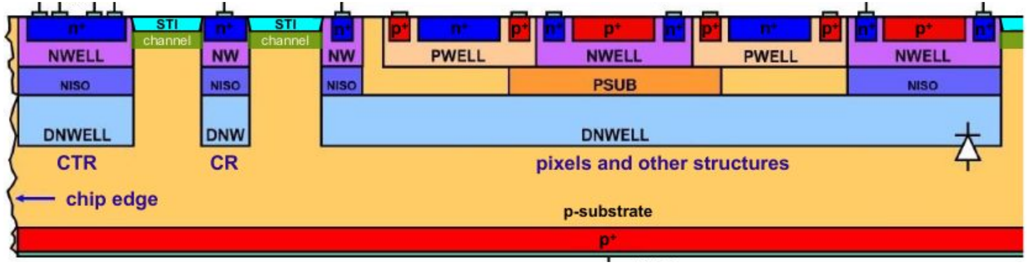
UKRI-MPW0





Backside biased only HV-CMOS
No topside biasing p-wells

UKRI-MPW0

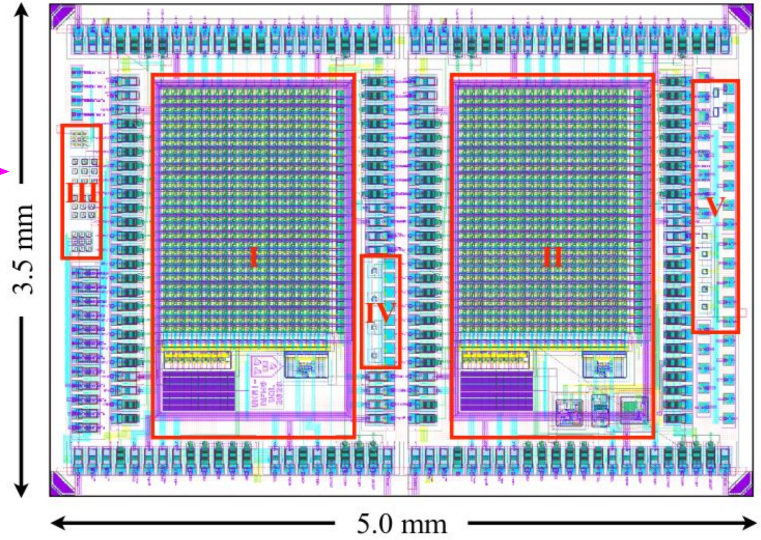


Cross-section of UKRI-MPW0 pixel

- LFoundry 150 nm, HV-CMOS
- 1.9 kΩ cm Substrate Resistivity
- Thinned to 280 μm thickness before backside processing
- Fully backside biased only

- 2 Backside Processing Methods (IBS)
- Current Terminating Ring (dn-well)
- 2 Matrices of 20 x 29 Pixels
- 60 x 60 μm^2 Pixel Size
- 3 Sets of Test Matrices (3 x 3 Passive pixels for eTCT)

eTCT Test Structures



Layout of the UKRI-MPW0 Pixel chip

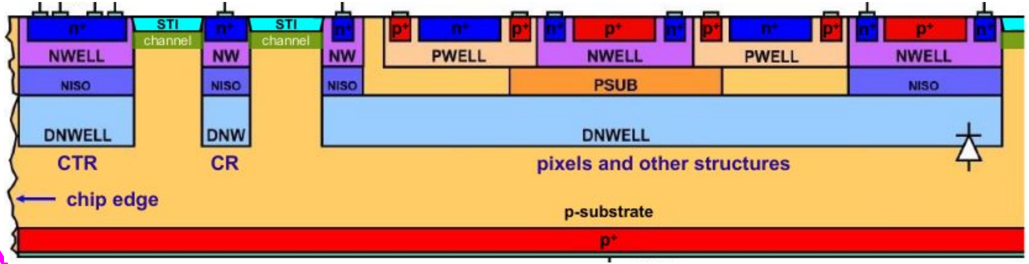
Backside Processing Method

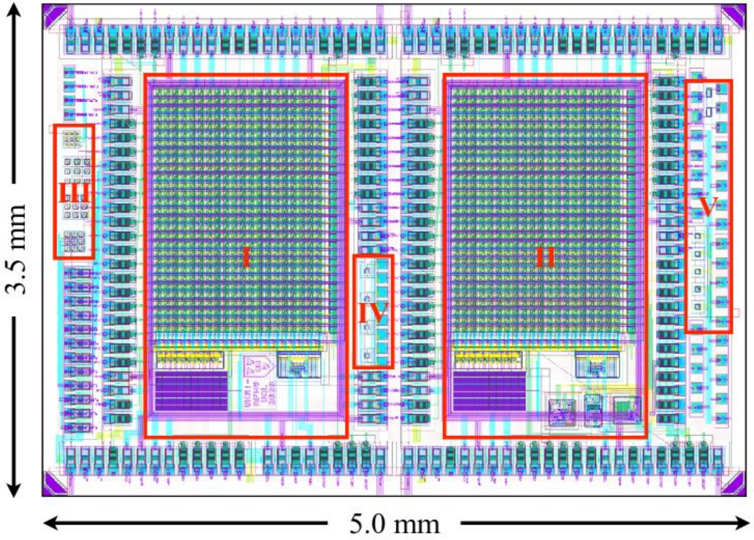
- Backside processing provided by Ion Beam Service (IBS)
- 2 Processing methods offered

- Beamline Ion Implantation + Rapid Thermal Annealing
    - Experience with processing method
    - Potential damage to readout electronics
    - Doesn’t fully anneal boron implantation damage

- Plasma-Immersion Ion Implantation + UV Laser Annealing
    - More defined doping profile
    - Targeted annealing has minimal damage to rest of the chip

Cross-section of UKRI-MPW0 pixel

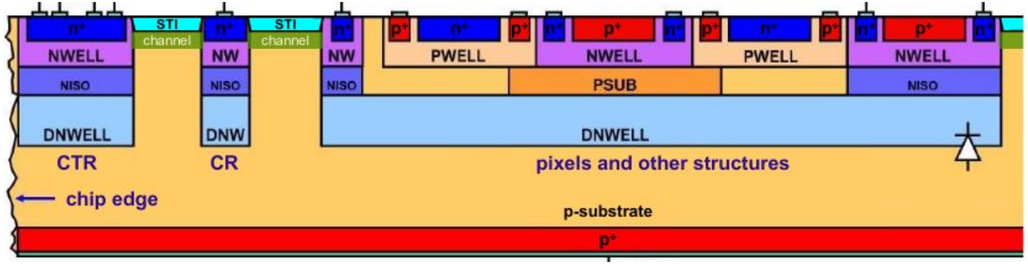




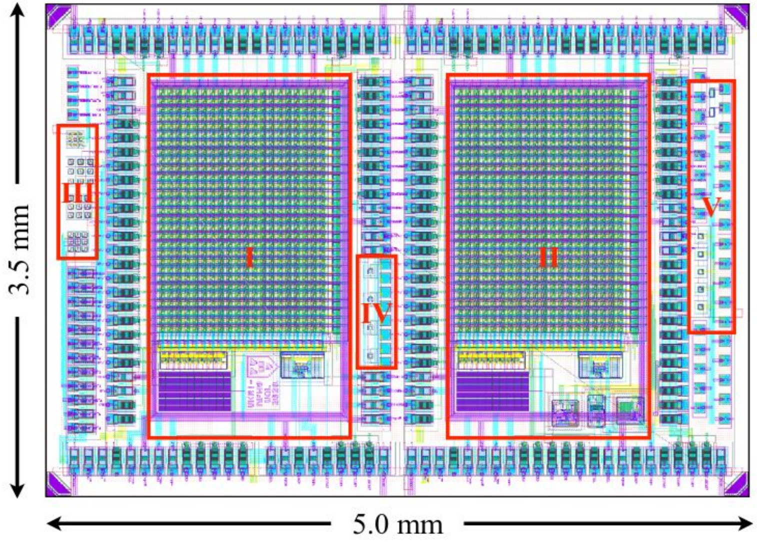
Layout of the UKRI-MPW0 Pixel chip

Current Terminating Ring (CTR)

Cross-section of
UKRI-MPW0 pixel



- Deep n-well ring structure, unconventional (No topside p-well)
- Increase fill factor (avoid multiple rings)
- Shorted to guard-ring
- High leakage current from edge of chip (~ 4 mA)
- Breakdown voltage limited by current through CTR metal
- Low pixel leakage current

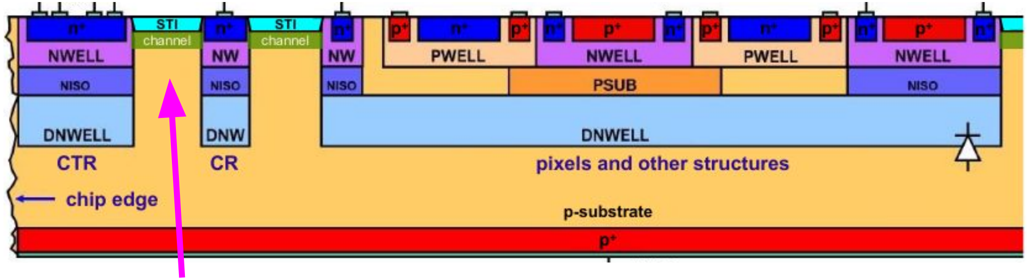


Layout of the
UKRI-MPW0
Pixel chip

“Breakdown”

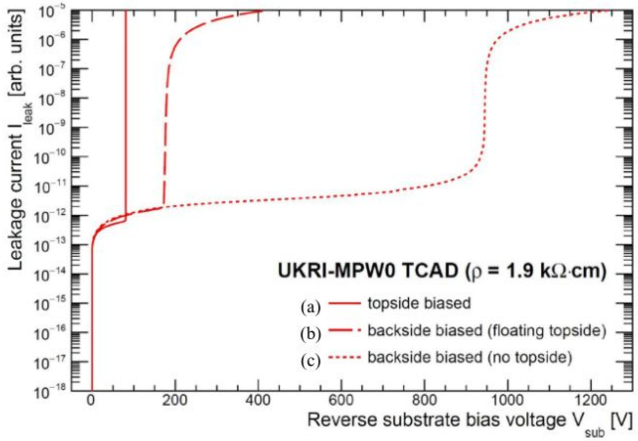
	Substrate Resistivity (Ω cm)	Breakdown Voltage (V)
UKRI-MPW0	**1900**	**~ 600**
LF-monoPix2	2000	~ 460
Astropix	100	~ 250

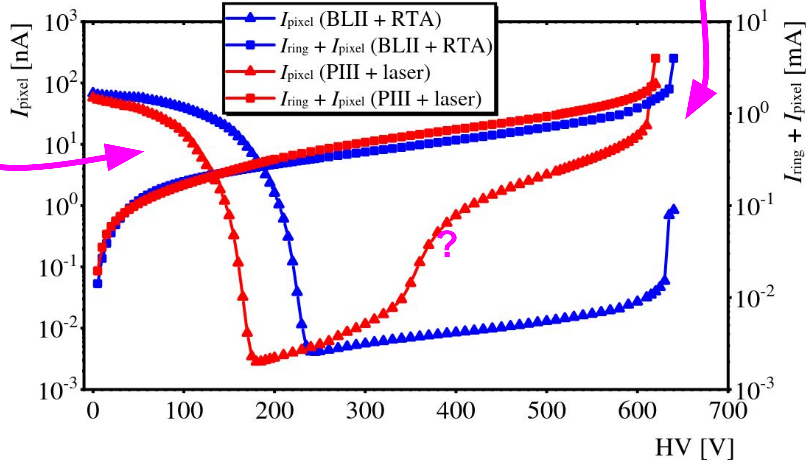
Cross-section of UKRI-MPW0 pixel



Parasitic channel between oxide and p-substrate
Closes at higher voltages

Breakdown not in pixel but thermal runaway in the CTR structure

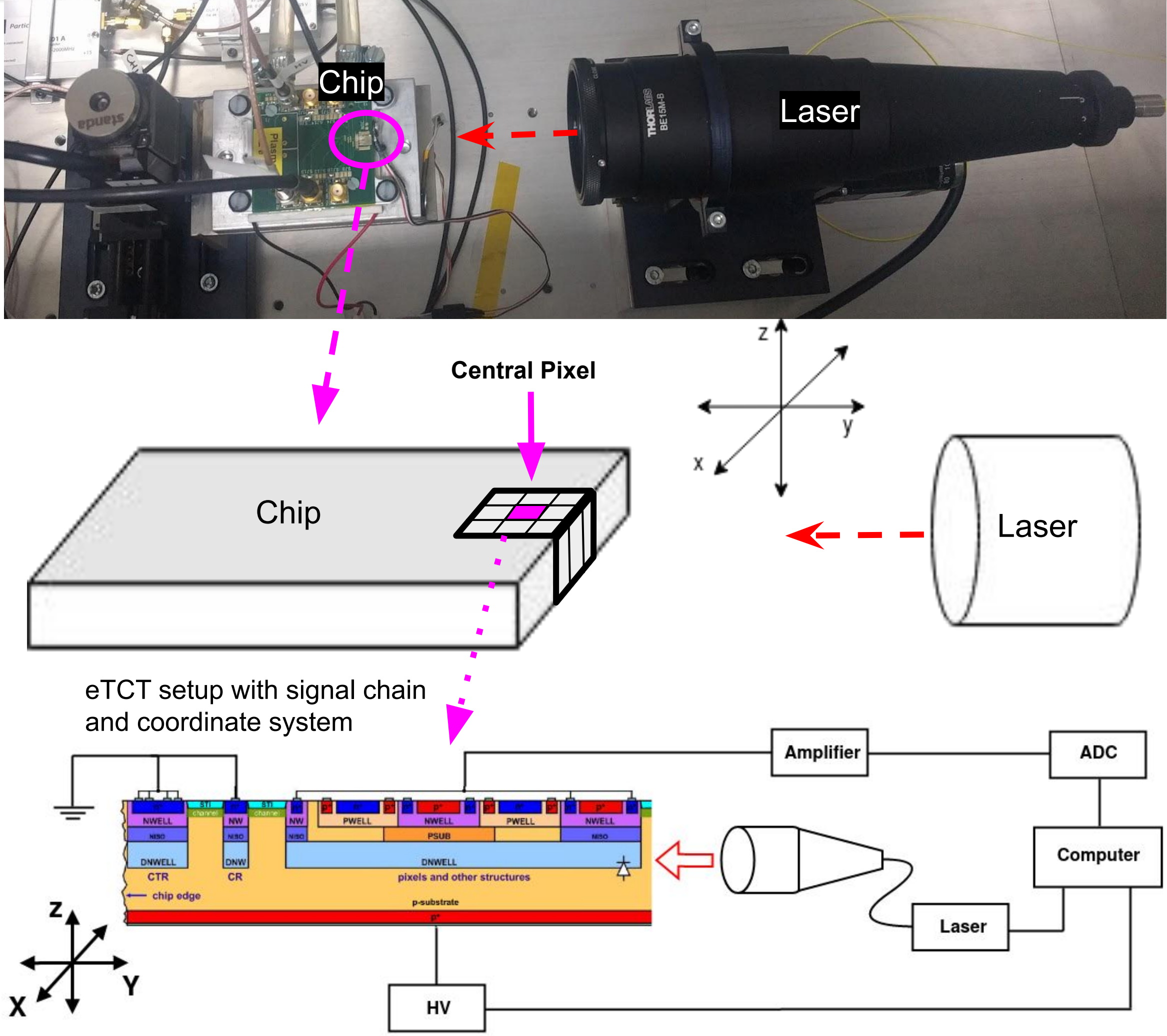




eTCT

- IR laser penetrates silicon
- Induces signal at focal point
- Used to map charge collection region
- Records the collected charge with a laser at a specific point

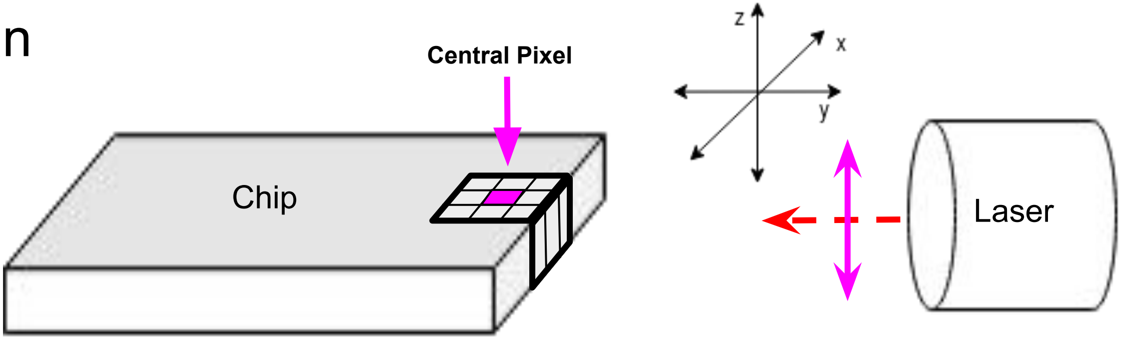
- Cooled to -20 °C temperature
- IR laser, 1 kHz firing
- 200 ns waveforms
- 2 GHz oscilloscope sample rate
- 10 ns integration around current peak



eTCT setup with signal chain and coordinate system

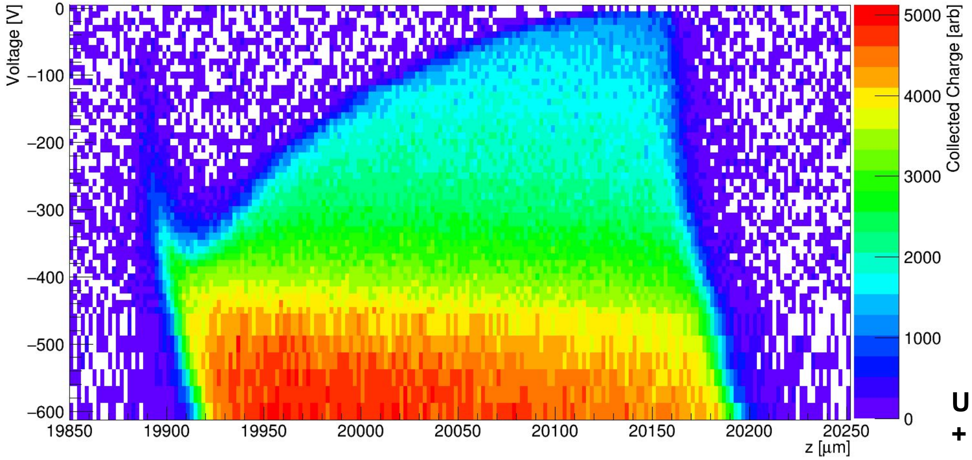
Depletion Depth Voltage Scan

- x and y values fixed
- z scanned (up/down) to measure depletion region growth
- Sensor biased between 0 to -600 V

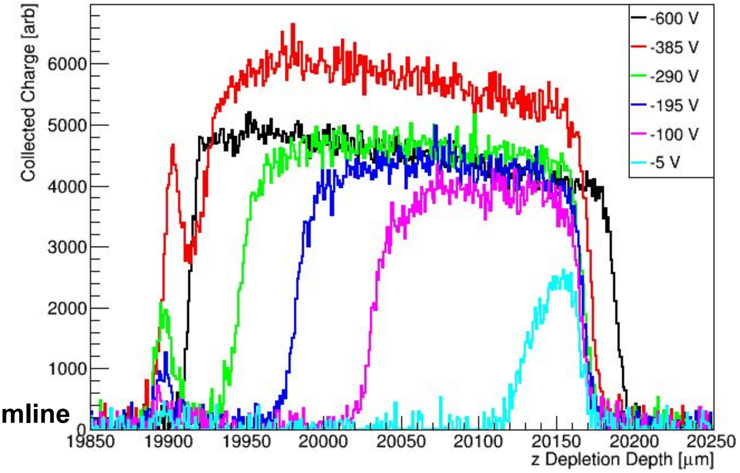


Backside peak

Top of chip



Top of chip



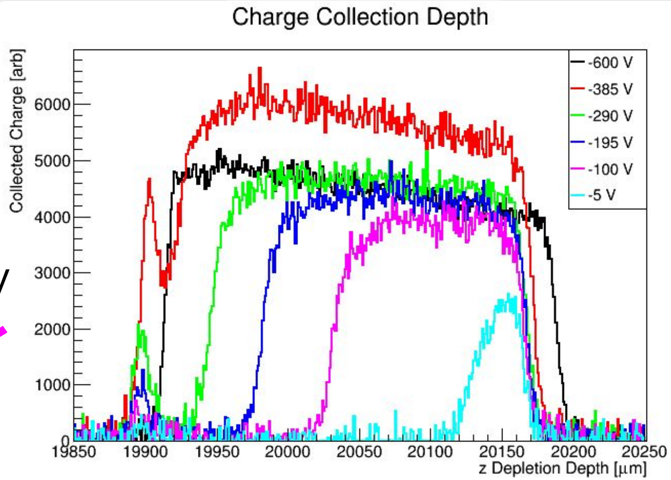
Unirradiated Beamline + RTA sample

Depletion Depth

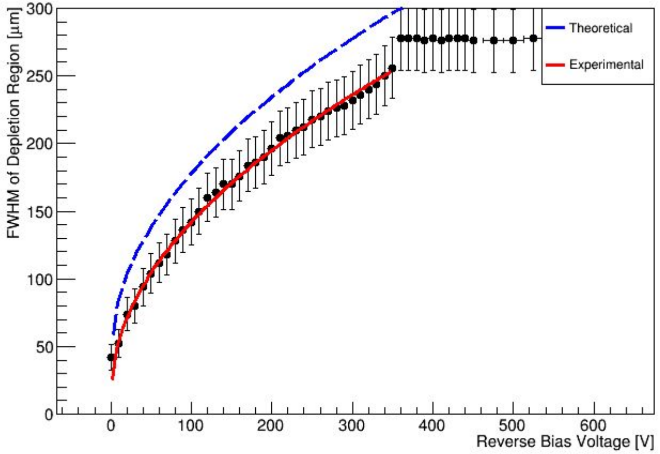
- FWHM of collected charge found for the region at each Voltage
- Substrate resistivity and doping concentration calculated from fit

$$W = W_0 + \sqrt{\frac{2\epsilon_r\epsilon_0}{qN_A}V_{bias}}$$

W = Depletion depth of semiconductor
W_0 = Depletion depth at 0 V
ϵ_r = Relative permittivity of silicon
ϵ_0 = Permittivity of free space
q = Charge of an electron
N_A = Doping concentration of acceptor atoms
V_{bias} = Reverse bias voltage



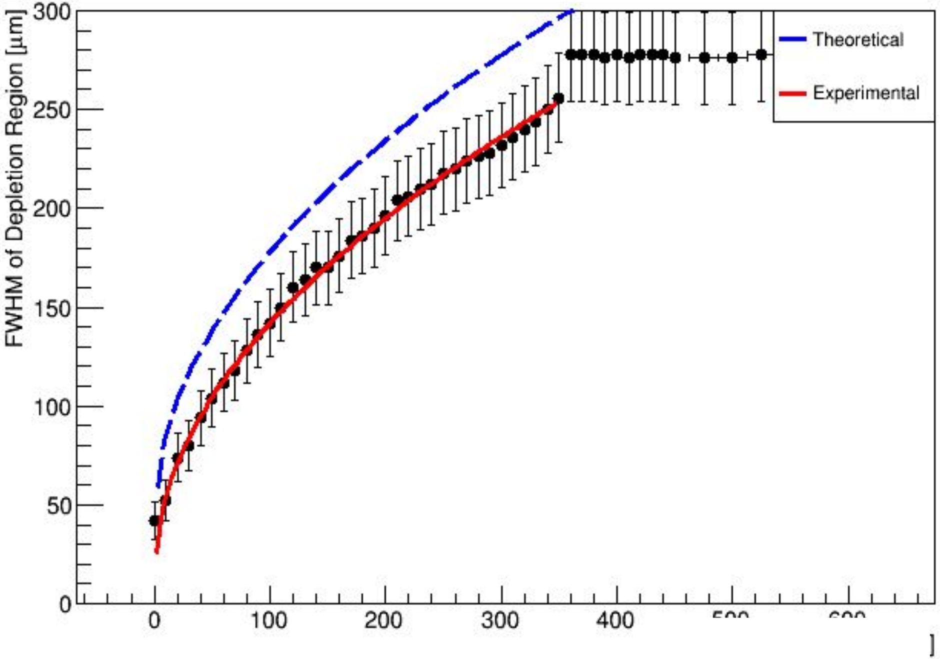
FWHM from all V values



Substrate Resistivity

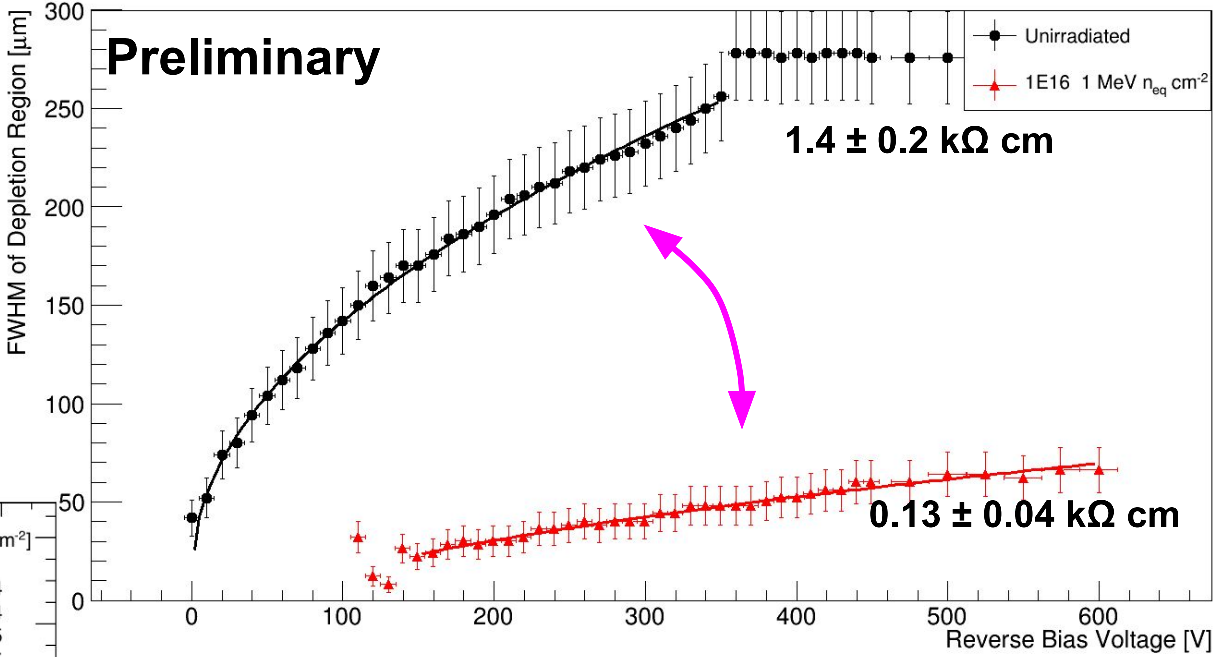
- Unirradiated Beamline Ion Implantation + Rapid Thermal annealing sample measured
- Fit shows resistivity less than nominal
- Inline with RD50-MPW1 with 1.9 kΩ cm

	Resistivity (kΩ cm)
UKRI-MPW0 Nominal	1.9
UKRI-MPW0 Experimental	1.4 ± 0.2
RD50-MPW1 Experimental (same nominal resistivity)	1.3



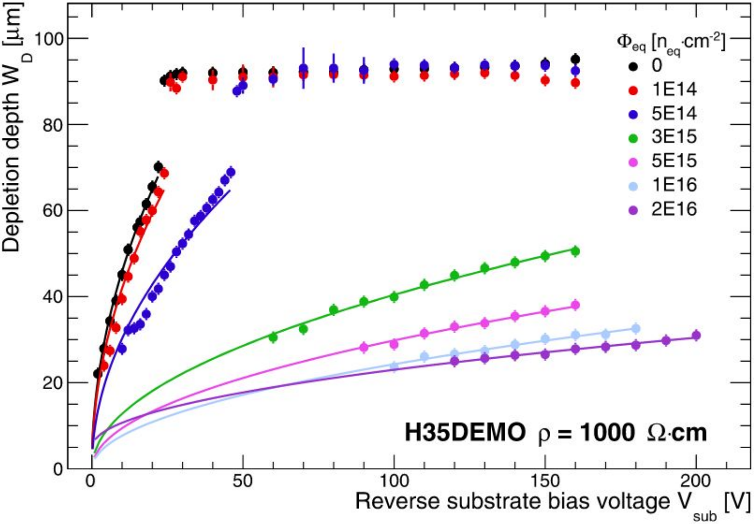
Sneak Peak

More fluences to be measured:
1 x 10^{13} to 1 x 10^{16} 1 MeV $n_{eq}cm^{-2}$

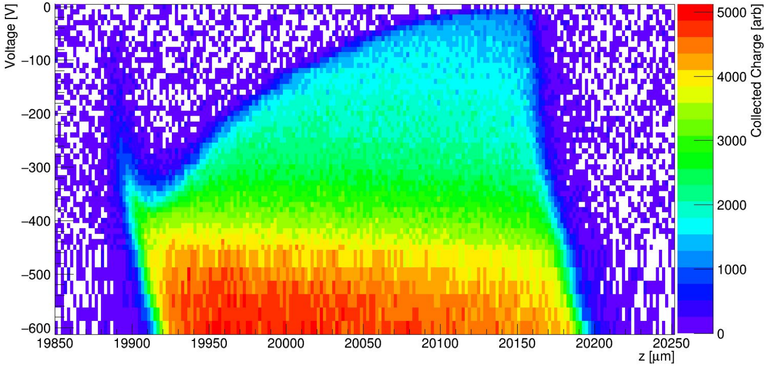


1.4 ± 0.2 kΩ cm

0.13 ± 0.04 kΩ cm



Conclusion & Outlook



- 600 V unprecedented breakdown for HV-CMOS pixel
- eTCT measurements starting to arrive

- Start measuring irradiated samples up to 10^{16} 1 MeV n_{eq} cm^{-2}
- Measure samples of other backside processing method

- Start TCAD simulations of UKRI-MPW1
  - Improve leakage current
  - Remove parasitic channel
  - Increase bias voltages
  - Improve depletion depth with fluence

Tune in next time
Same bat-time, Same bat-channel