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Edge-TCT evaluation of High Voltage-CMOS test structures with unprecedented breakdown voltage for high radiation tolerance

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High Voltage-CMOS (HV-CMOS) sensors can offer a thin, cost effective, and radiation tolerant solution to future experiments using current manufacturing capabilities. At present HV-CMOS sensors are not capable of reaching the time resolution, pixel size, and radiation tolerances specified for the next generation of high luminosity colliders, such as the Future Circular Collider (FCC), or further upgrades to the Large Hadron Collider (LHC). Further research and development is needed for a step change improvement in the performance of HV-CMOS sensors. The monolithic nature of HV-CMOS sensors allows front-end electronics to be embedded in the collecting electrode, isolated from the bulk which gets biased to high voltage. There is no need for bump-bonding like that of hybrid pixels. As the embedded electronics are isolated from the substrate higher biases, compared to conventional CMOS designs, can be achieved giving faster collection times, through drift rather than diffusion, and better radiation tolerance.

UKRI-MPW0 is a proof-of-concept monolithic, backside biased, HV-CMOS chip aiming to improve radiation tolerance. The chip implements a dedicated sensor cross-section, which achieves a breakdown voltage of more than 600 V before irradiation. The sensing junction made between the deep n-well (DNWELL) and the p-substrate uses backside biasing only; an absence of any topside p-wells in direct contact with the substrate further improves the breakdown voltages. UKRI-MPW0 uses a high substrate resistivity of 1.9 k Ω -cm and is in the 150 nm technology of the LFoundry HV-CMOS process.

This contribution presents the first edge-TCT measurements of the test structures, included on the edge of the UKRI-MPW0 pixel chip, irradiated with neutrons to high fluences.

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