Trento Institute for Fundamental Physics and Applications

ARCADIA

Advanced **R**eadout **C**MOS **A**rchitectures with **D**epleted **I**ntegrated sensor **A**rrays

First characterization results of ARCADIA FD-MAPS after x-ray irradiation

Coralie Neubüser, T. Corradino, G-F. Dalla Betta, S. Matiazzo, L. Pancheri
on behalf of the ARCADIA collaboration

29/06/2022

23nd International Workshop on Radiation Imaging Detectors

ARCADIA main demonstrator characterisation

analysis currently ongoing...

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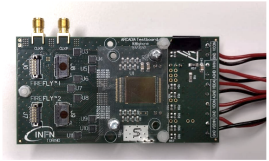
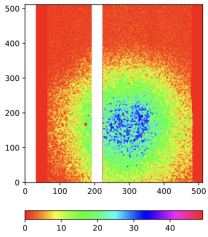


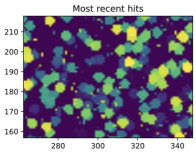
110 nm CMOS CIS technology, high-resistivity bulk, operated in full depletion mode

Pixel size = 25x25 μm^2
Matrix = 512 x 512
Thickness = 200 μm

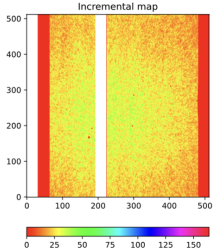
^{241}Am



Few events (zoom)



^{90}Sr



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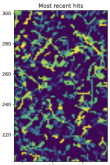
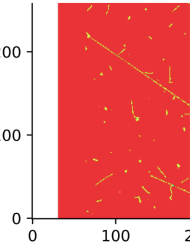


Few cosmic tracks (Tilted sensor)



...more results are coming soon.

Introduction

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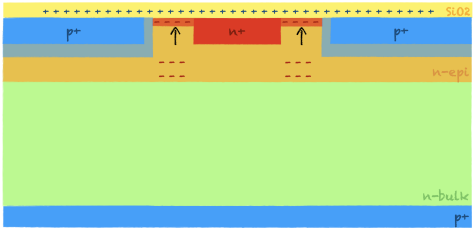

capacitance at nwell is input capacitance to readout chain thus impacts noise of chip

- started investigation of impact of oxide charges on pixel capacitance in 2020 in simulations (different pixel designs for ARCADIA engineering runs)
  [1] [C. Neubüser et al., *Sensor design optimization of innovative low-power, large area MAPS for HEP and applied science*, in Frontiers in Physics Vol. 9 2021, doi:10.3389/fphy.2021.625401]
- presented impact of X-ray irradiation on SEED (predecessor of ARCADIA) samples at iWorid 2021
  [2] [C. Neubüser et al., *Impact of X-ray induced radiation damage on FD-MAPS of the ARCADIA project*, 2022 JINST 17 C01035]

in the meantime... 2 production runs of ARCADIA FD-MAPS.

ARCADIA passive pixel matrices

allow electronics independent process validation and tests for pixel design optimizations

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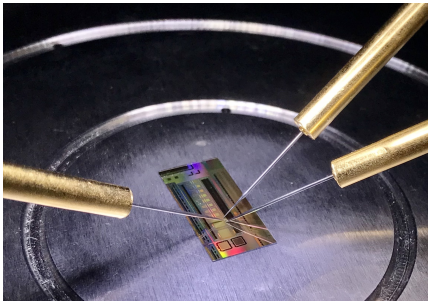
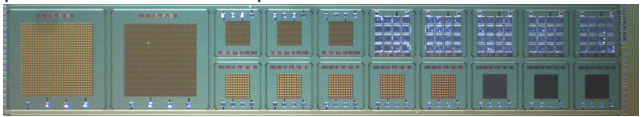
wafer	wafer type	thickness [μm]
20,22	1	48
3,10	2	100
6,15	3	200



- two large $1.5 \times 1.5\,\mathrm{mm}^2$ matrices with pixels of 25 and 50 μm pitch
- $3/3/5$ small $500 \times 500\,\mu\mathrm{m}^2$ matrices with different designs for pixels of $10/25/50\,\mu$m pitch
- each pixel type, one design optimised for low capacitance and one for fast charge collection

picture under microscope:



pitch [μm]	# layouts
50	5
25	3
10	3

IV curves used to match simulation to data per wafer

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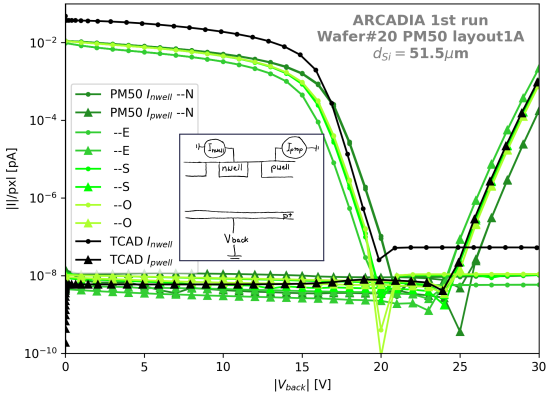

- uncertainties on doping concentrations, thicknesses and implant accuracies taken to reproduce data

variable	uncertainty*
N_{sub}	(42 / 230)%
d_{Si}	(- / 8)%
d_{epi}	(12 / 14)%

*given for 2 main wafer types

- multidimensional parameter space only limited by necessary CPUs for 3D TCAD simulations
- found good matches of the operating voltage range

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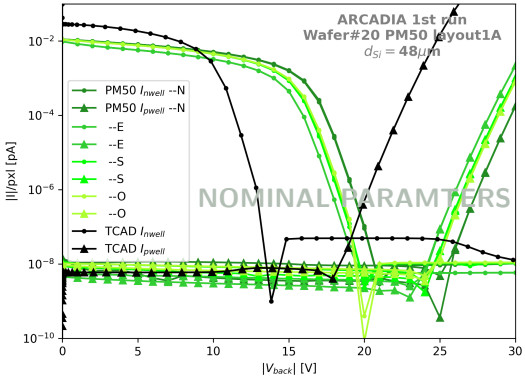

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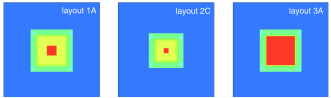
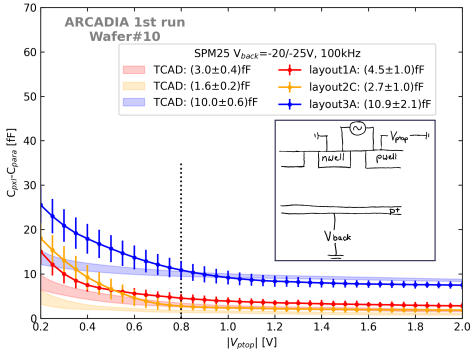
CV curves for different pixel designs

$25 \times 25\ \mu m^2$ pixels





- in simulations observed already at low oxide charge concentrations non-negligible impact on capacitance [1]
- TCAD simulations include N_{ox}=6.5·10^{10} cm^{-3}
- simulations show too low capacitances, potentially underestimated N_{ox}
- found oxide charge concentrations with gated diodes on backside of 1-1.5×10^{12} cm^{-3} [3], but need estimations of frontside

[3] T. Corradino et al., Design and Characterization of Backside Termination Structures for Thick Fully-Depleted MAPS, MDPI Sensors doi:10.3390/s21113809

Leakage current after x-ray irradiation

together with Uni Padova irradiation campaign with x-ray tube with a Tungsten anode, up to a dose of 10Mrad

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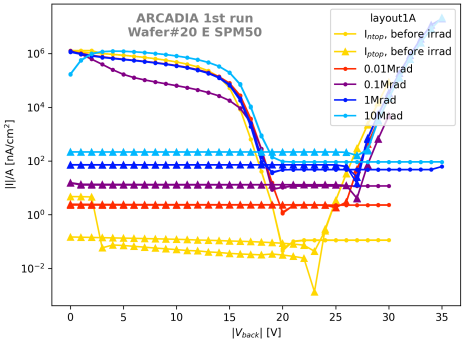

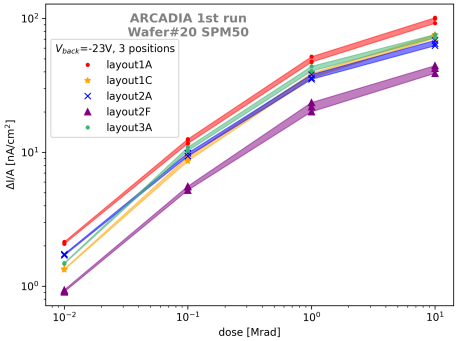

- all measurements performed at room temperature
- after every radiation step, annealing step of 10min@80°C
- stable operating range
- non-linear increase of radiation induced leakage currents with possible saturation >1 Mrad

Modelling of surface damage in TCAD

following New Perugia model [6,7]

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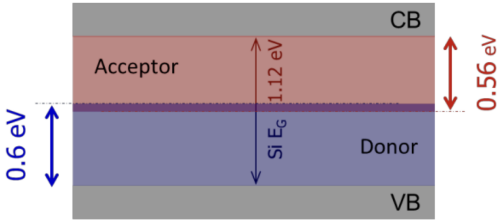
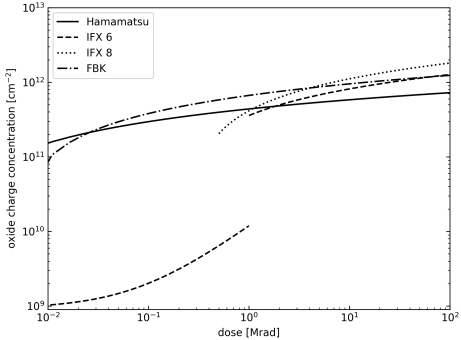
- included positive oxide charge, and 1 acceptor + 1 donor trap



- parametrized on p-type Si from different producers; Hamamatsu, Infineon, FBK
- data points from 50 krad-100 Mrad



- **oxide charge $(1{\cdot}10^{9}\text{-}8{\cdot}10^{10})\,\mathrm{cm}^{-2}$ at 0 dose**

[6] AIDA2020 report,

[7] A. Morozzi et al., TCAD Modeling of Surface Radiation Damage Effects: A State-Of-The-Art Review, Frontiers in Physics doi:10.3389/fphy.2021.617322

CV curves before/after irradiation

$50\times50\,\mu m^2$ pixels

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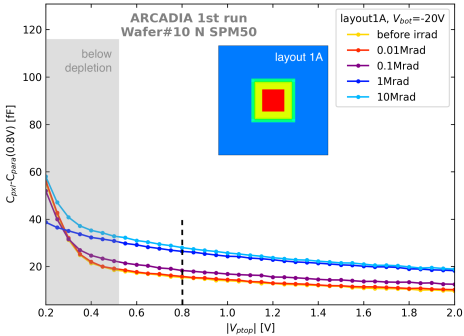

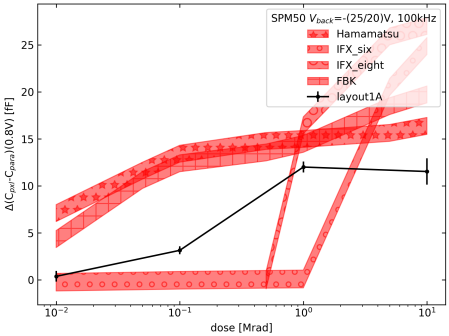

- impact of surface damage on capacitance clearly visible
- capacitance almost doubles after 10Mrad, starting from 15fF before irradation
- comparison with simulation: none of the models describes the data over full dose range

→ included new test-structures in next ARCADIA run to determine trap and oxdide charge concentrations for new paramterisation

Capacitance increase for different pixel designs

$50 \times 50\ \mu m^2$ pixels

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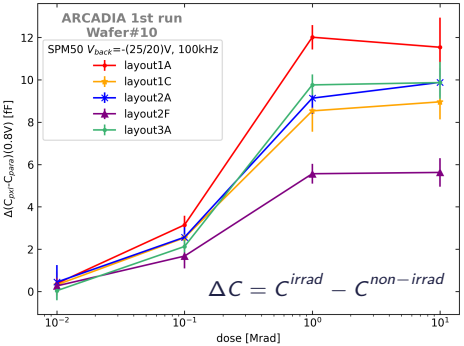
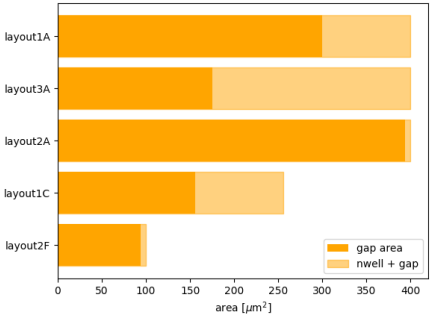


- absolute capacitance increase of up to 12 fF/pixel



- layouts differ in collection node size and gap between n and pwell
- increase of the capacitance is clearly correlated with pwell-free area

Capacitance increase for different pixel designs

$50 \times 50\ \mu m^2$ pixels

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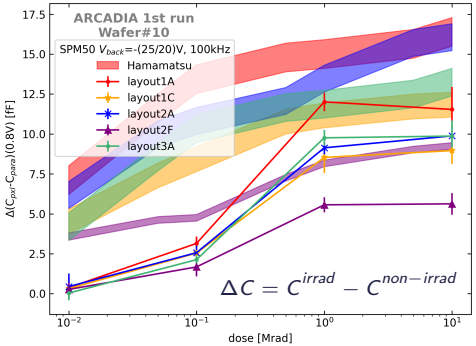

- Hamamatsu parametrisation predicts earlier and stronger increase of capacitance
- good reproduction of the impact of the designs on capacitance
- layout optimised for low capacitance before irradiation, shows smallest impact of surface damage after irradiation

Capacitance-current increase correlation

$50 \times 50\ \mu m^2$ pixels

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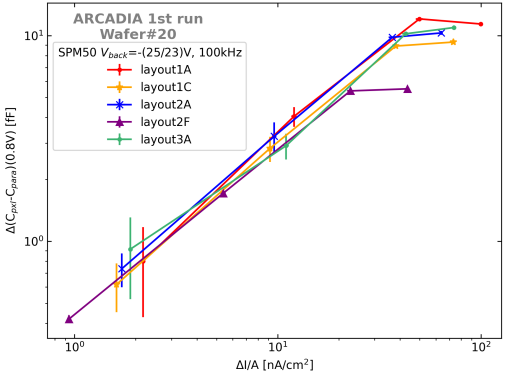

- clear correlation between capacitance and leakage current increase
- all layouts show similar relationship, except for saturation in capacitance which is observed at different stages of leakage increase

Capacitance increase for different pixel designs

$25 \times 25\ \mu m^2$ pixels

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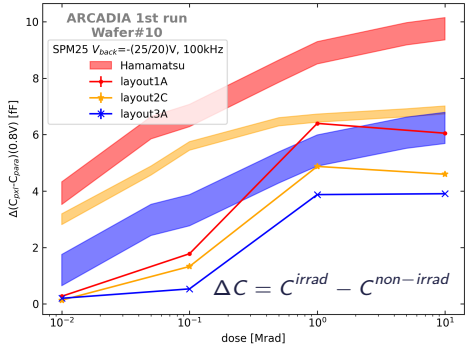

- similar results on matrices with smaller pixel pitch

potentially interesting design of small capacitance (layout 2C):

- 3 fF/pixel before irradiation
- smaller increase after irradiation compared to *default* pixel (layout 1A), currently in use in main demonstrator (MD) chip
- slower charge collection at edges

Conclusions

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- ARCADIA collaboration successfully produced functional sensors in first 2 production runs
- method to adjust TCAD inputs per wafer established and good agreement with measurements achieved
- surface damage non-negligible impact on pixel capacitances, main trends of impact of positive oxide charges validated with data
- radiation damage model needs technology-optimised parametrisation
  $\rightarrow$ gated diodes and MOS capacitors included in 3rd ARCADIA run for characterisation and parameter determination

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THANK YOU FOR YOUR ATTENTION!

ARCADIA collaboration

INFN - Bologna, Milano, Padova, Perugia, Pavia, TIFPA, Torino

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Many thanks!

F. Alfonsi, G. Ambrosi, A. Andreazza, G. Andrini, E. Bianco, G. Balbi, M. Barbanera, S. Beole, C. Bonini, J. Cai, M. Caccia, A. Candelori, D. Chiappara, F. Cossio, S. Cometti, **Thomas Corradino**, T. Croci, M. Da Rocha Rolo, G. F. Dalla Betta, A. De Angelis, G. Dellacasa, N. Demaria, L. De Cilladi, B. Di Ruzza, A. Di Salvo, S. Durando, D. Falchieri, C. Ferrero, A. Gabrielli, L. Gaioni, S. Garbolino, G. Gebbia, R. A. Giampaolo, N. Giangiacomi , P. Giubilato, R. Iuppa, M. Mandurrino, M. Manghisoni, M. Mignone, **Serena Mattiazzo**, C. Neubuser, F. Nozzoli, **Lucio Pancheri**, D. Passeri, A. Paterno, M. Pezzoli, P. Placidi, **Harvey M. Postlethwaite**, L. Ratti, E. Ricci, S. B. Ricciarini, A. Rivetti, R. Santoro, L. Servoli, S. Tedesco, G. Torilla, G. Traversi, C. Vacchi, R. Wheadon, J. Wyss, P. Zuccon

BACKUP

ARCADIA MD1 – specs

trigger-less, and binary readout

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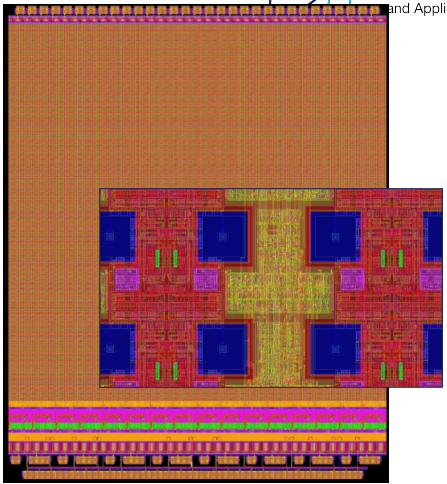
- matrix core 512×512 pxls of $25\,\mu$m pitch
- pixels are $\sim$(50/50)% analog/digital
- sensor diode about 20% of total area
- clock-less matrix (to minimize power dissipation)
- pixel regions propagate the output data to the periphery



Manuel Rolo, INFN Torino