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Development of Low Noise Pixels and Readout Architectures for Scientific Applications in a 180nm CMOS Image Sensor Process

28/06/2022

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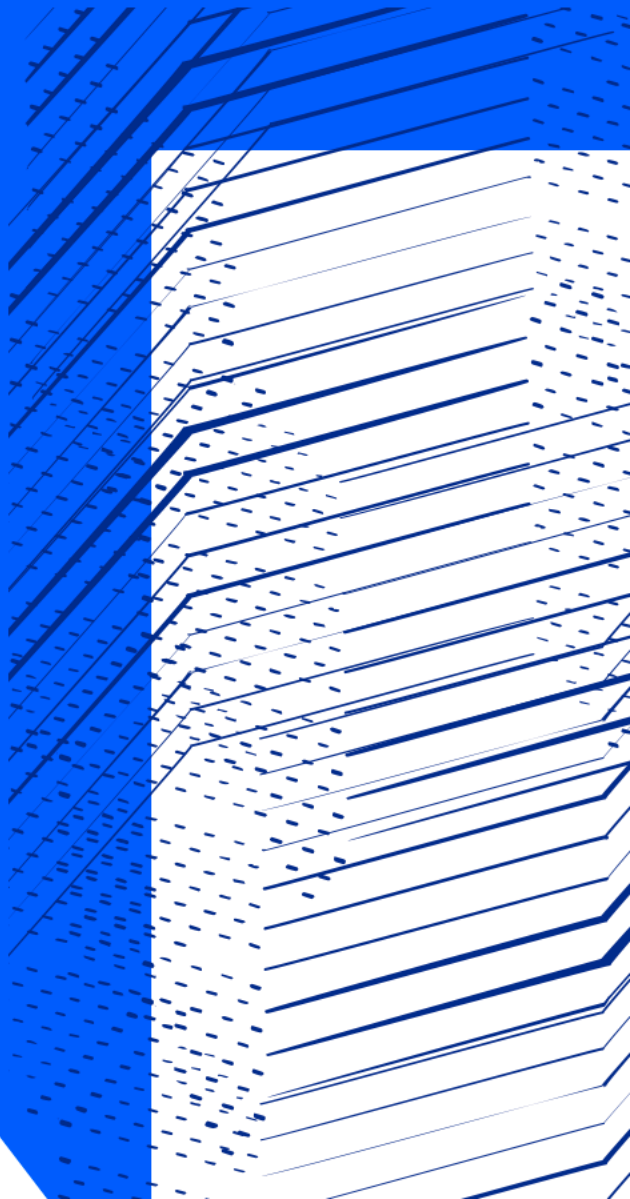
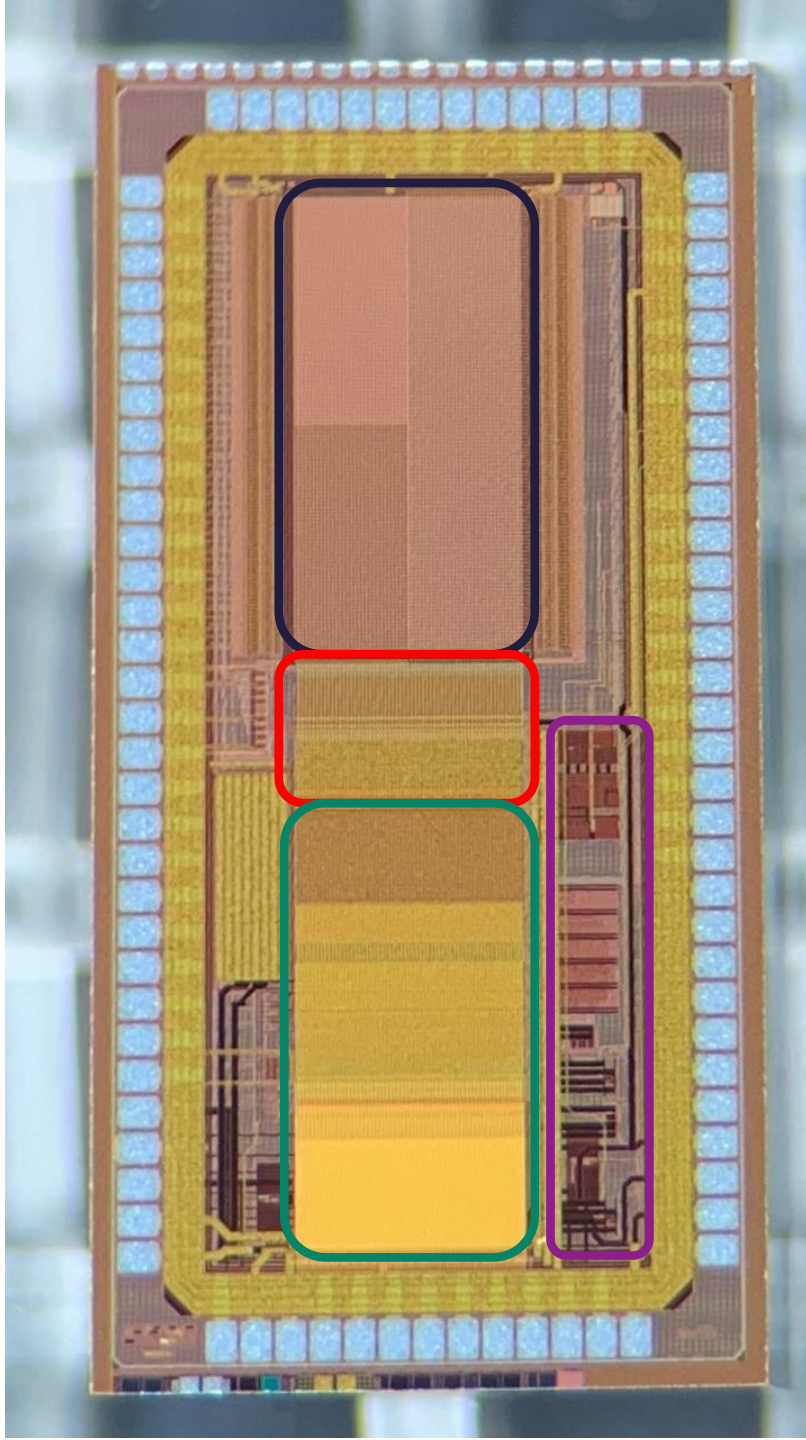


Introduction

Outline

- Motivation
- Chip overview
- Test results
  - **High Gain Pixels**
  - **Programmable Gain Amplifier**
  - **ADC**
- Application to lower gain pixels
- Conclusion



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Introduction

Background

- ASIC development is high risk – prepare IP in advance
- Much work recent on very low noise CMOS pixels [1-4] – exploit for different applications
- High speed data links also key, but for another day…

PRECISE

- Various pixel types – 4T, PMOS SF, 3T, gated diode
- Programmable Gain Amplifier and averaging stage
- Sigma-Delta ADC

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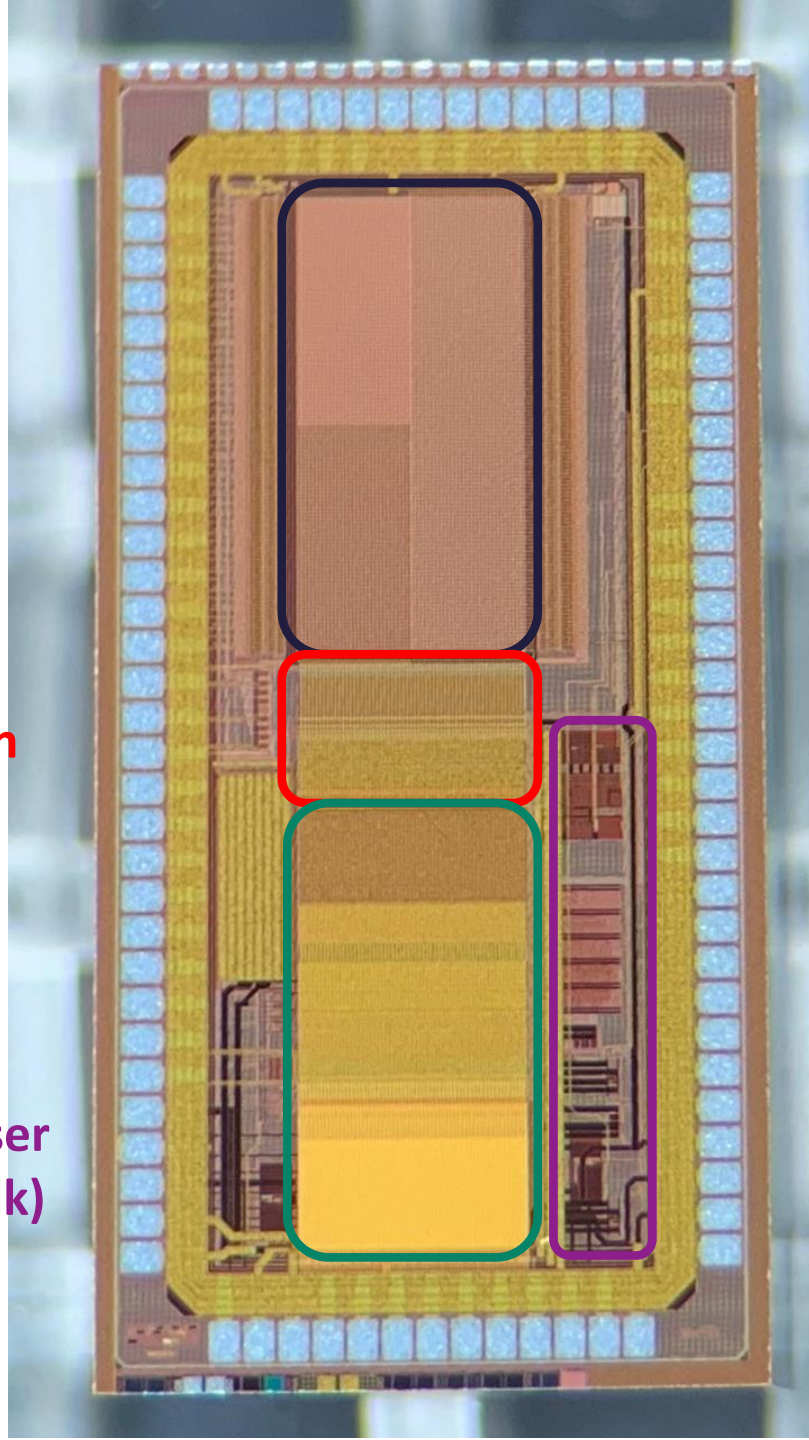

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Chip Overview

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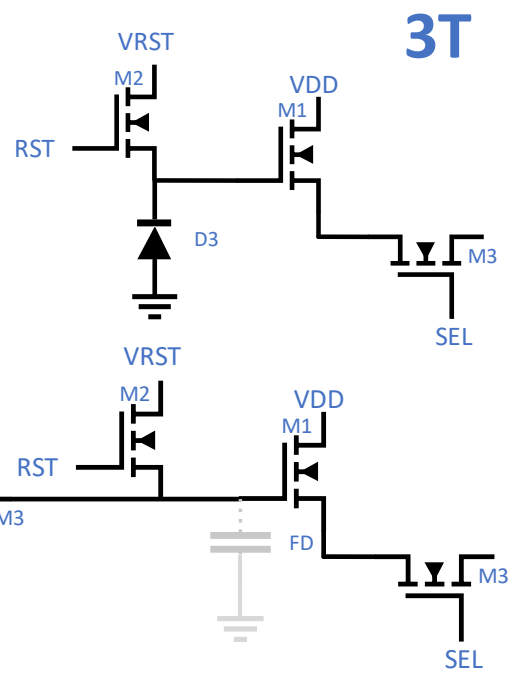
Chip Overview

Pixels

- Chip has 4T and 3T flavours
- 4T
  - Standard gain 4T pixel
  - High conversion gain 4T pixel
  - High conversion gain 4T pixel with PMOS SF
- 3T
  - Gated diode
  - Overflow for HDR



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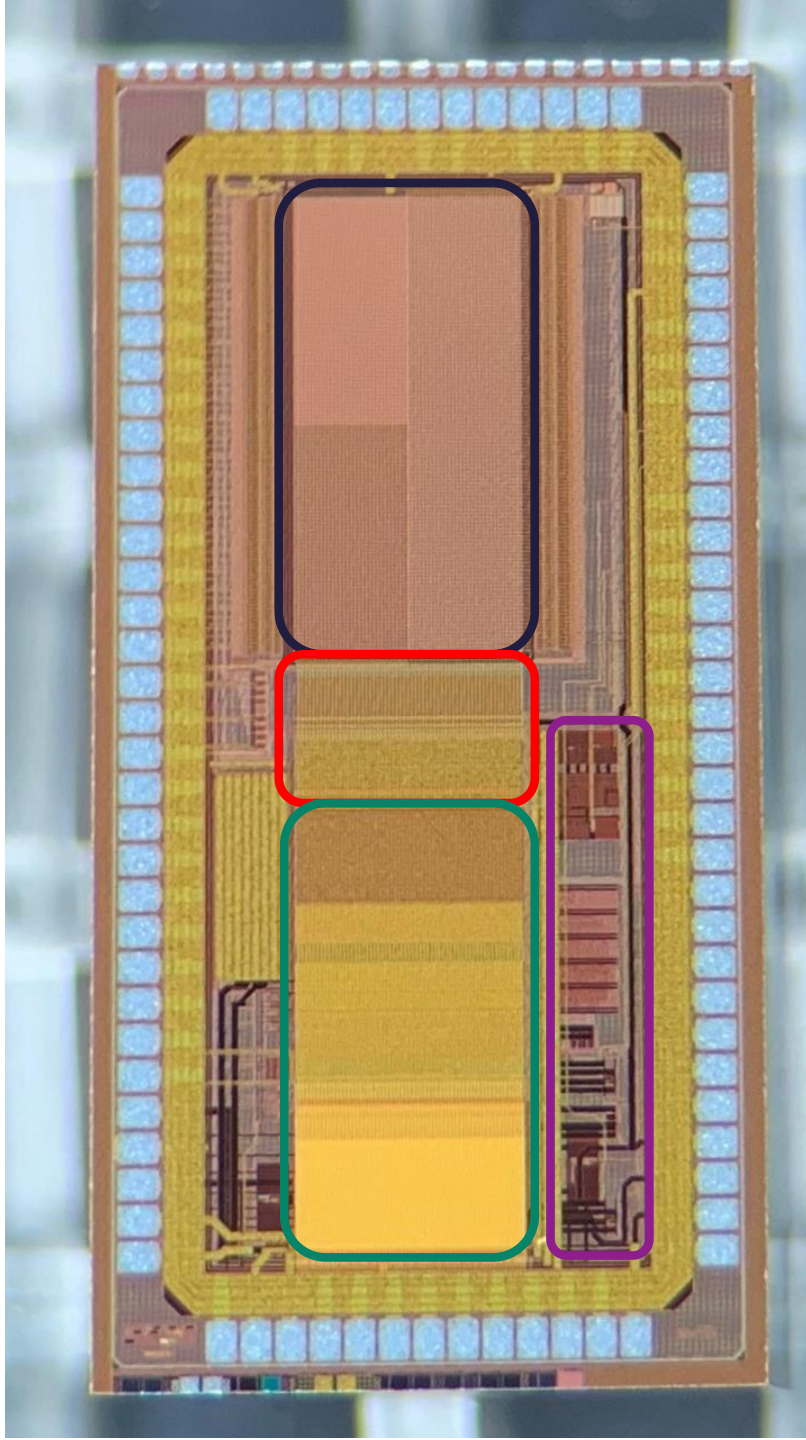
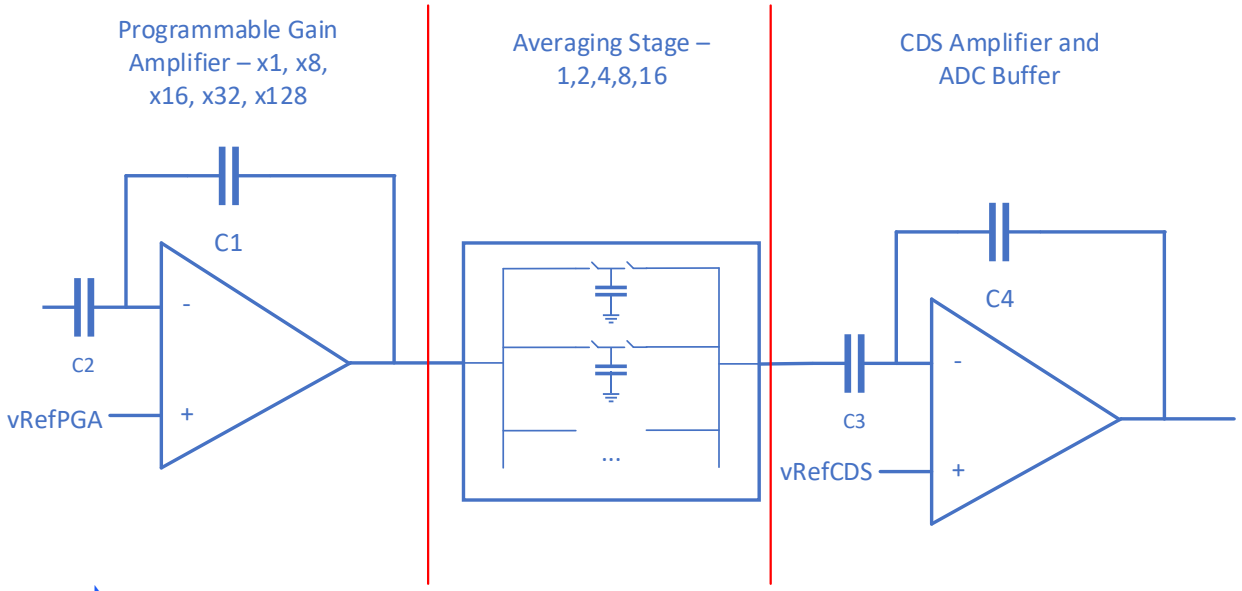


Chip Overview

Analogue Readout Chain

- Capacitive PGA
- Averaging Stage
- Correlated Double Sampling (CDS) Amplifier/ADC Buffer



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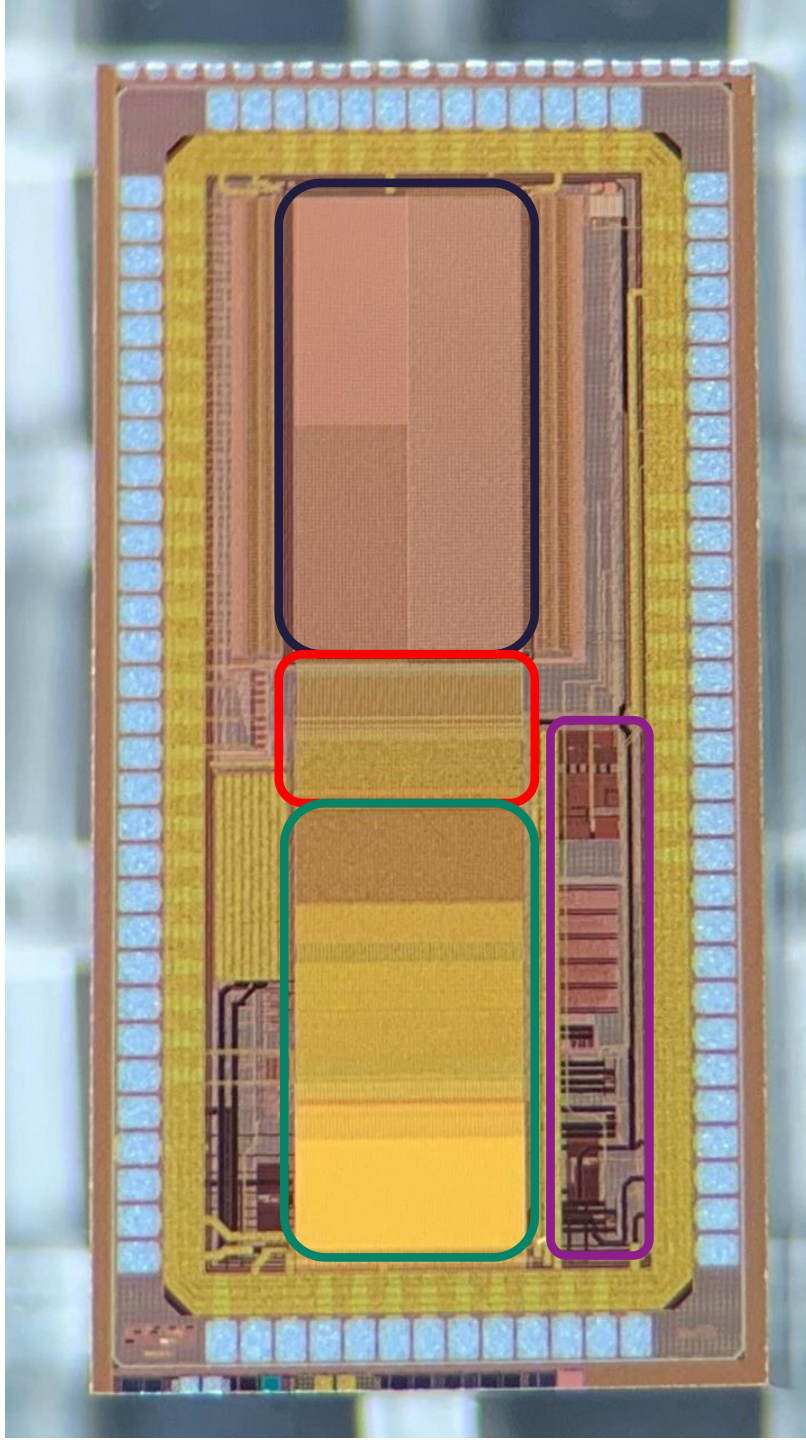
Pixel Array

Analogue Readout Chain

Sigma-Delta ADC

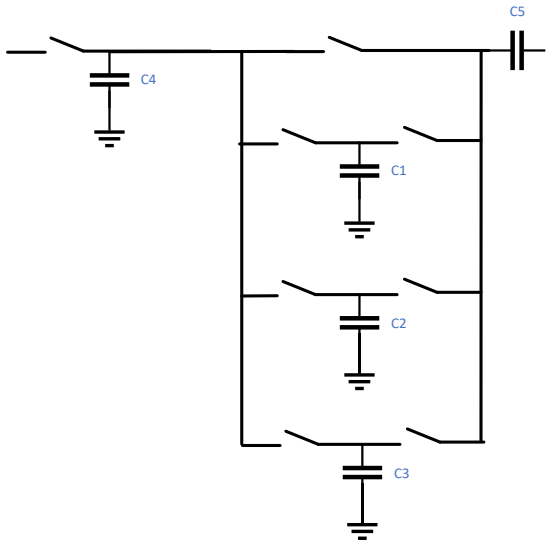
5Gbps Serialiser



Chip Overview

Averaging Stage

- Based on "Experimental Verification of the Impact of Analog CMS on CIS Readout Noise" [5]
- Allows averaging 2,4,8,16 samples
- Only tested up to 2 so far (see following slides)



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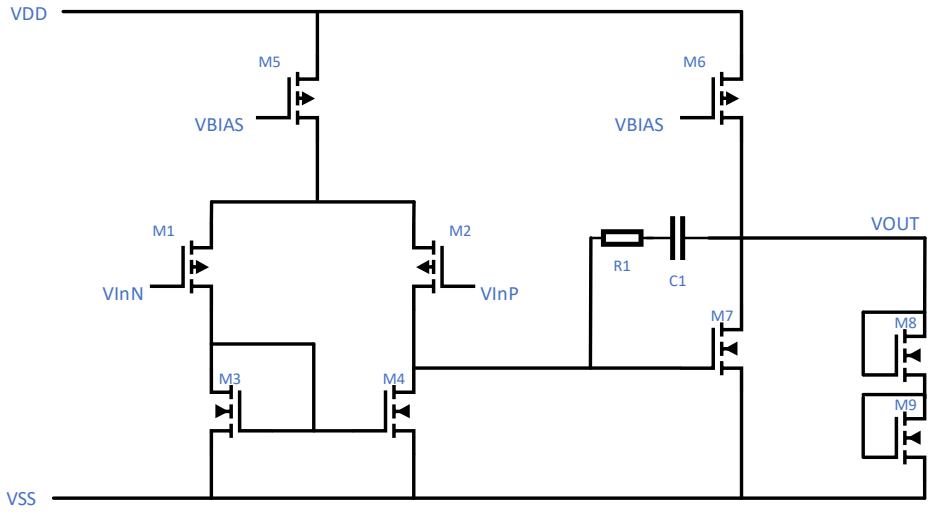
Amplifier

- 2-stage
- Miller compensated with nulling resistor
- PMOS input to match expected pixel range
- Output clamp

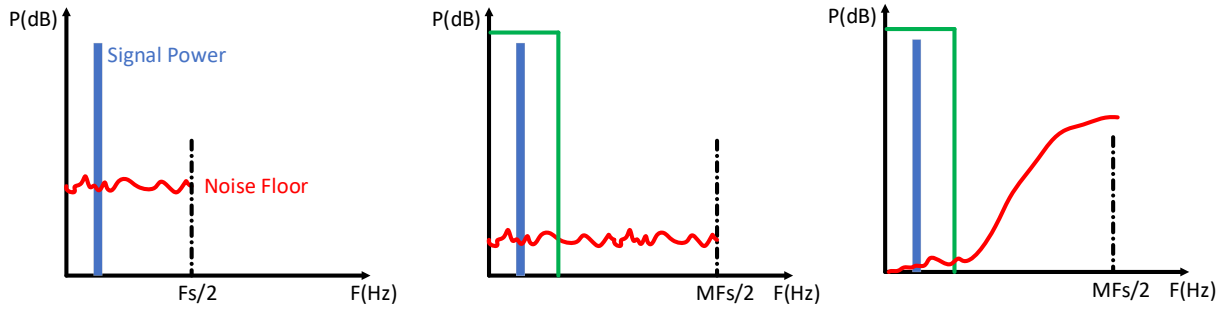


Chip Overview

Sigma-Delta ADC

Advantages over ramp topologies:

- Low Noise
- Highly digital – ease of integration
- Low sensitivity to analogue components – good for large sensor and arrays



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Pixel Array

Analogue Readout Chain

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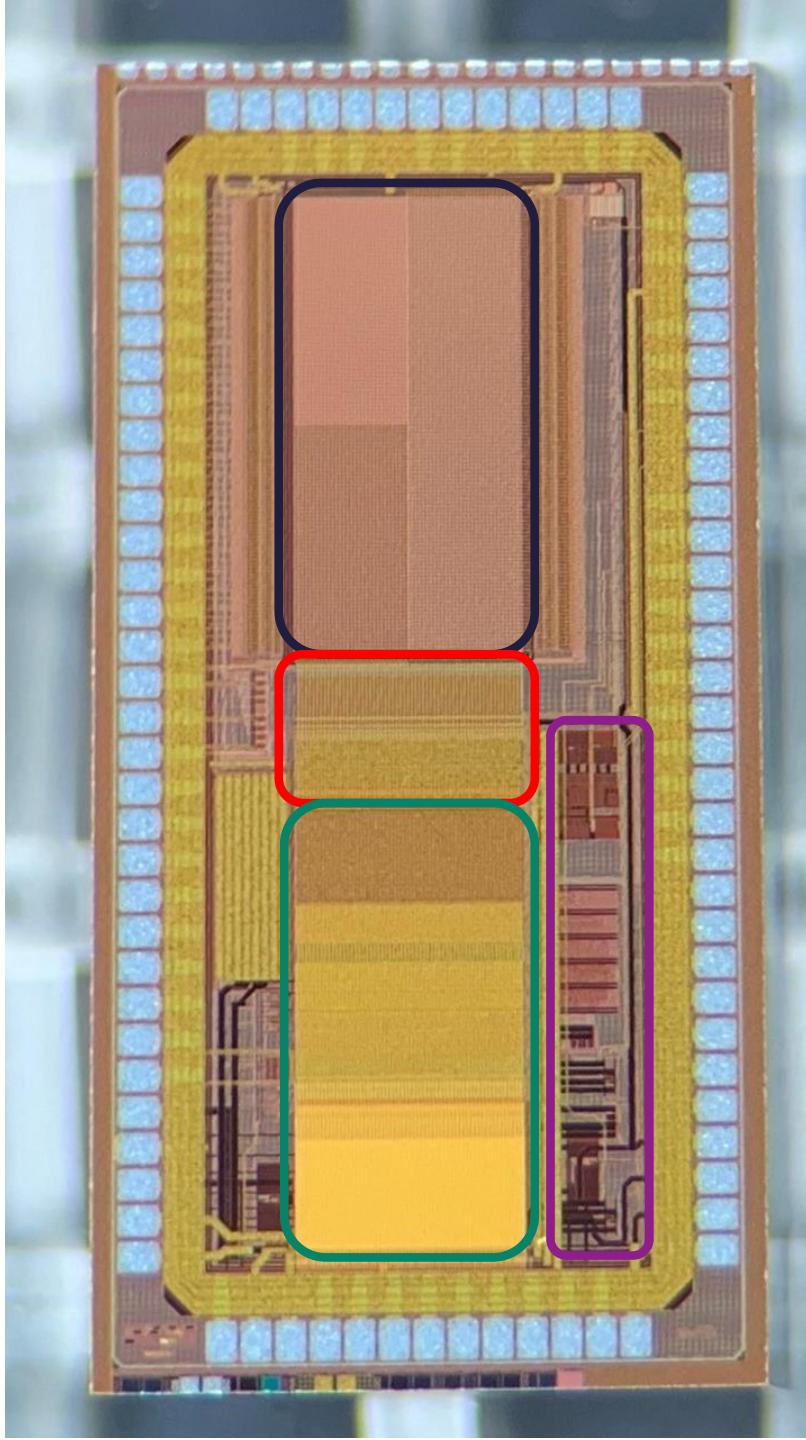
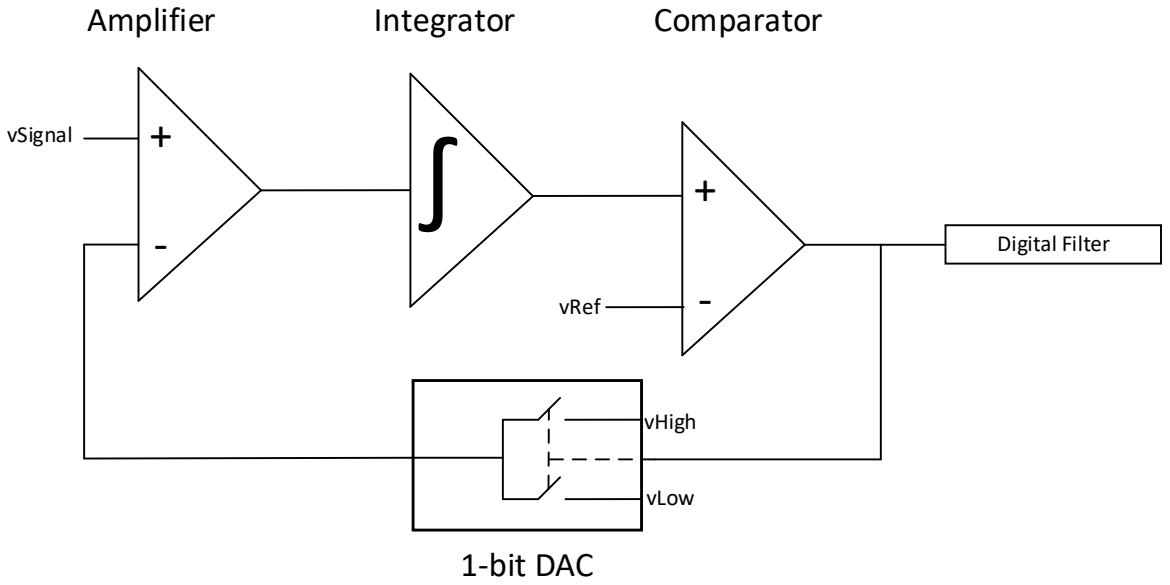


Chip Overview

Sigma-Delta ADC

- Second Order Feed Forward Incremental Sigma Delta
- Reduced area, easier to achieve stability
- Second order reduces OSR, easier to get high speed for a given resolution
- $ENOB \sim 2log_2(M) - 1$



Over Sampling Ratio M and Speed

- 12 bit resolution implies M>=91
- Select 100
- ADC clock of 100MHz for 1MSPS
- Supplied by on-chip PLL
- Max bit depth 17, variable just by changing number of cycles (with speed penalty)

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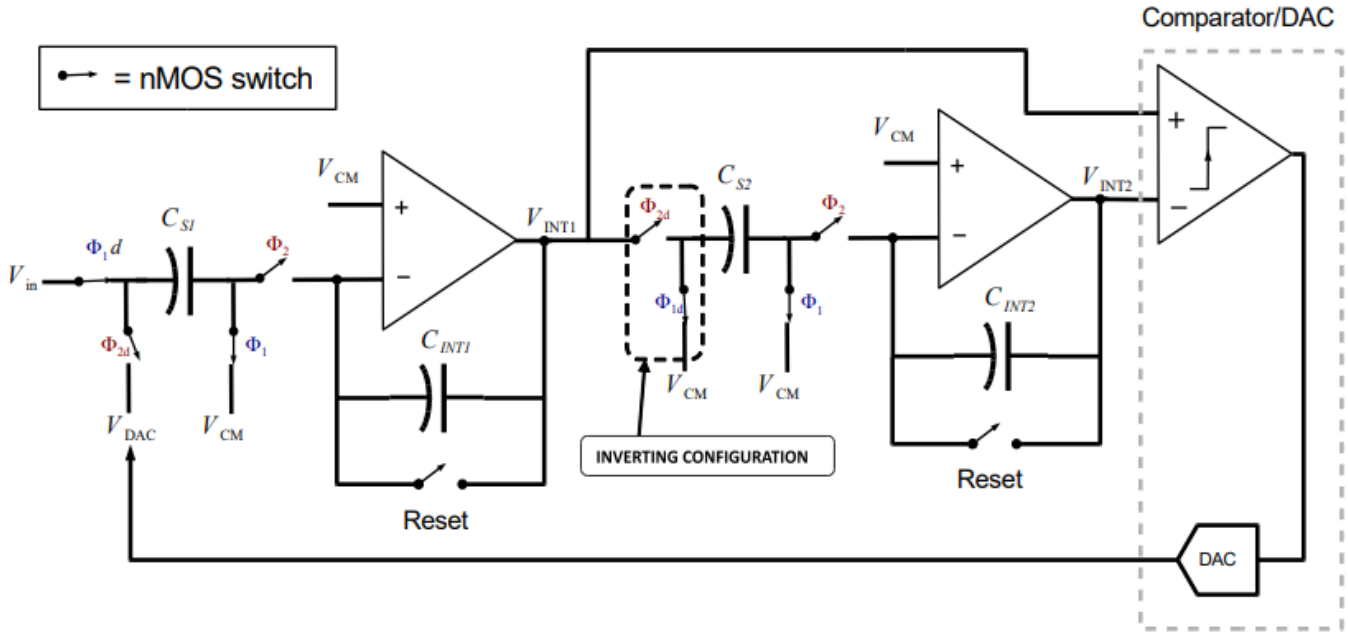

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Testing

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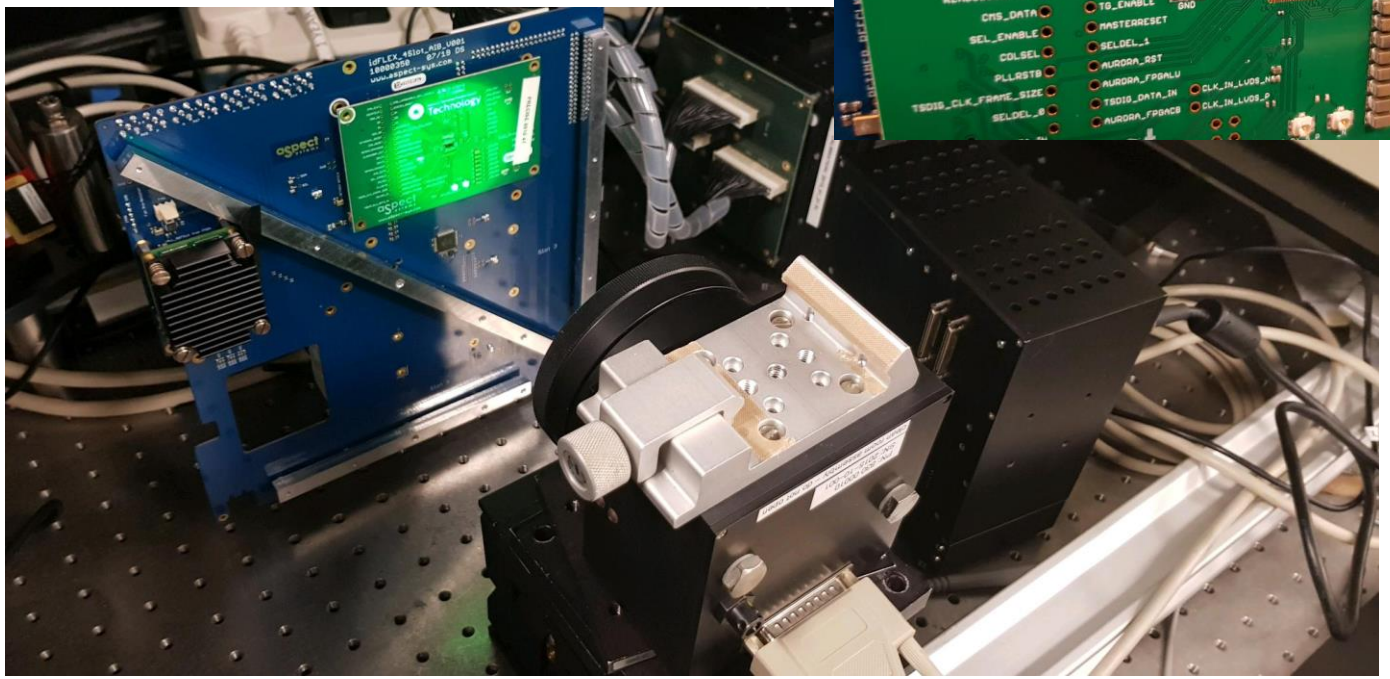
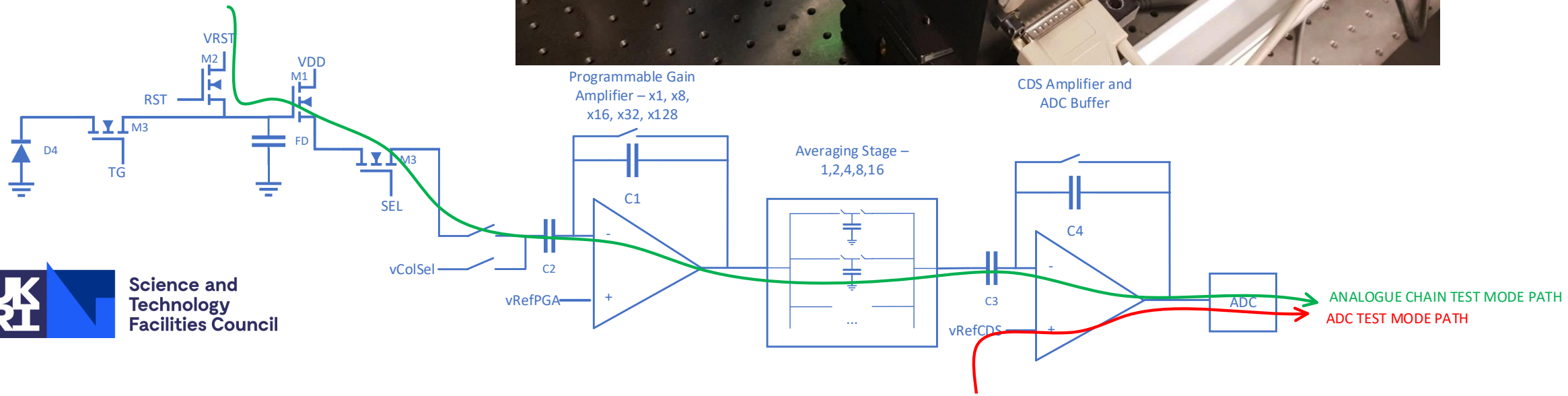
Outline and Test Set-up

Outline

- Test set-up
- ADC Testing
- Analogue Chain Testing
- Pixel Testing
  - 4T Pixels
  - 3T Pixels





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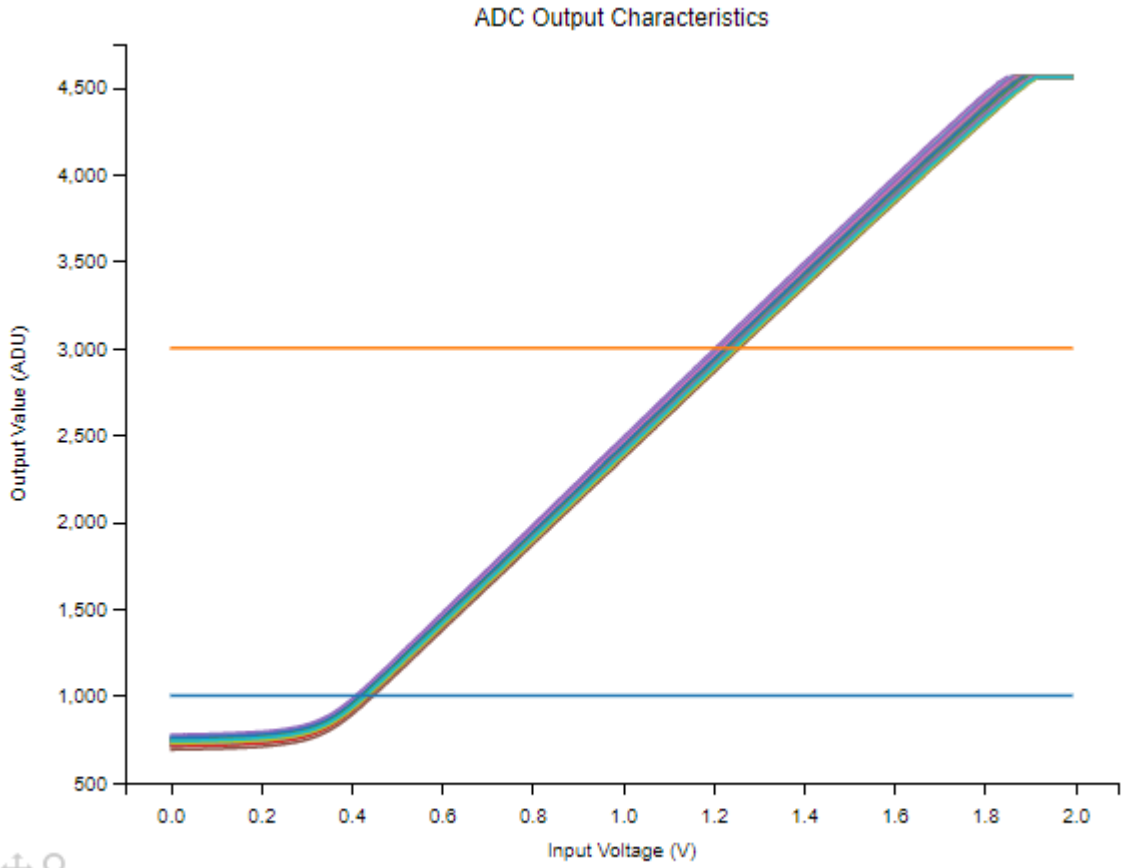
ADC Testing

Quantity	Unit	Value
Gain	ADU/V	2470 ± 20
Max DNL	ADU	1.24
Min DNL	ADU	-0.82
Max INL	ADU	2.26
Min INL	ADU	-7.53
Average Noise	uV rms	323



NOTE: Lines indicate the limits between which ADC gain is calculated

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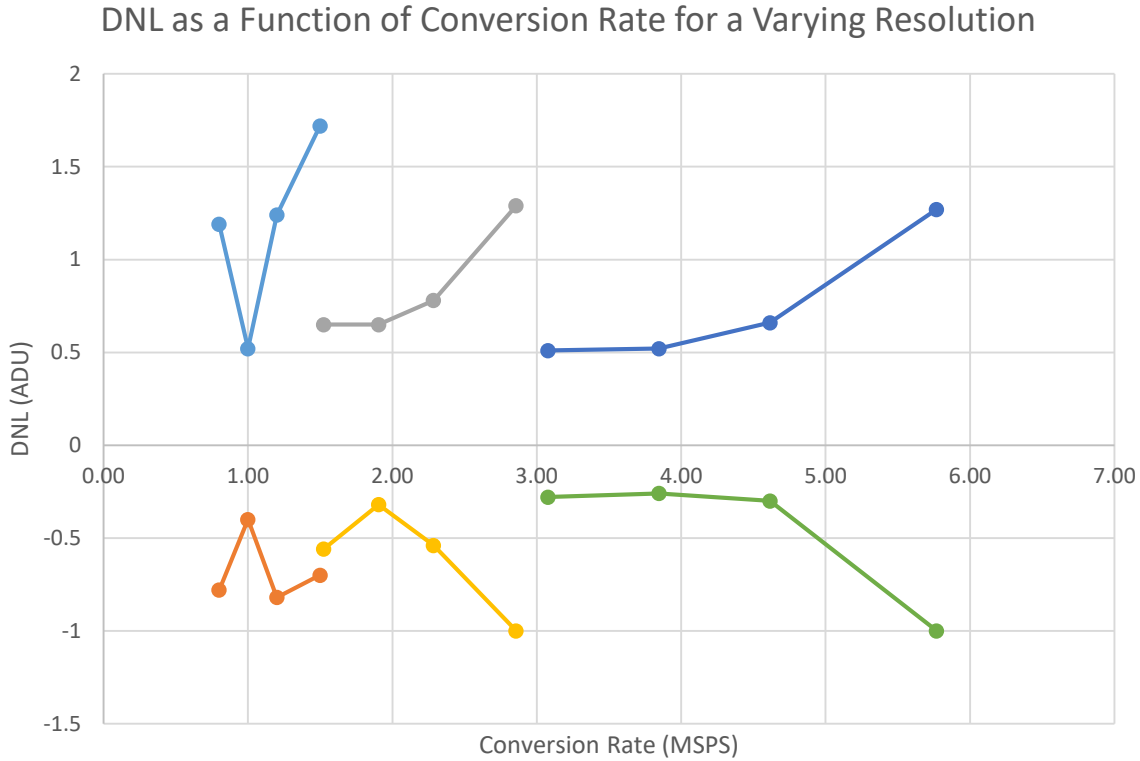
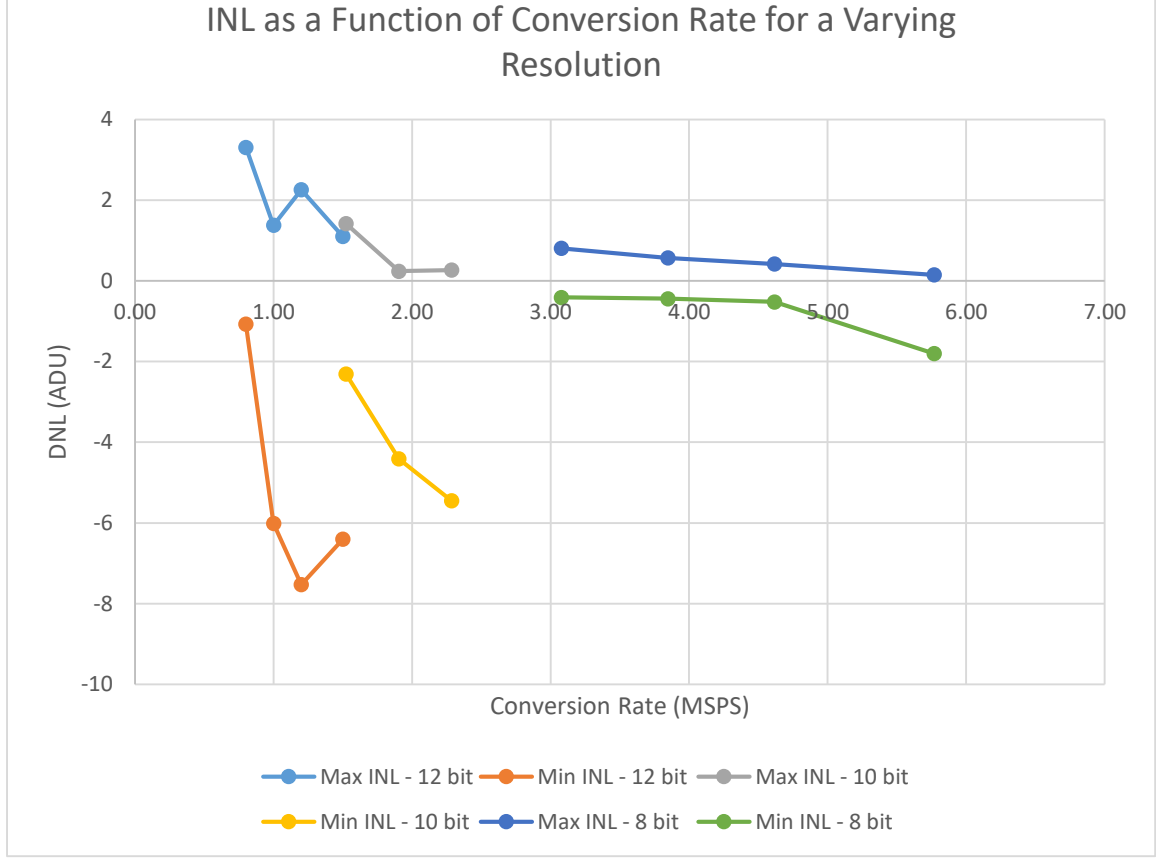
ADC Testing





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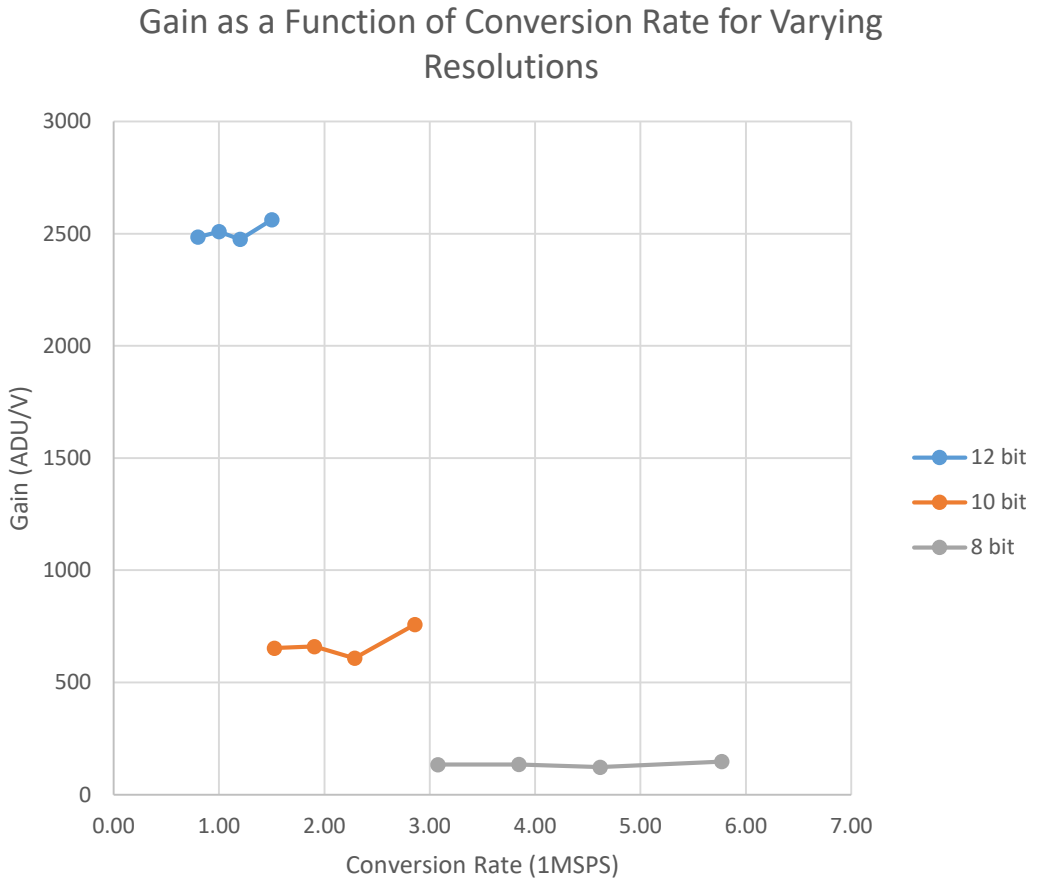
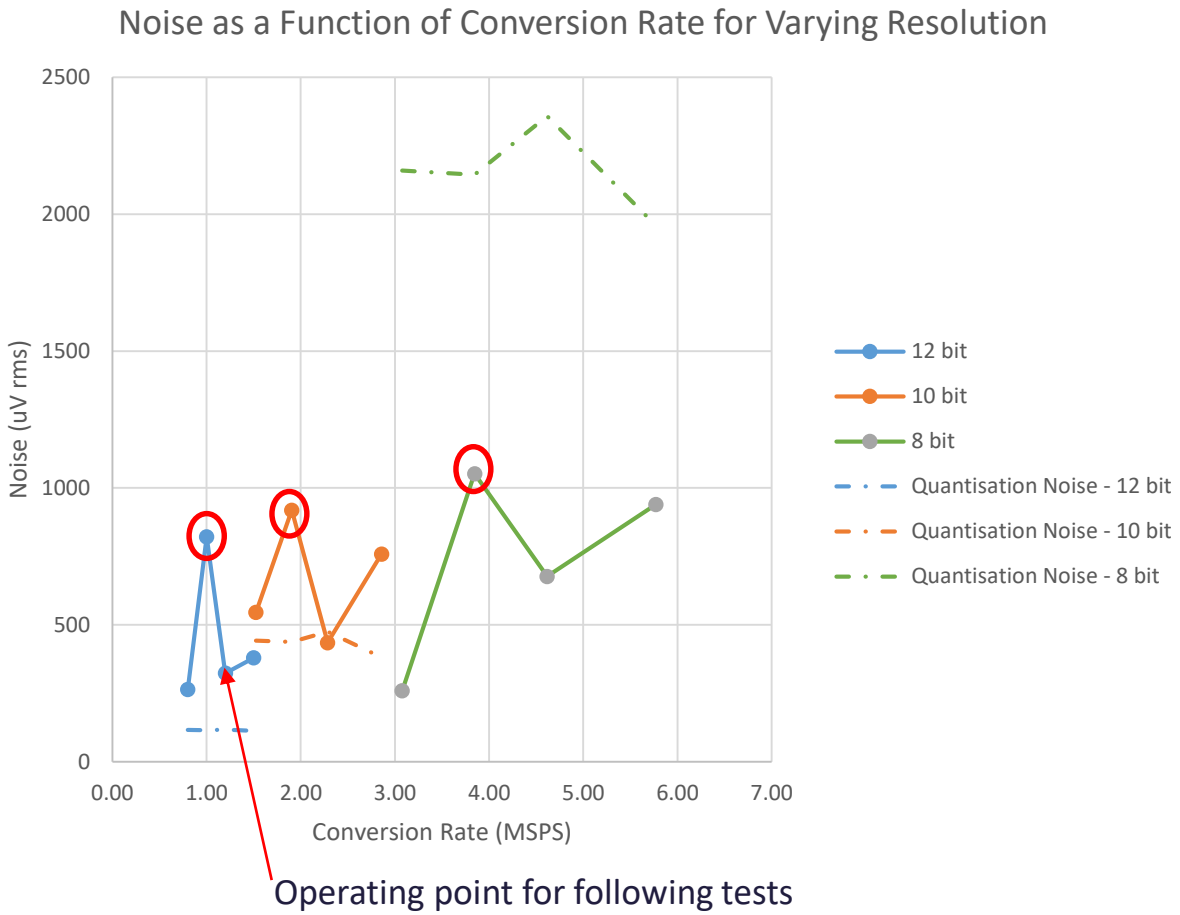
ADC Testing





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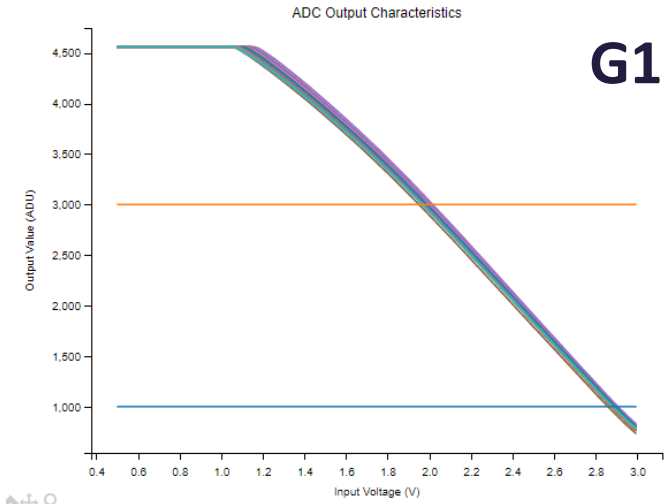
Analogue Chain Testing

Analogue Chain

- 5 gains. Nominally:
  - G1 – 1
  - G2 – 8
  - G3 – 16
  - G4 – 32
  - G5 - 128



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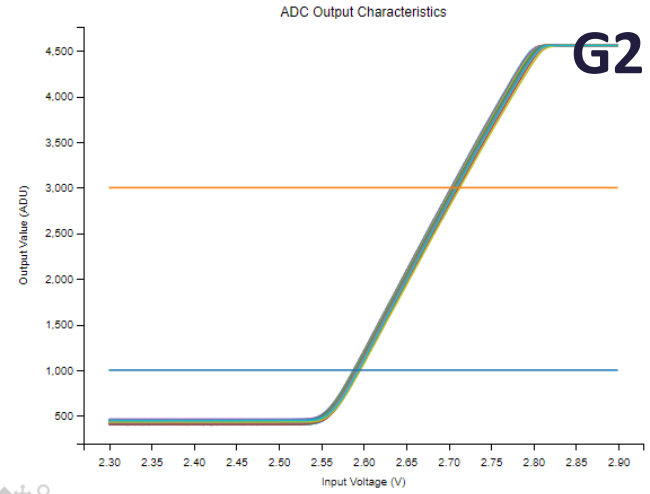

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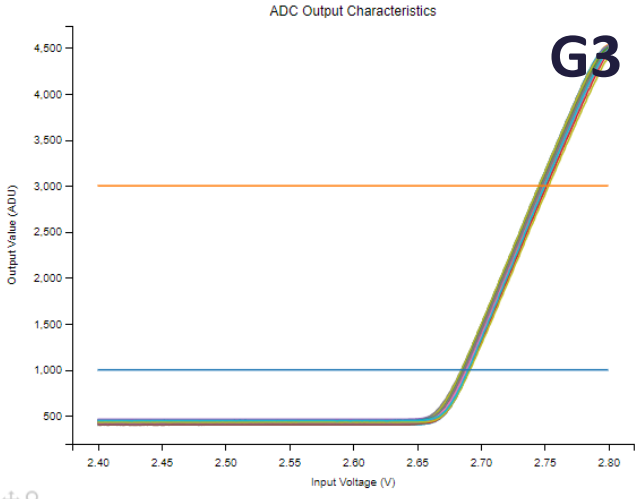

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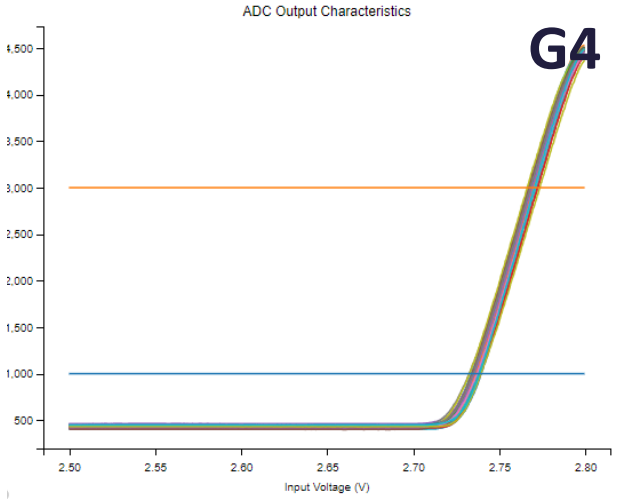

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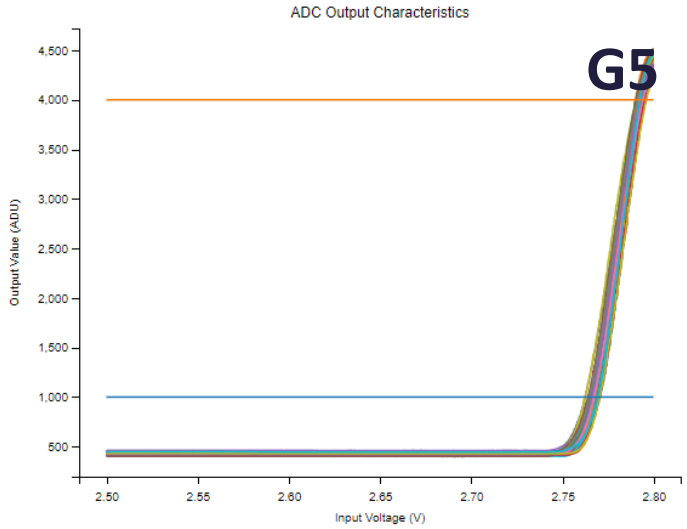

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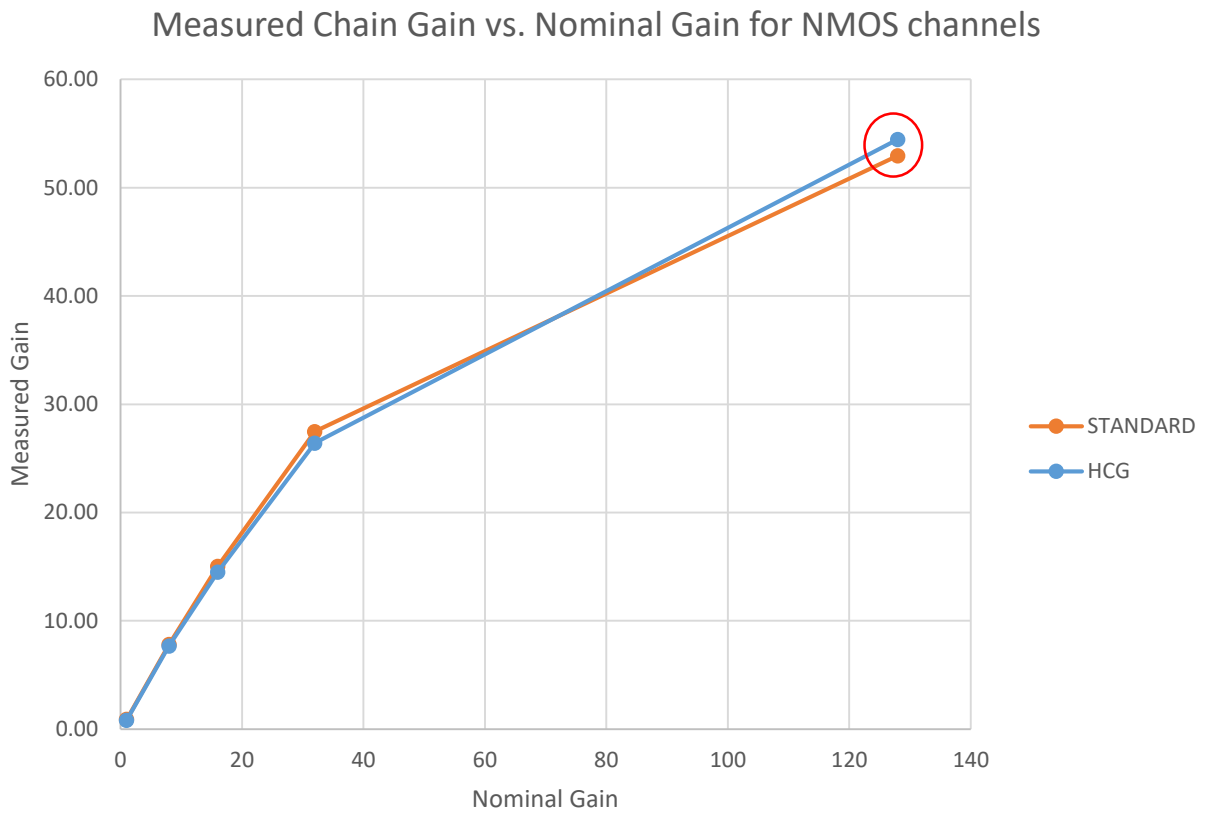
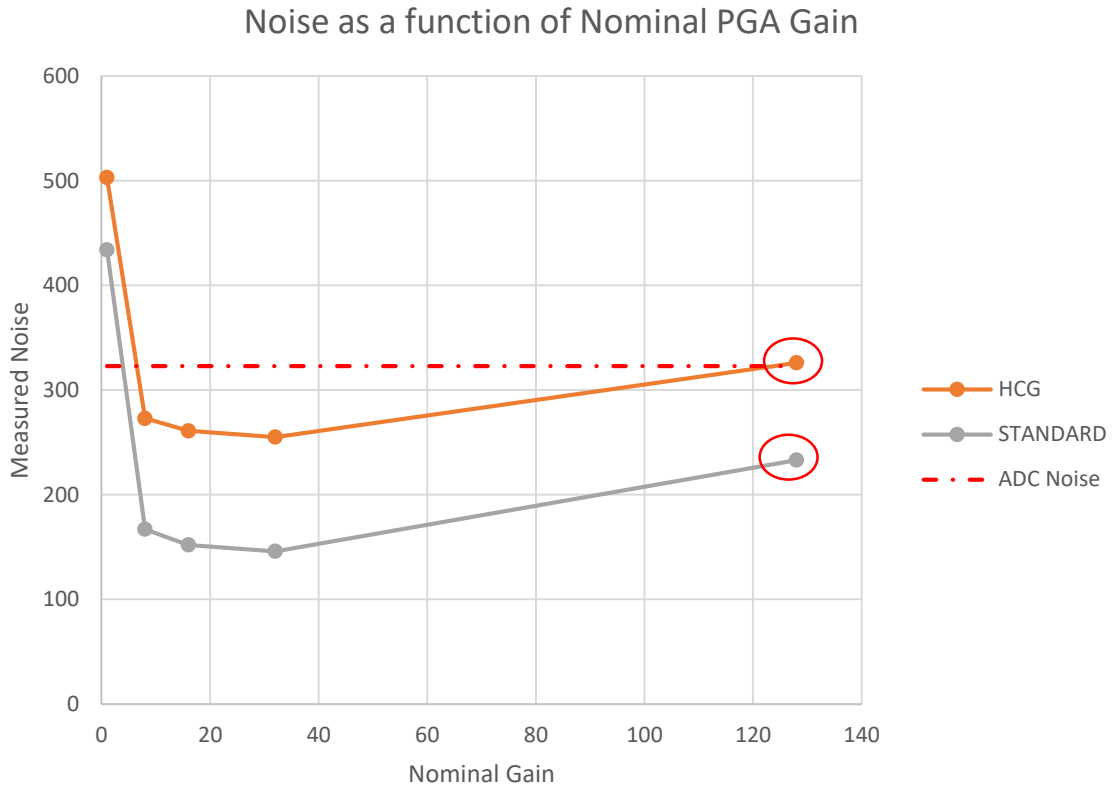
Analogue Chain Testing





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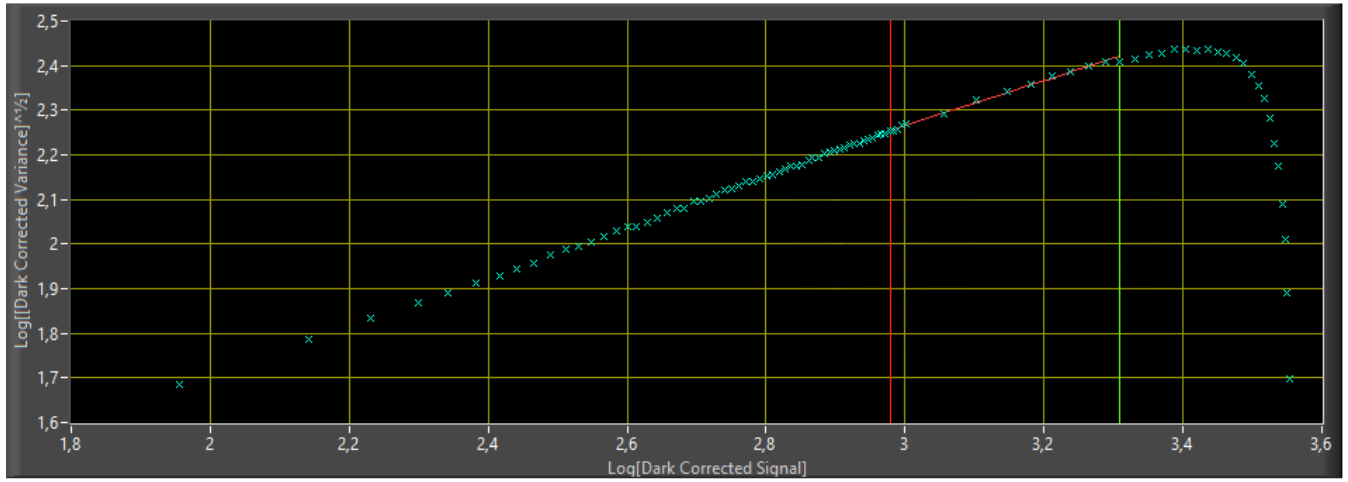
Reduced Nominal Gain x128 due to systemic error

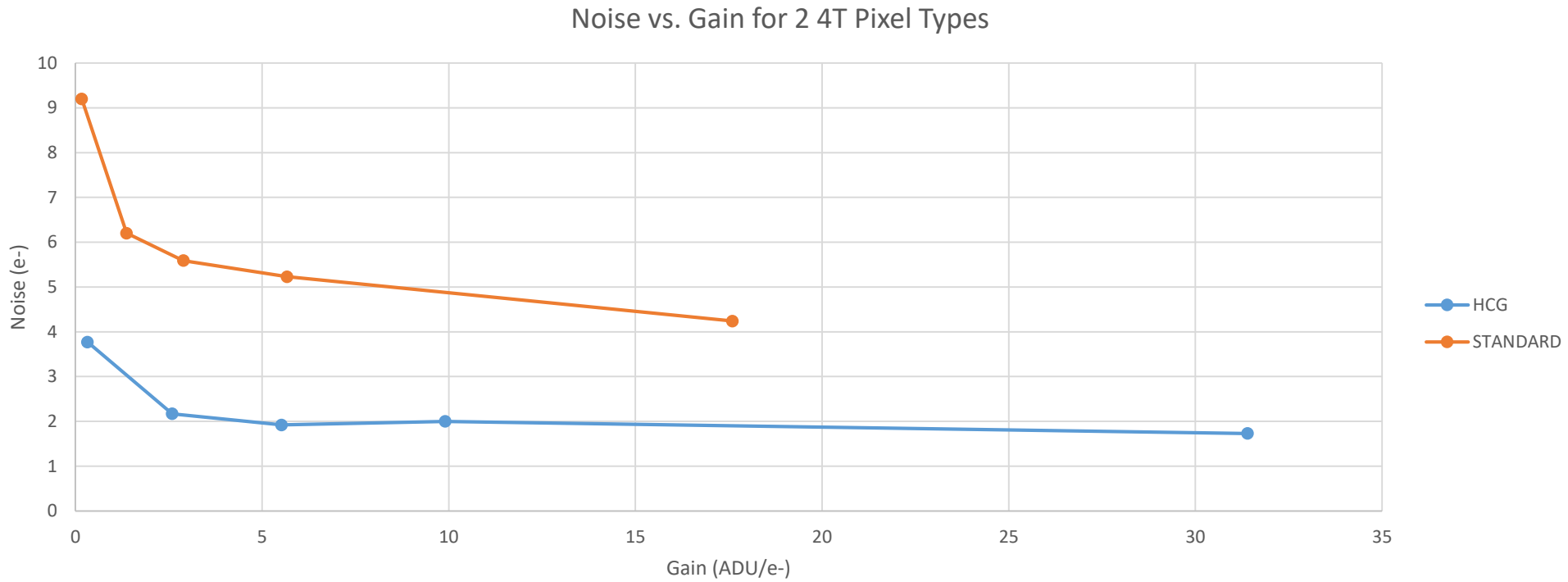
Pixel Testing – 4T

4T Pixels

- 2 types – different conversion gains
- Tested for all gains of the PGA
- Best noise level < 2e-



Photon Transfer Curve – 4T HCG Pixel using G5



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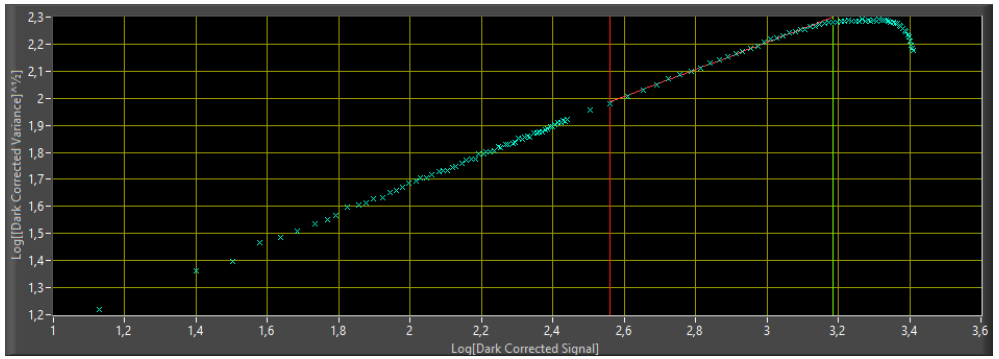
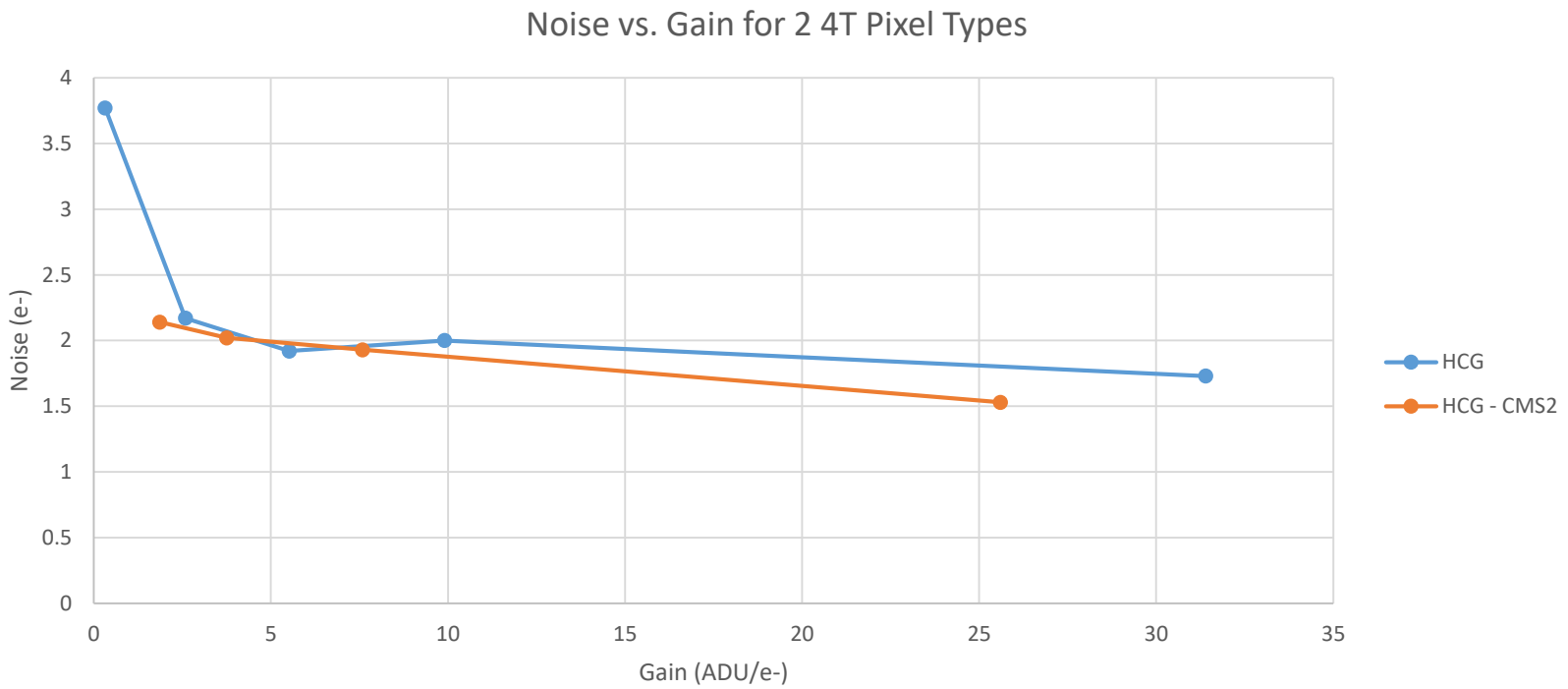
Pixel Testing – 4T

Averaging Stage

- Sampling the pixel twice and averaging allows the noise to be reduced to almost 1.5e-
- Gain is slightly reduced when averaging



Photon Transfer Curve – 4T HCG Pixel using G5 and CMS2



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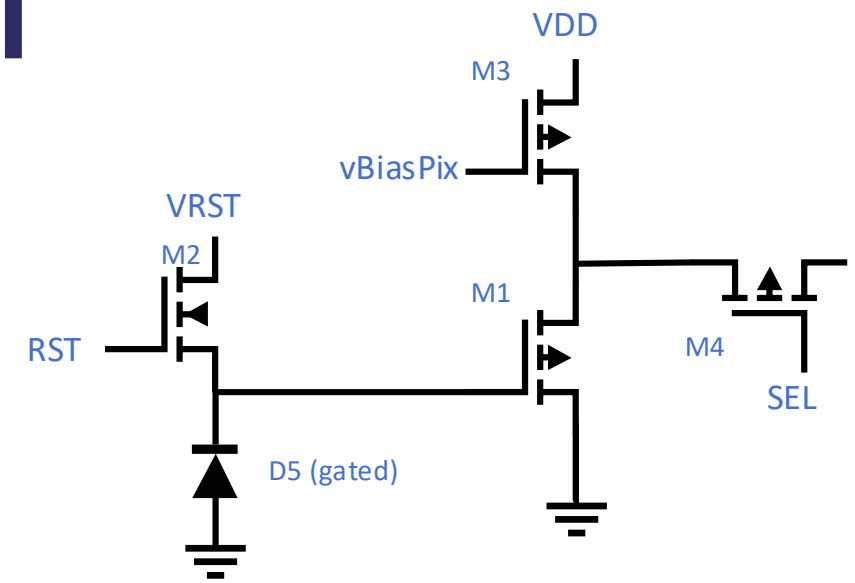
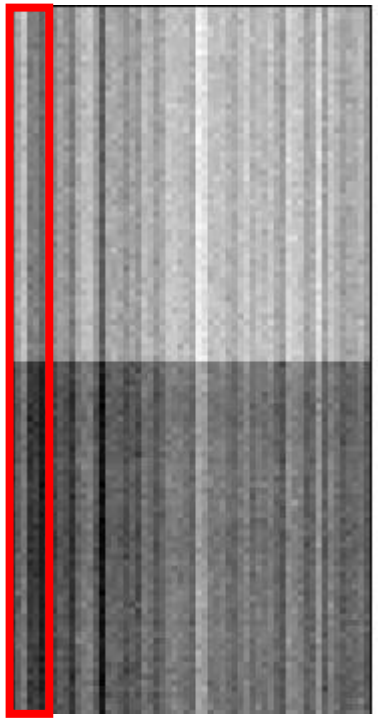
Pixel Testing – 3T

3T Pixels

- Pixel targeting radiation hardened designs:
  - Gated diode [7,8], large transistors
  - Leads to low conversion gain

- Use techniques from previous slides to reduce noise in spite of low conversion gain





Additional Techniques

- Off-chip CDS
  - Read reset level, then signal level one frame later

- Row Noise Correction
  - Use dark pixels at row edges to measure row noise, then subtract from image

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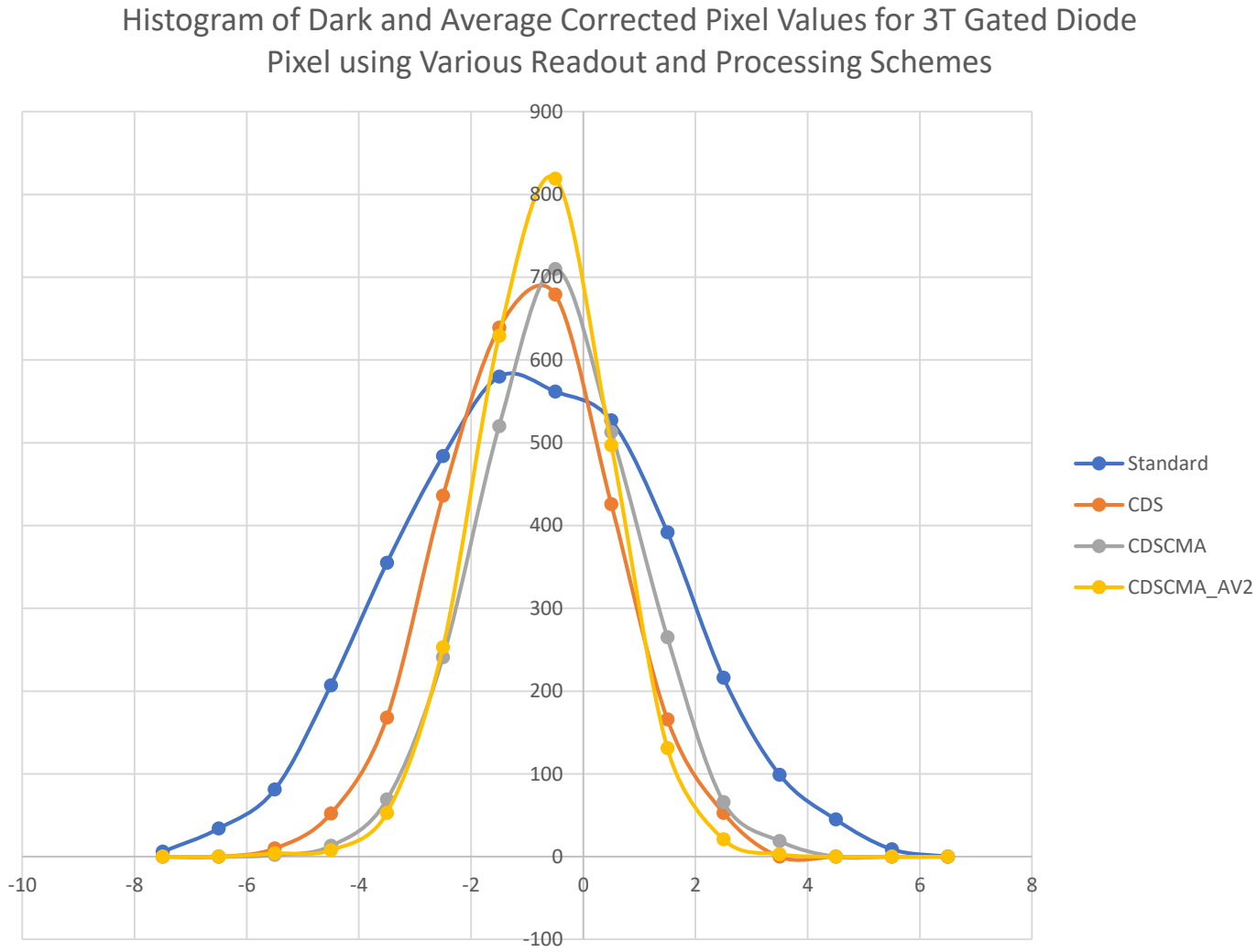
Pixel Testing – 3T

Noise Improvement

- Standard readout – 42e-
- Off-chip CDS – 38.7e-
- Off-chip CDS plus row noise correction – 36.2e-
- 2 sample averaging – 30.7e-
- 27% improvement. Also c.f. 30e- noise at room temp with similar designs – 35e-[9], 80e-[10]



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Conclusions

Motivation

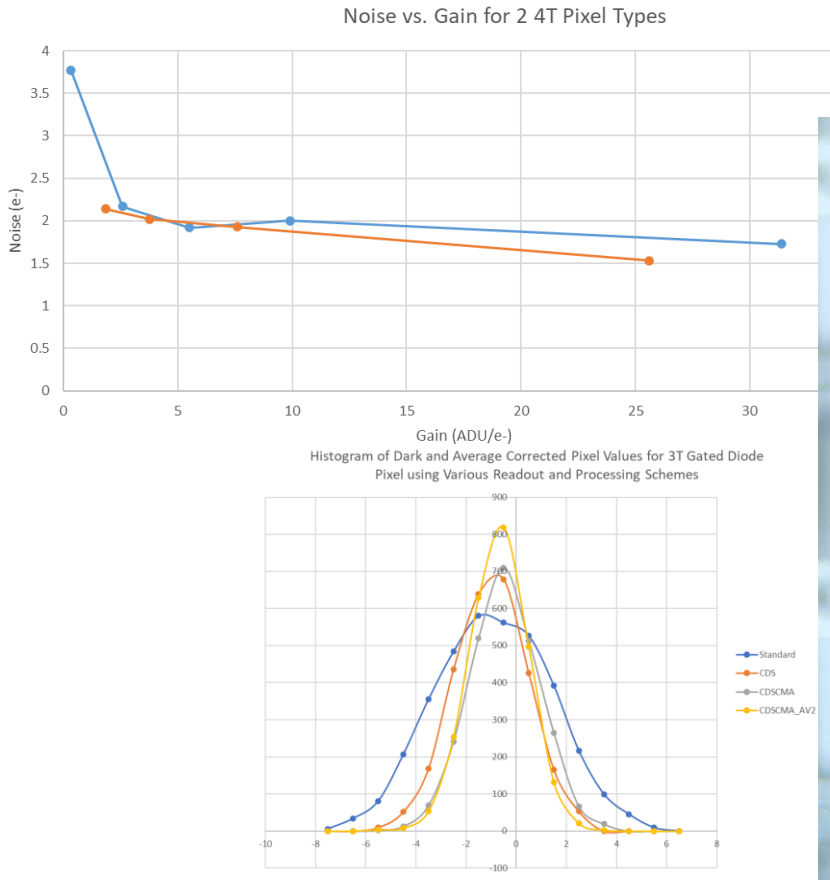
- Goal is to develop the circuit blocks for low noise, high speed future sensors
- Will help to de-risk future projects

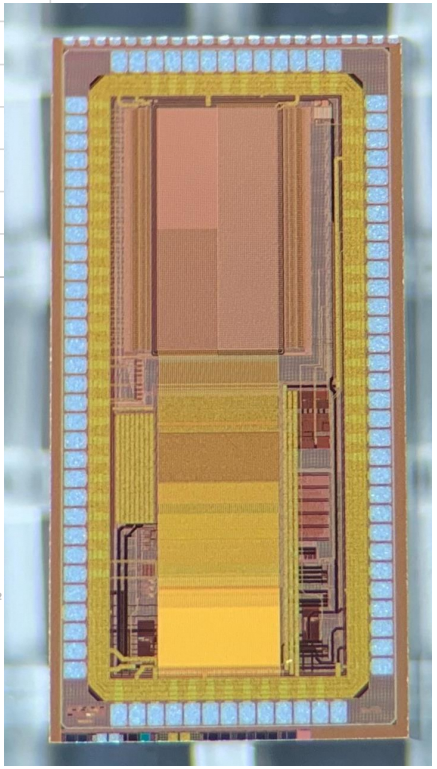
Circuit Blocks

- Sigma-Delta ADC: 12 bit, 322uV noise >1MSPS, 15um pitch
- Programmable Gain Amplifier: Gains 1-128, IR noise <150uV
- Averaging Stage
- Multiple pixel types, including radiation hardened design

Noise Performance

- 1.5e- for highest gain pixel in best performing configuration
- 27% improvement in noise of lower conversion gain pixel





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Extra Slides

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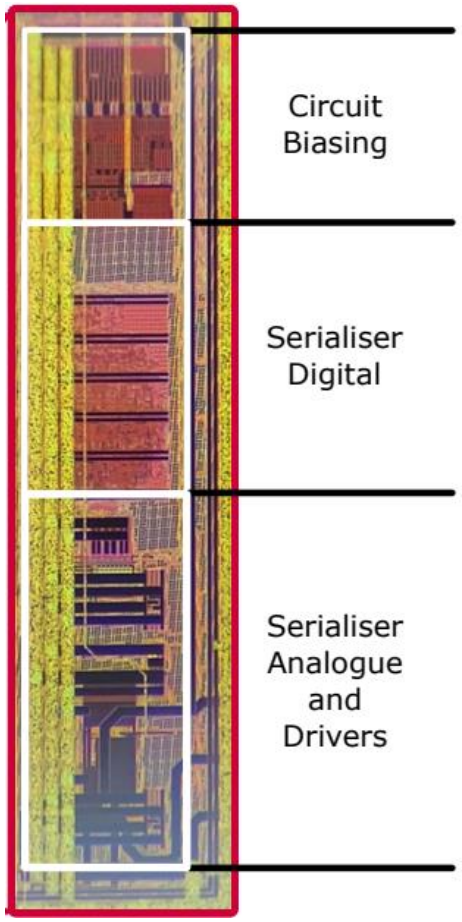
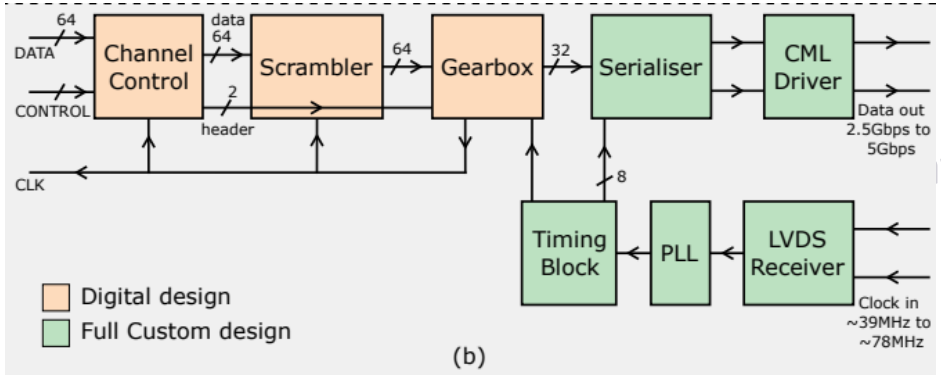
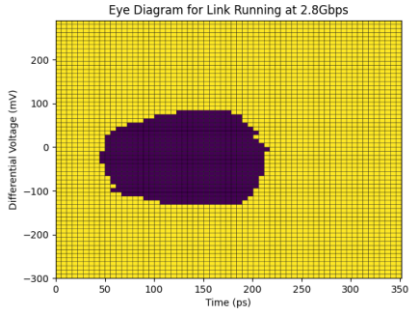
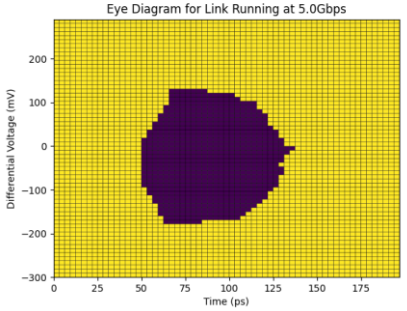
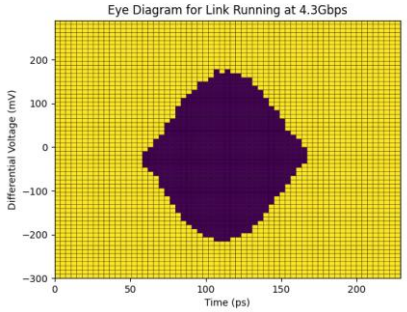
5Gbps Serialiser



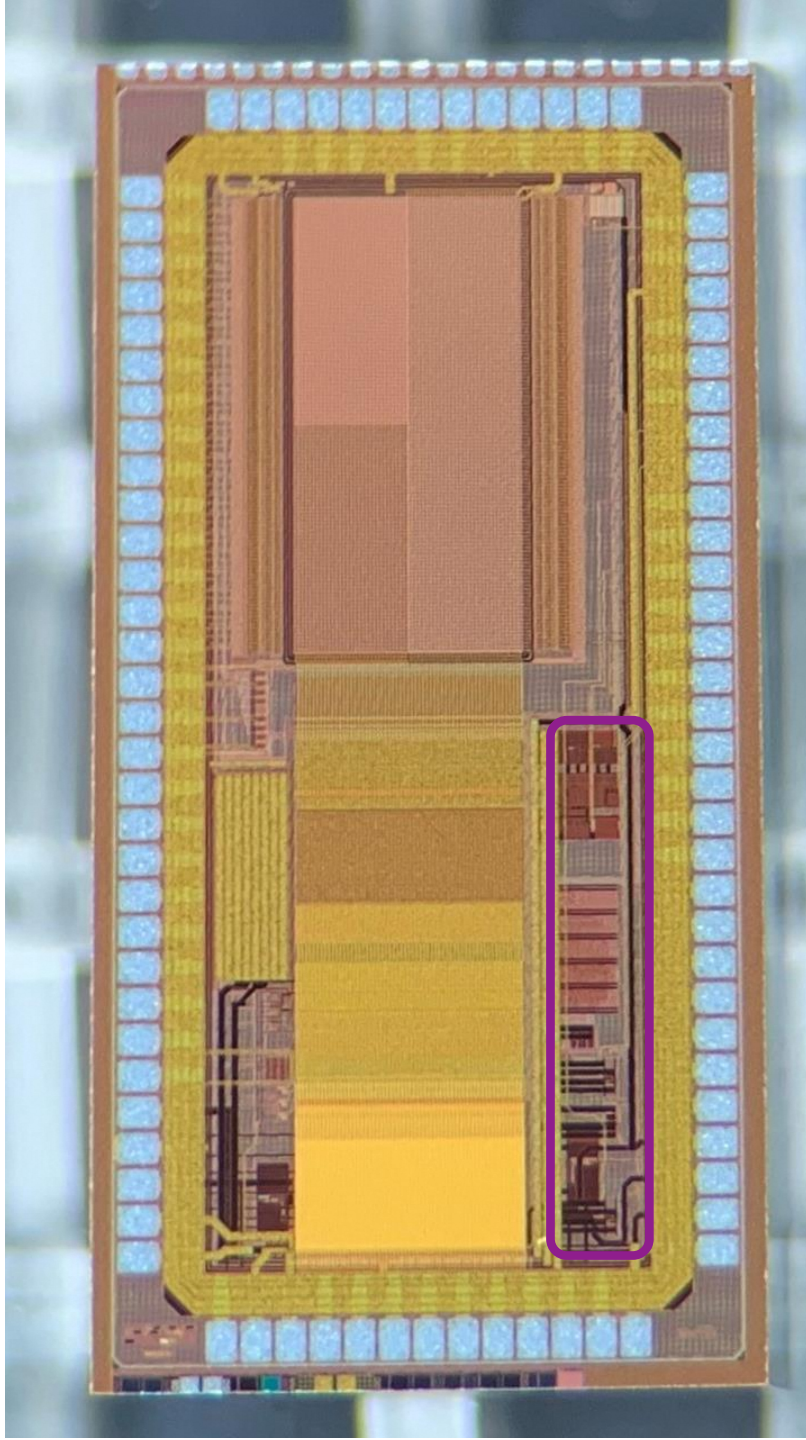








5Gbps Serialiser



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