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# Development of Low Noise Pixels and Readout Architectures for Scientific Applications in a 180nm CMOS Image Sensor Process

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## Development of Low Noise Pixels and Readout Architectures for Scientific Applications in a 180nm CMOS Image Sensor Process

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Progress in the performance of CMOS Image Sensors (CIS) in recent years has been extremely rapid, especially in the area of low noise, where values below  $1e^-$  have been reported [1] [2] and are even commercially available [3], allowing new science and improved performance in many fields.

However, there are also areas of scientific imaging (electron microscopy, X-ray imaging, proton therapy, FEL and synchrotron detectors) where low noise is required alongside other performance parameters such as radiation hardness, high dynamic range, or high frame rate. Achieving this performance means further developing low noise pixels and circuits to include additional features. This requires not just improved pixel performance, but also advanced readout circuitry.

With these goals in mind, we present PRECISE, a test structure in a 180nm CMOS Image Sensor process, which contains several flavours of 3T and 4T pixels targeting different application areas. Some are optimised for low noise, others implement radiation hardened architectures, and some show high dynamic range performance. The chip also implements a capacitive Programmable Gain Amplifier (PGA), a Sigma-Delta ADC and implements on-chip CDS. These features are crucial for the integration of the low noise pixels in real systems. The goal of the chip is to demonstrate the performance of the various “building blocks” needed for a larger scientific detector. Suitable blocks can then be combined with the desired pixel type for best performance.

With this device, we have so far demonstrated noise as low as  $2e^-$  at room temperature with a 1 $\mu$ s ADC conversion time (for 12 bits). We will present these results alongside results from the pixels which exhibit other functionalities, and discuss the performance of the ADC and PGA blocks. To complete the necessary set of “building blocks”, the chip implements a separate 5 Gbps serialiser, whose performance will also be briefly discussed.

[1] A. Boukhayma, A. Peizerat and C. Enz, “A Sub-0.5 Electron Read Noise VGA Image Sensor in a Standard CMOS Process”, IEEE Journal of Solid-State Circuits, vol. 51, no. 9, pp. 2180-2191, 2016. Available: 10.1109/jssc.2016.2579643.

[2] J. Ma and E. Fossum, “Quanta Image Sensor Jot With Sub 0.3e<sup>-</sup> r.m.s. Read Noise and Photon Counting Capability”, IEEE Electron Device Letters, vol. 36, no. 9, pp. 926-928, 2015. Available: 10.1109/led.2015.2456067.

[3] Hamamatsu.com, 2022. [Online]. Available: <https://www.hamamatsu.com/eu/en/product/cameras/qcmos-cameras.html>. [Accessed: 30- Mar- 2022].

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