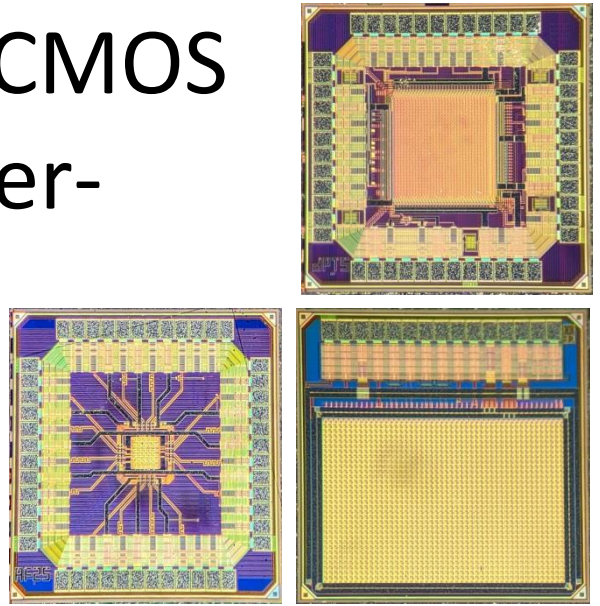
Exploration of the TPSCo 65 nm CMOS imaging process for building wafer-scale, thin and flexible detection layers for the ALICE ITS3

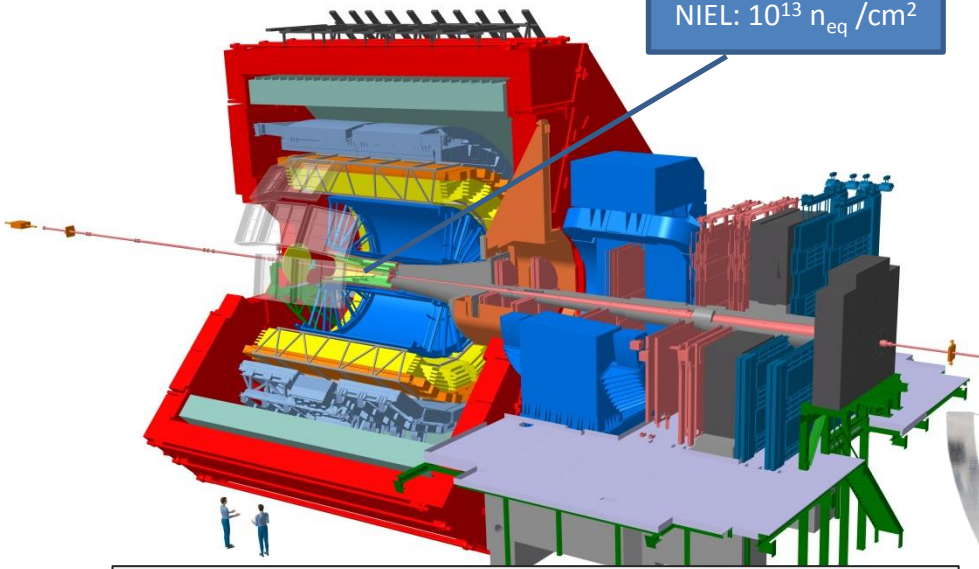


Serhiy Senyukov (IPHC CNRS-IN2P3) for the ALICE ITS project

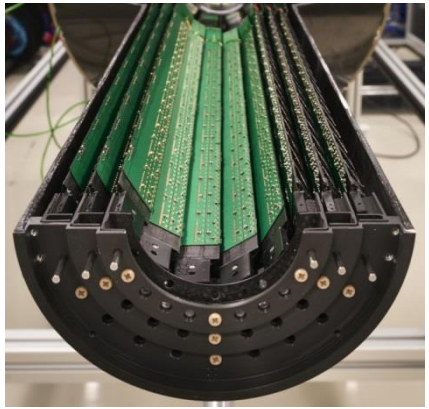
Outline

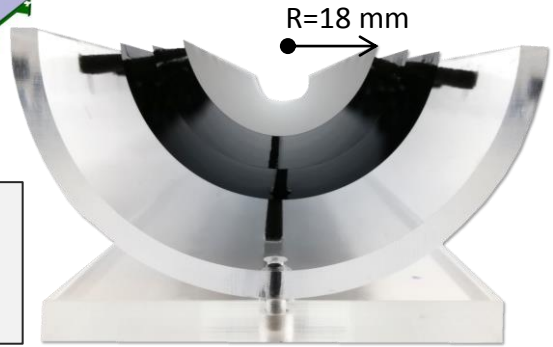
- ALICE detector LS3 upgrade: from ITS2 to ITS3
- Small bent sensors
- Technology choice for larger sensors
- First submission in TPSCo 65 nm CIS process
- Overview of test results
- Summary and next steps

ALICE detector LS3 upgrade: ITS2 → ITS3



ALICE – general purpose detector at LHC:
- Tracking (100 MeV/c – 100 GeV/c)
- Particle identification: π, K, p, e (0.1 – 50 GeV/c)



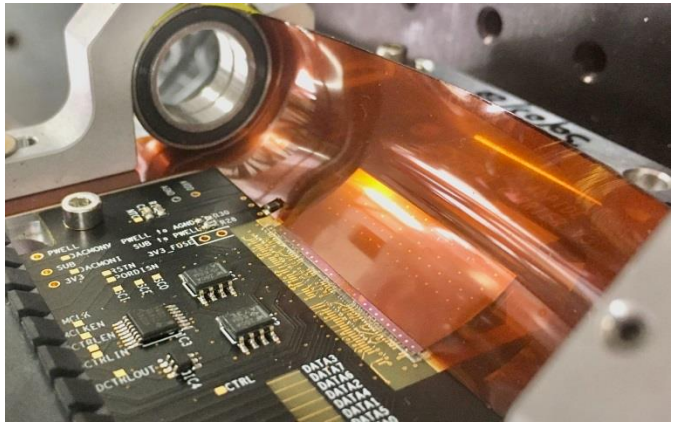


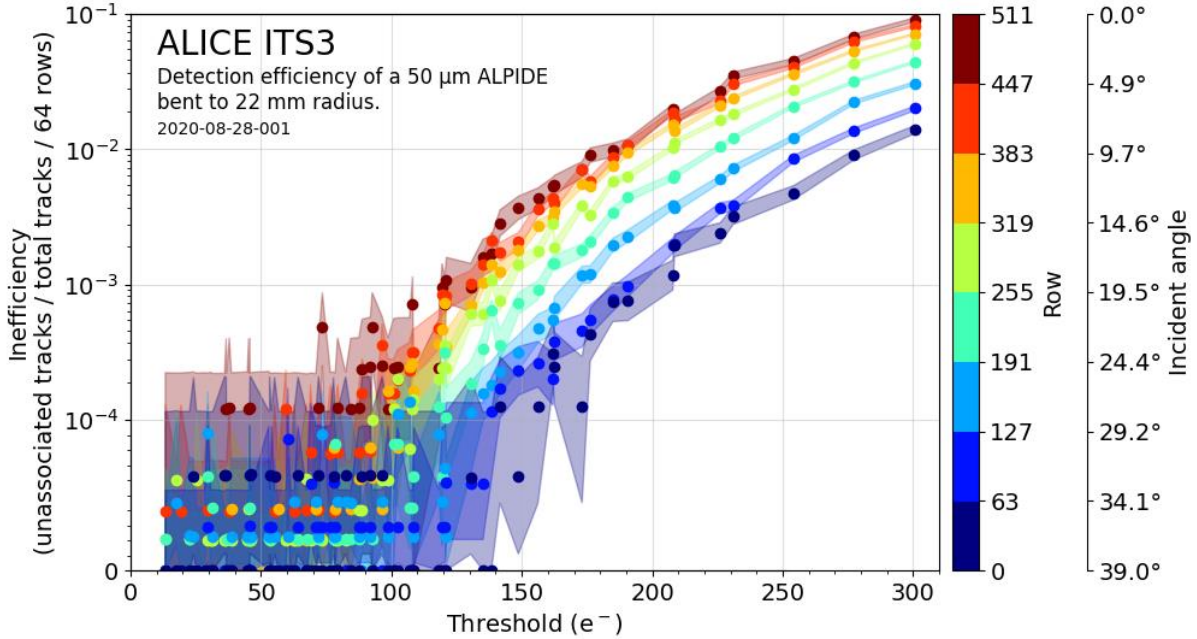
ITS2: (S.Beolé's talk)
- 7 layers of MAPS
- TJ 180 nm CMOS
- 12.5 Giga pixels
- Pixel size: 27×29 μm^2
- Water cooling
- **0.3 % X_0 / inner layer**

ITS3:
- 4 outer layers of ITS2
- 3 new fully cylindrical inner layers
  - Sensor size up to 27×9 cm
  - Thickness 30-40 μm
  - No FPCs
  - Air cooling in active area
- **0.05 % X_0 / inner layer**

Small bent sensors work well

50 µm thick ITS2 chip (ALPIDE) bent to 22 mm showed excellent efficiency in the beam test in 2020

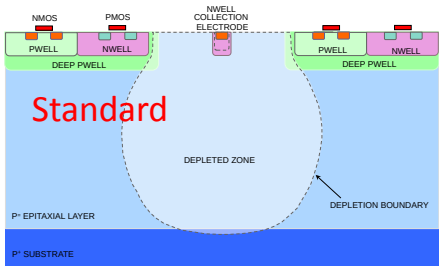


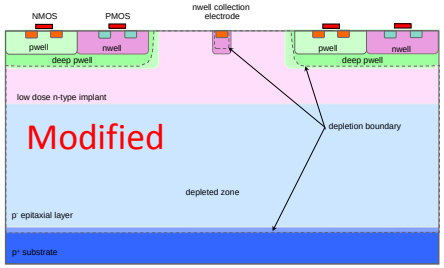


https://doi.org/10.1016/j.nima.2021.166280

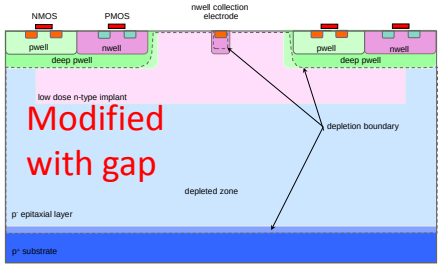
It’s time to go bigger (in area): TPSCo 65 nm CMOS IS

- Continuation of the TowerJazz 180 nm (ITS2)
- Provides 2D stitching
- Available on 300 mm wafers → 27×9 cm^2 final sensor
- 65 nm → lower power consumption
- 7 metal layers
- Process modifications for full depletion:
  - Standard (no modifications)
  - Modified (low dose n-type implant)
  - Modified with gap (low dose n-type implant with gaps)
- 4 process splits:
  1. **Default**
  2. First intermediate optimization
  3. Second intermediate optimization
  4. **Fully optimized process**





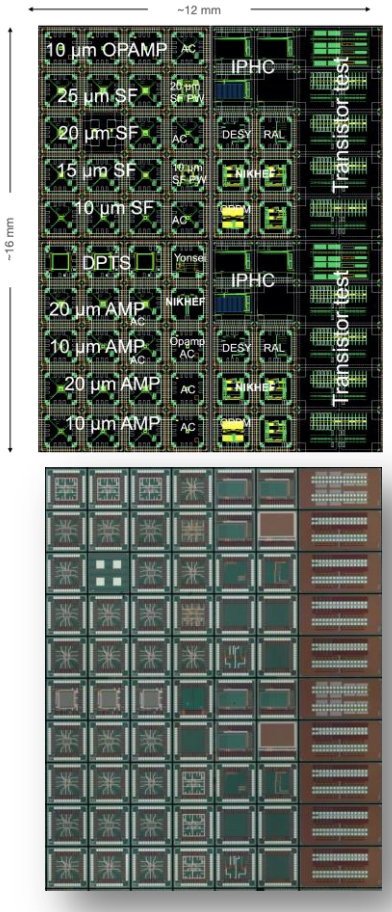
https://doi.org/10.1016/j.nima.2017.07.046



https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

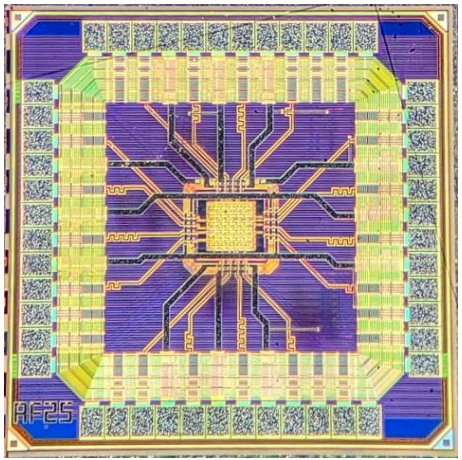
First test submission: MLR1

- Submitted in December 2020
- Main goals:
  - Learn technology features
  - Characterize charge collection
  - Validate radiation tolerance
- Each reticle (12×16 mm^2):
  - 10 transistor test structures (3×1.5 mm^2)
  - 60 chips (1.5×1.5 mm^2)
    - Analogue blocks
    - Digital blocks
    - **Pixel prototype chips: APTS, CE65, DPTS**
- Testing since September 2021



APTS: Analogue Pixel Test Structure

- 6×6 pixel matrix
- Direct analogue readout of central 4×4 submatrix
- Two types of output drivers:
  - Traditional source follower (APTS-SF)
  - Very fast OpAmp (APTS-OA)
- AC/DC coupling
- 4 pitches: 10, 15, 20, 25 µm
- 3 process variations
- Presented results with ^{55}Fe source

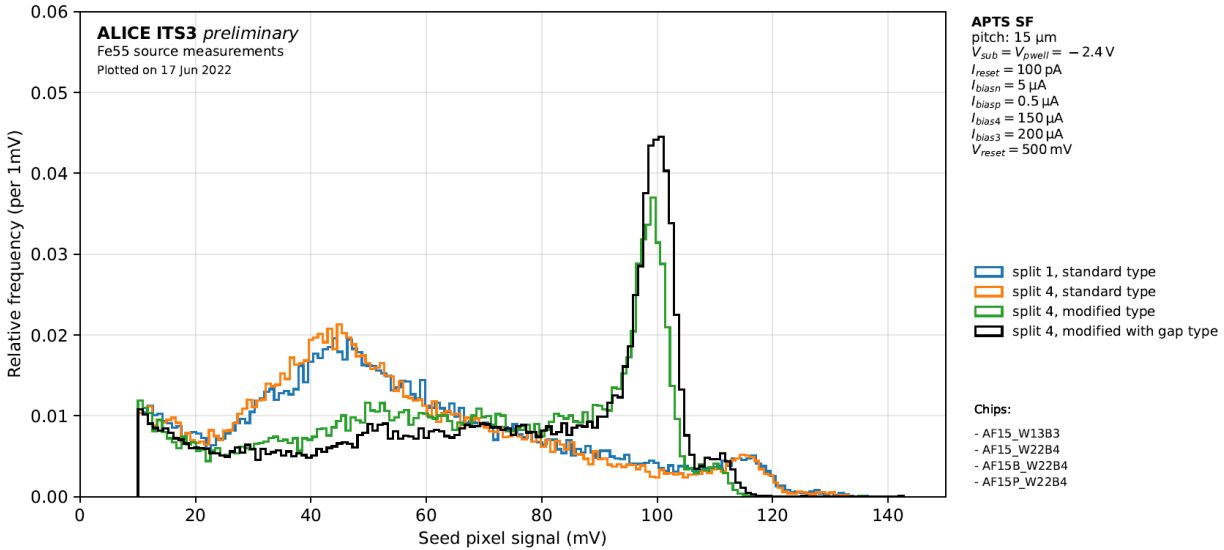


1.5×1.5 mm^2

APTS-SF:
Process modification reduces charge sharing

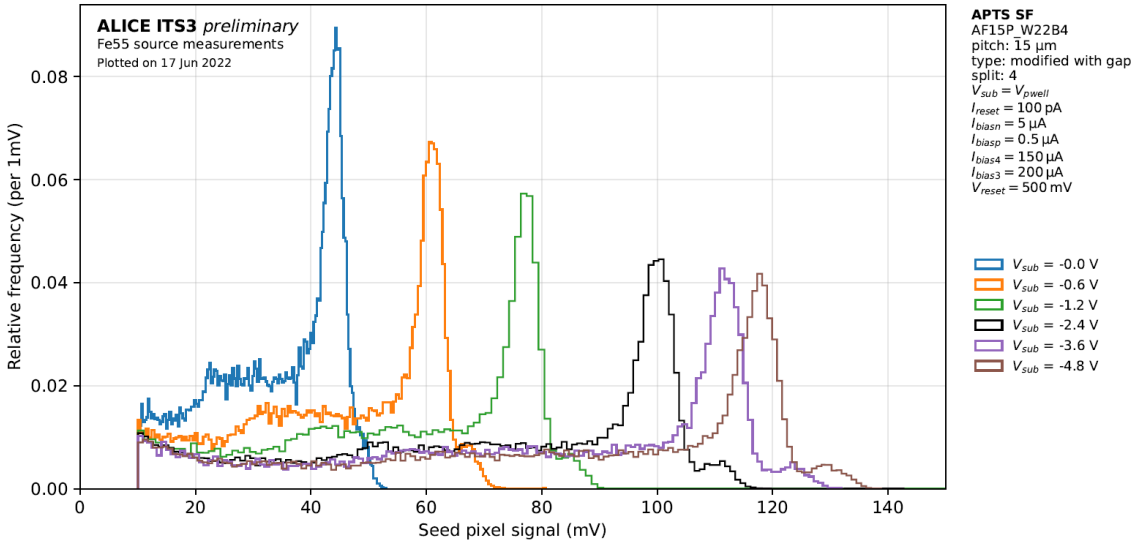
- In standard process seed pixel takes ~50% of charge
- In modified process most of the charge is collected in one pixel

Effect on efficiency and spatial resolution to be verified at beam test



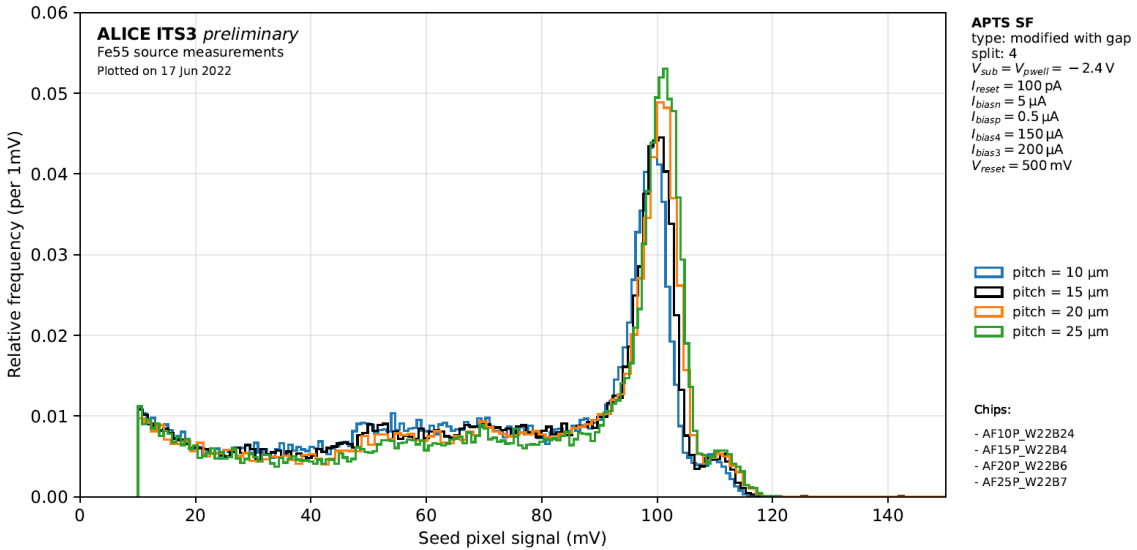
APTS-SF:
Substrate bias amplifies the signal

- Substrate bias lowers the node capacitance to as low as 2.2 fF
- Signal amplitude increases



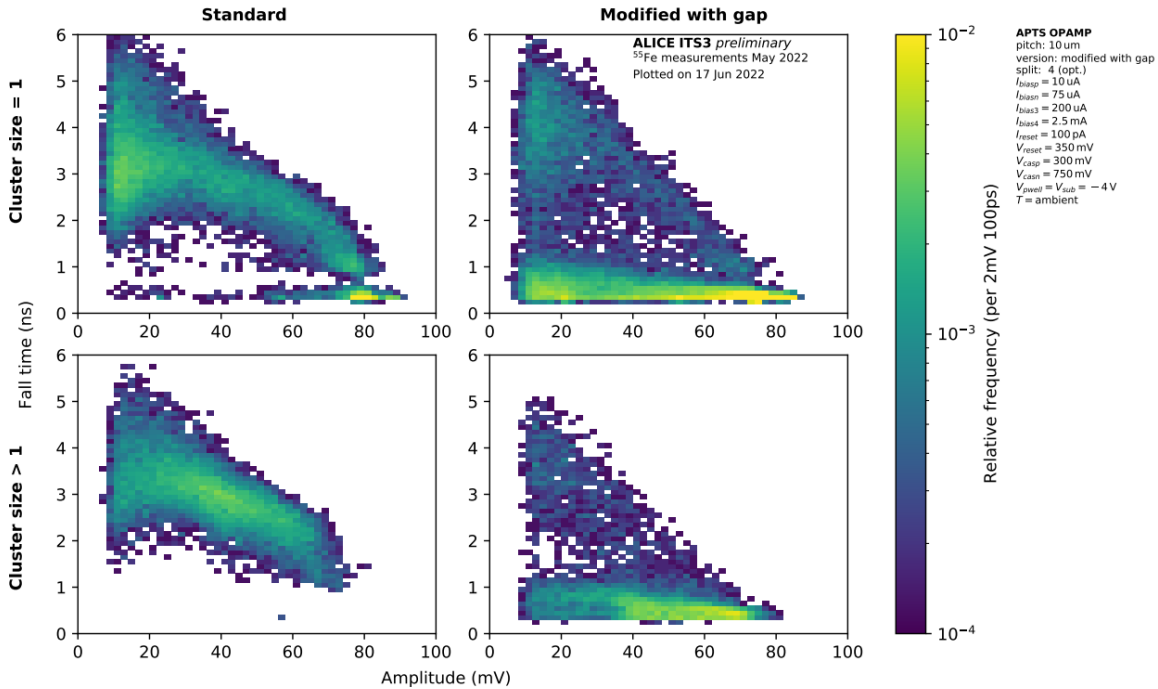
APTS-SF:
Charge collection vs. pixel pitch

- Charge collection efficiency doesn't seem to depend on pixel pitch
- Remarkable result to be confirmed by beam test
- If efficiency stays high at larger pitches -> way to decrease the power consumption



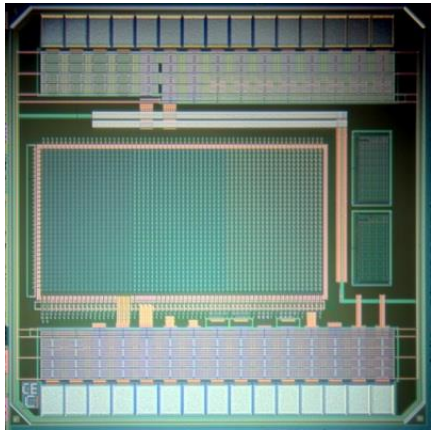
APTS-OA:
Process modification reduces charge collection time

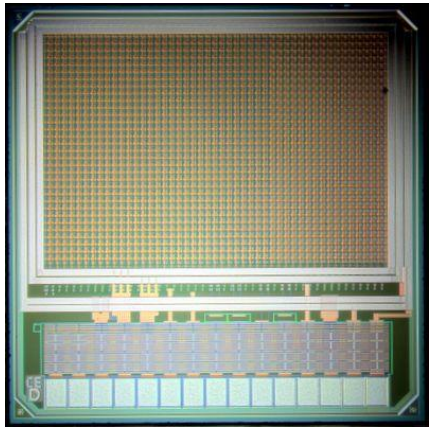
- Fast readout allows to estimate the charge collection time via signal fall time
- In modified process the charge is collected faster



CE65:
Circuit Exploratoire 65 nm

- 2 matrix sizes
  - 64×32 with 15 µm pitch
  - 48×32 matrix with 25 µm pitch
- Rolling shutter readout (50 µs integration time)
- 3 in-pixel architectures:
  - AC-coupled amplifier
  - DC-coupled amplifier
  - Source follower
- 4 chip variants:
  - **Standard process 15 µm pitch**
  - Modified process 15 µm pitch
  - **Modified process with gaps 15 µm pitch**
  - Standard process 25 µm pitch
- Presented results from CERN PS beam test

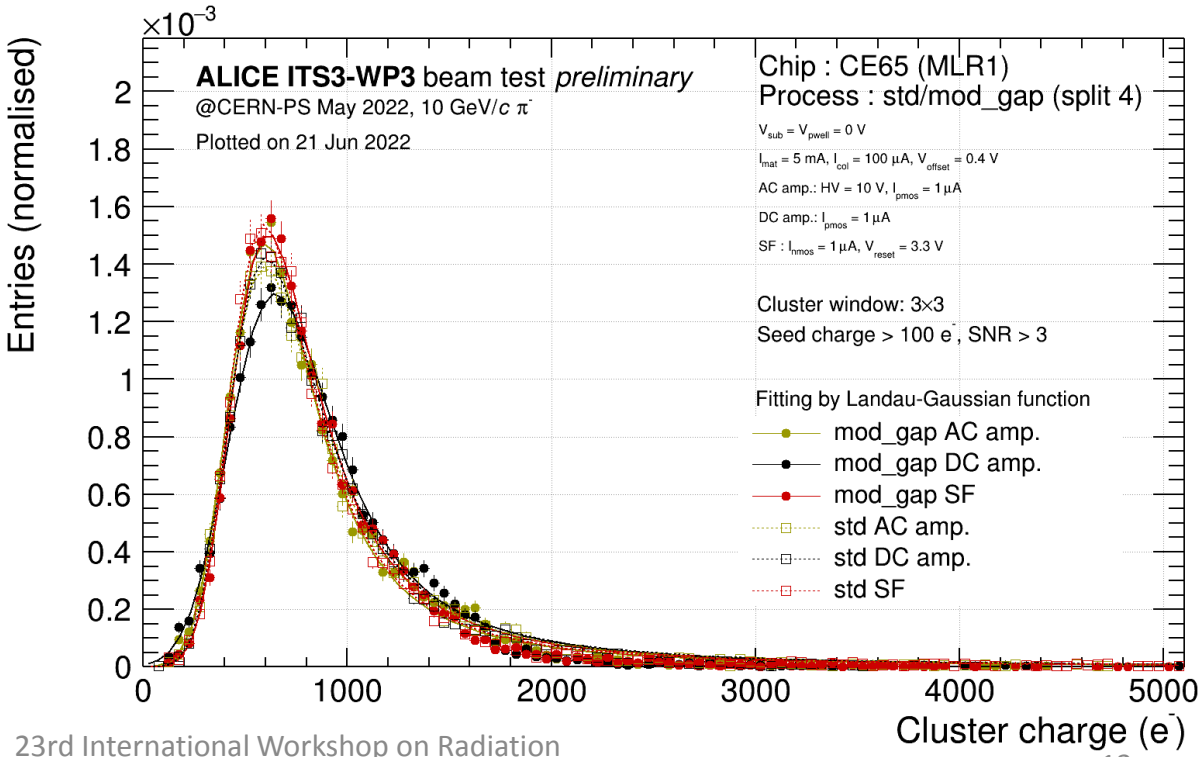




1.5×1.5 mm^2

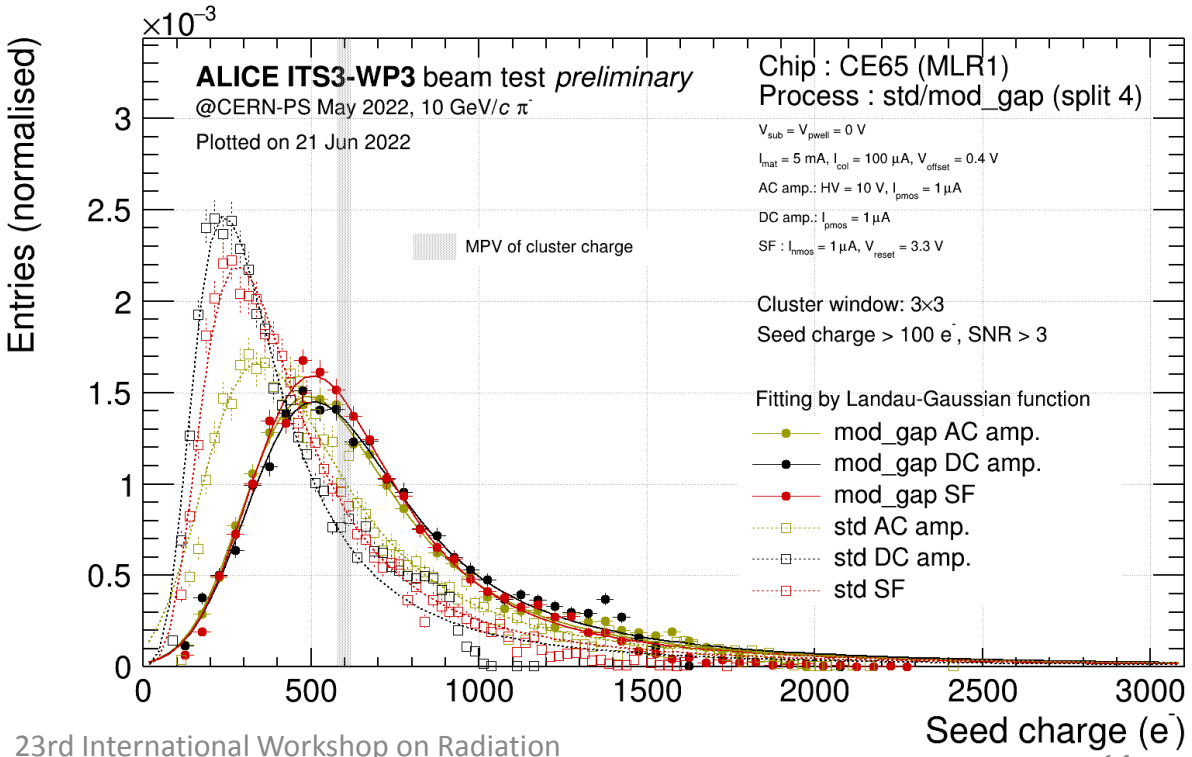
CE65: Cluster charge doesn't depend on process modification and pixel architecture

- All submatrices in standard and modified processes collect the same total charge
- Charge distribution parameters roughly correspond to effective epitaxial layer of 11 µm
  (via H. Bichsel
  https://doi.org/10.1103/RevModPhys.60.663)



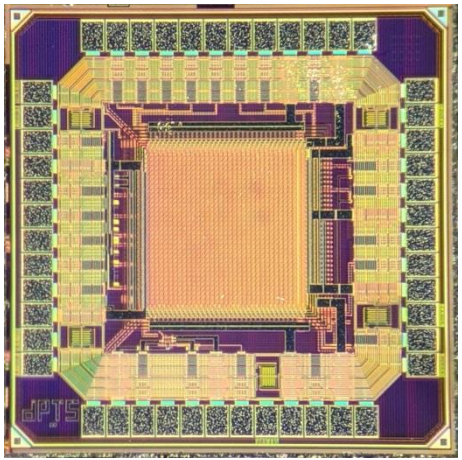
CE65: Process modification reduces charge sharing

- Effect observed in APTS with ^{55}Fe sources confirmed at beam test
- In modified process all charge is mostly collected by single pixel



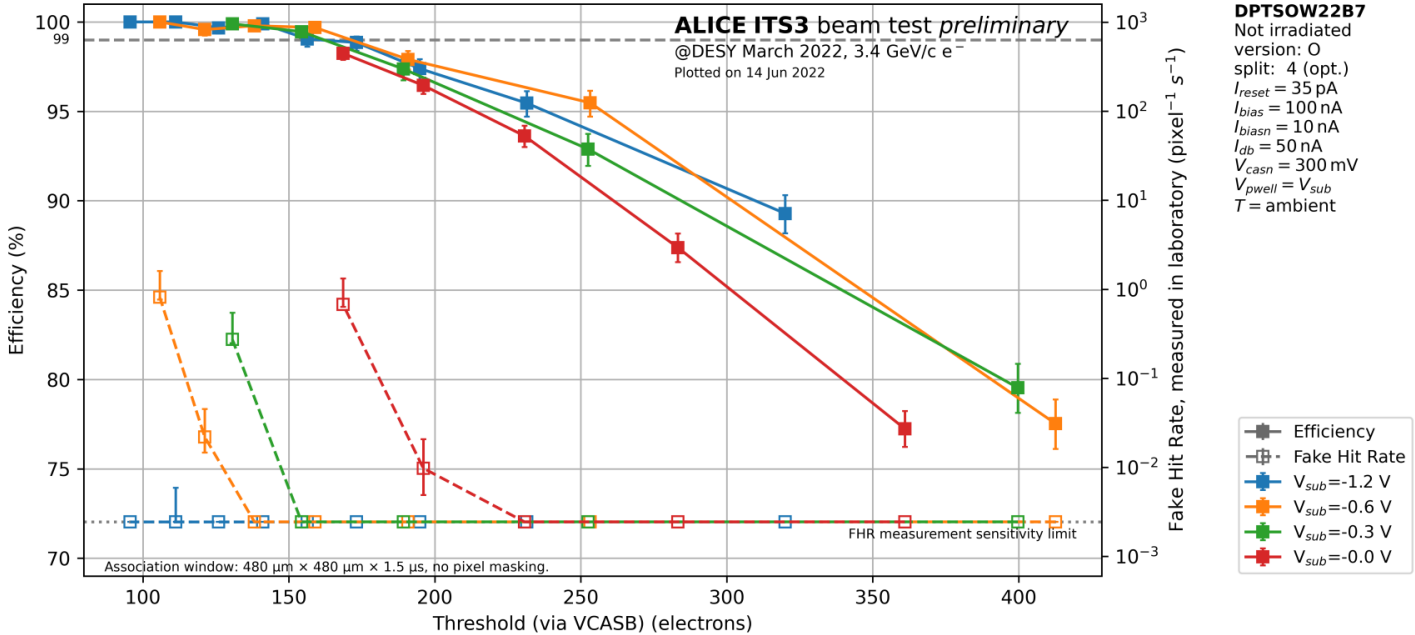
DPTS: Digital Pixel Test Structure

- 32×32 pixel matrix
- Asynchronous digital readout
- Time-over-Threshold information
- Pitch: 15×15 μm^2
- Only “modified with gap” process modification
- Tunable Power vs Time resolution via pixel frontend parameters
- Presented results from DESY and PS beam tests

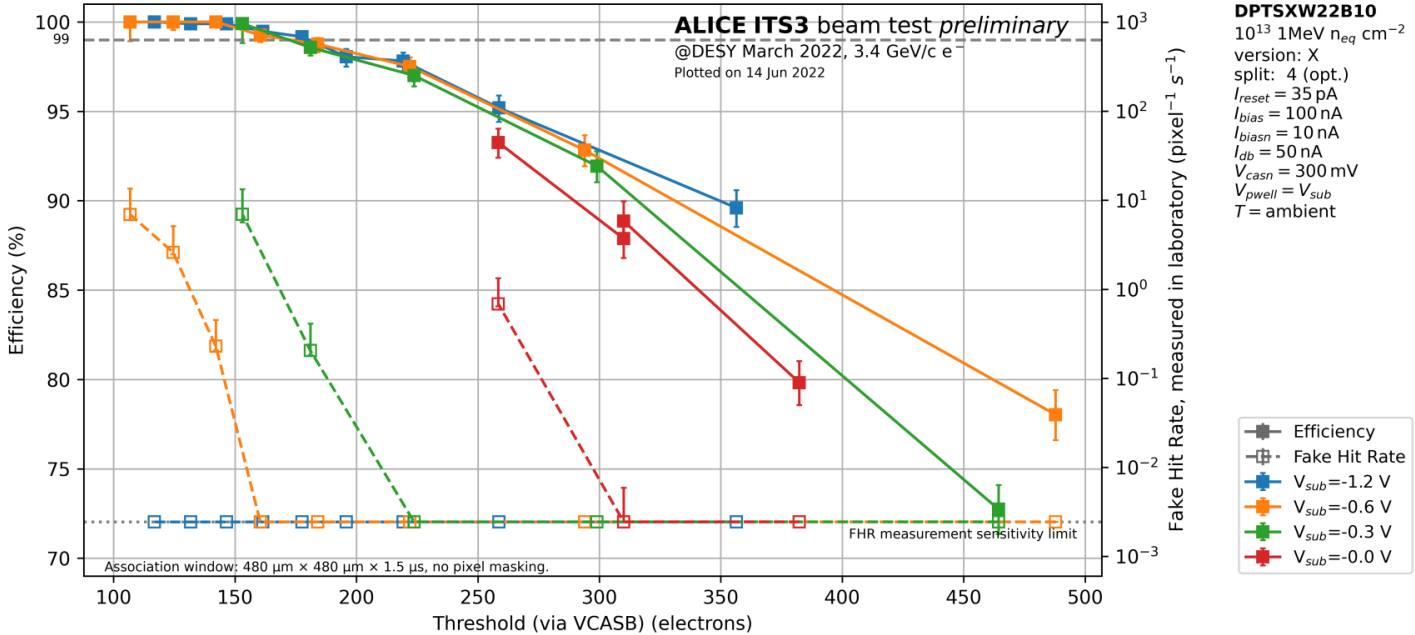


1.5×1.5 mm^2

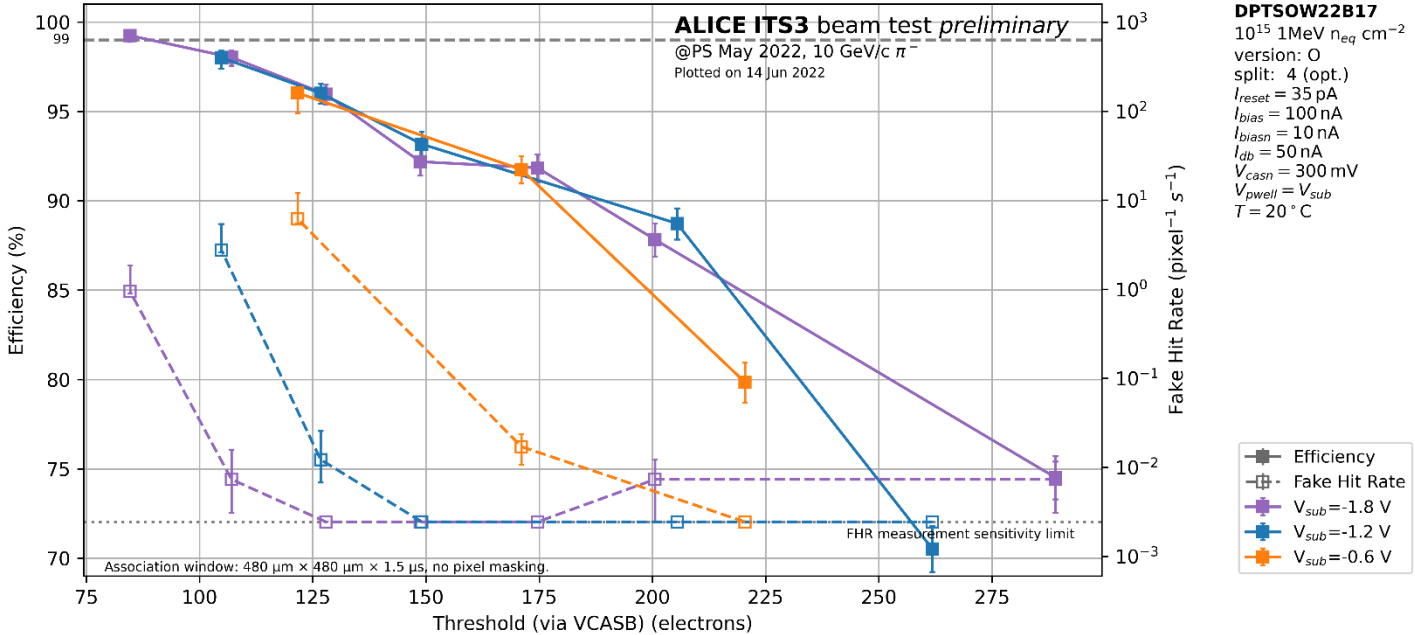
Non irradiated DPTS:
Excellent efficiency and low fake hit rate



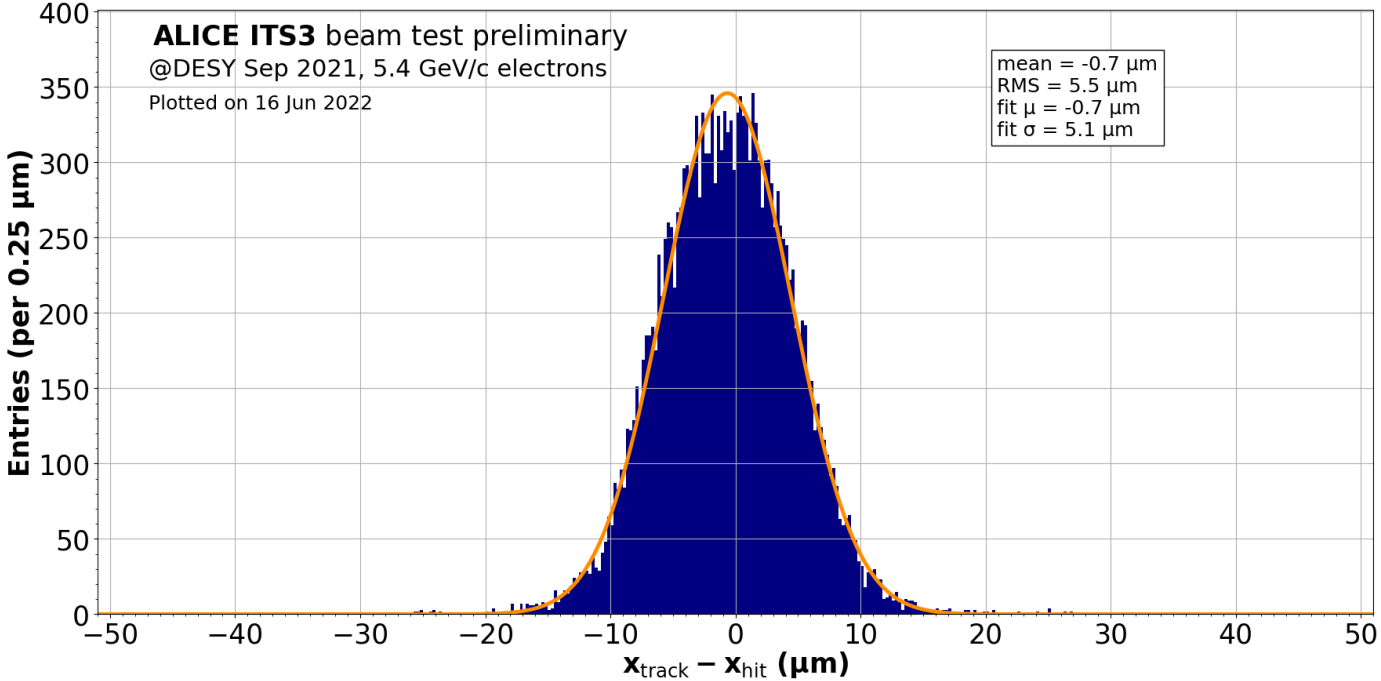
Irradiated DPTS (10^{13} n_{eq}): Larger fake hit rate, but has margin



Irradiated DPTS (10^{15} n_{eq}): Efficient at 20 °C with limited fake hit rate

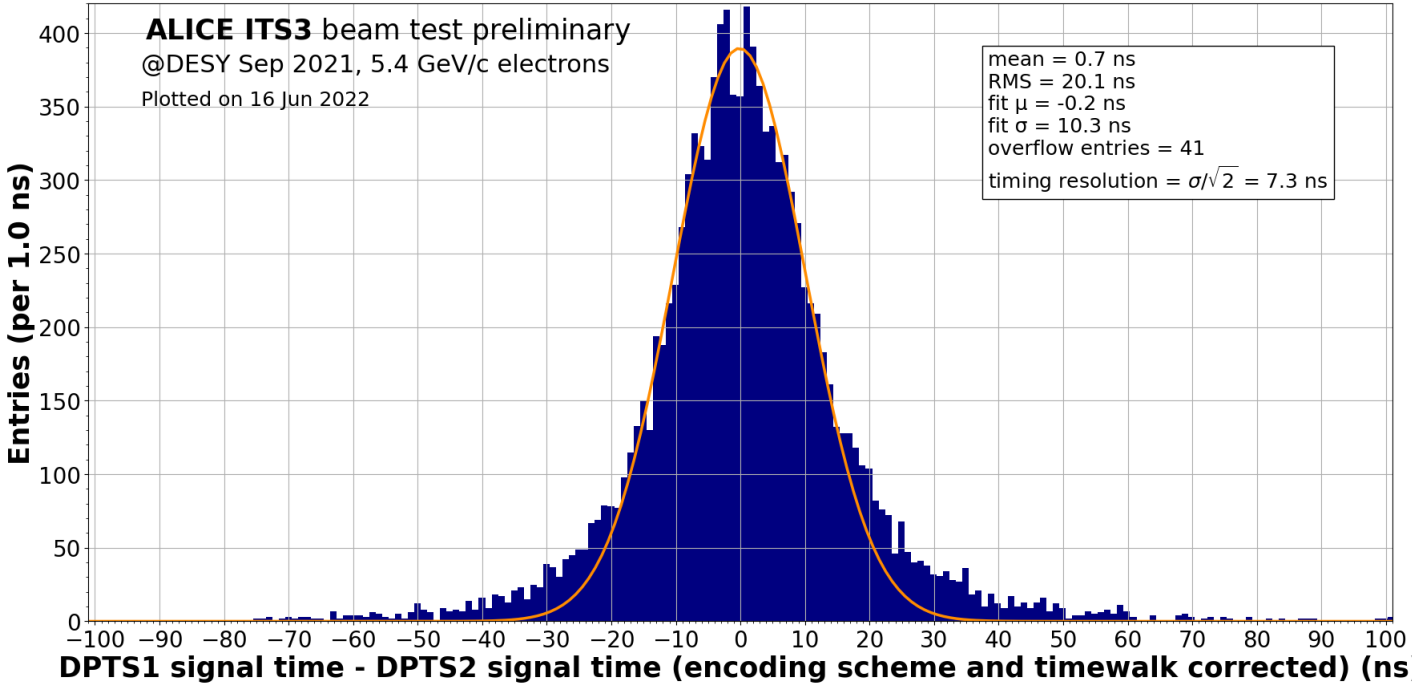


DPTS: Spatial resolution ~5 µm



DPTSOW22B3 (not irradiated)
version: O
split: 4 (opt.)
$I_{reset} = 10\,pA$
$I_{bias} = 100\,nA$
$I_{biasn} = 10\,nA$
$I_{db} = 100\,nA$
$V_{casn} = 300\,mV$
$V_{casb} = 250\,mV$
$V_{pwell} = V_{sub} = -1.2V$

DPTS: Temporal resolution ~7 ns



DPTSOW22B3 (not irradiated)
version: O
split: 4 (opt.)
$I_{reset} = 10\,pA$
$I_{bias} = 100\,nA$
$I_{biasn} = 10\,nA$
$I_{db} = 100\,nA$
$V_{casn} = 300\,mV$
$V_{casb} = 250\,mV$
$V_{pwell} = V_{sub} = -1.2V$

DPTSXW22B1 (not irradiated)
version: X
split: 4 (opt.)
$I_{reset} = 10\,pA$
$I_{bias} = 100\,nA$
$I_{biasn} = 10\,nA$
$I_{db} = 100\,nA$
$V_{casn} = 300\,mV$
$V_{casb} = 280\,mV$
$V_{pwell} = V_{sub} = -1.2V$

Summary

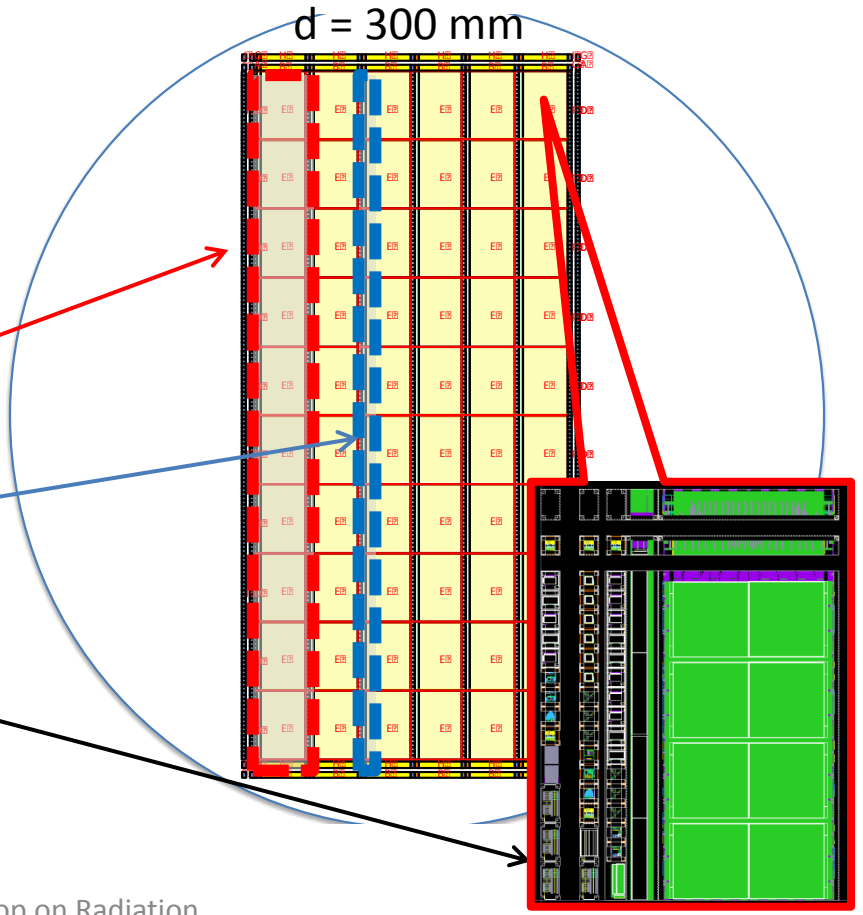
- TPSCo 65 nm CMOS IS process is being evaluated for future ALICE ITS3
- Chips from MLR1 submission yield promising results on technology capabilities:
  - Efficiency > 99% at FHR < 1 hit/second/1024 pixels
  - Spatial resolution ~5 µm
  - Temporal resolution ~7 ns
  - Withstands NIEL irradiation of up to 10^{15} n_{eq}/cm^2
    - Efficiency ~99% at FHR 1 hit/second/pixel at 20 °C

Next step: stitching

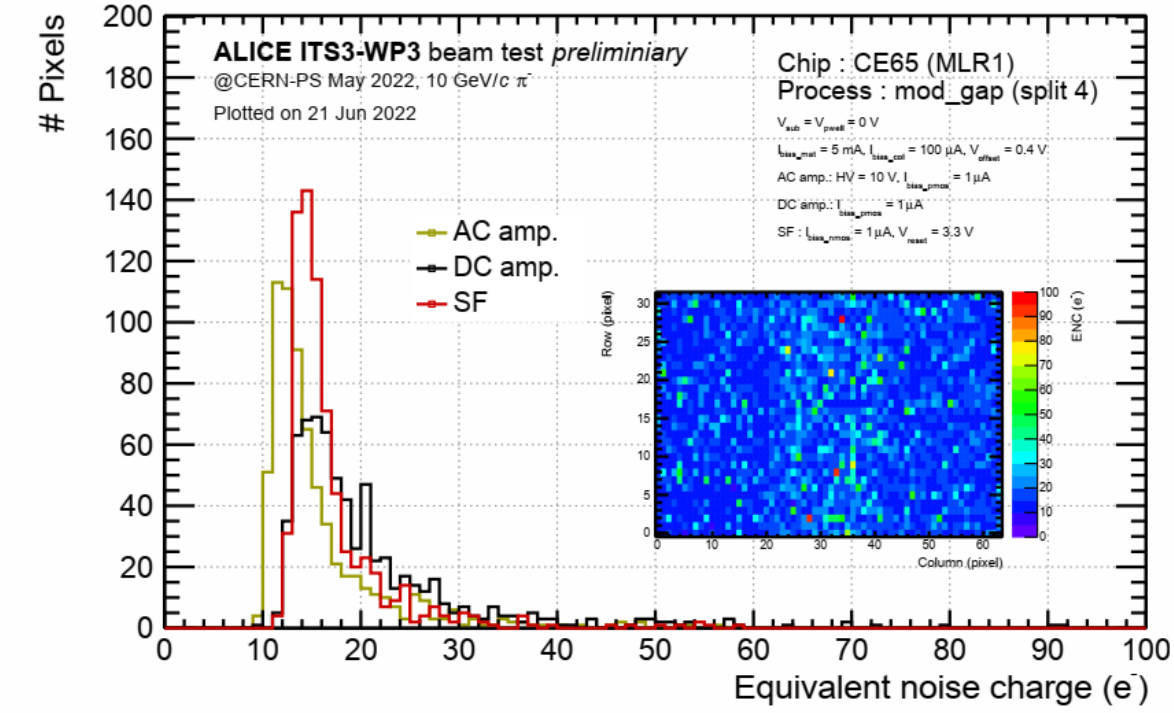
First run with 2 stitched sensors in preparation:

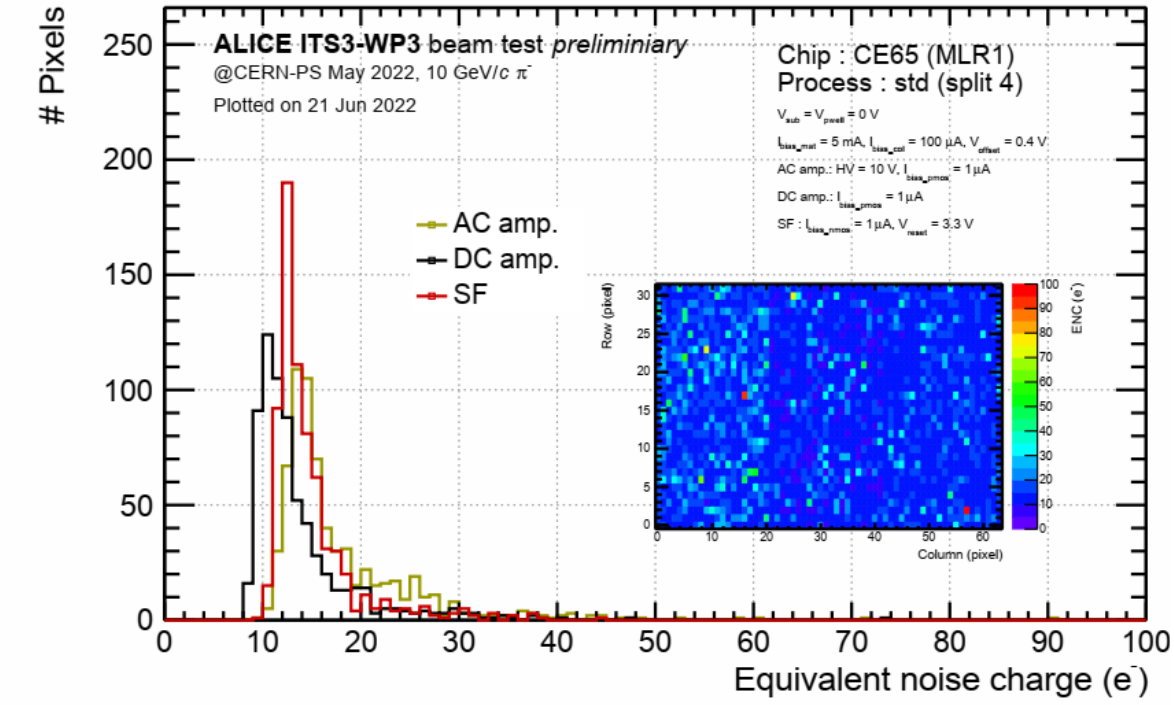
- MOSS
  260×14 mm² 6.72 Mpixels
- MOST
  260×2.5 mm² 900 kPixels
- + multiple small chips for further technology exploration

More news at IWoRiD 2023?




ALICE


ALICE ITS3-WP3 beam test preliminiary
@CERN-PS May 2022, 10 GeV/c π⁻
Plotted on 21 Jun 2022
Chip : CE65 (MLR1)
Process : mod_gap (split 4)
V_sub = V_pwell = 0 V
I_bias_mat = 5 mA, I_bias_col = 100 µA, V_offset = 0.4 V
AC amp.: HV = 10 V, I_bias_pmos = 1 µA
DC amp.: I_bias_pmos = 1 µA
SF : I_bias_nmos = 1 µA, V_reset = 3.3 V
AC amp.
DC amp.
SF
Pixels
Equivalent noise charge (e⁻)
Row (pixel)
Column (pixel)
ENC (e⁻)


ALICE ITS3-WP3 beam test preliminiary
@CERN-PS May 2022, 10 GeV/c π⁻
Plotted on 21 Jun 2022
Chip : CE65 (MLR1)
Process : std (split 4)
V_sub = V_pwell = 0 V
I_bias_mat = 5 mA, I_bias_col = 100 µA, V_offset = 0.4 V
AC amp.: HV = 10 V, I_bias_pmos = 1 µA
DC amp.: I_bias_pmos = 1 µA
SF : I_bias_nmos = 1 µA, V_reset = 3.3 V
AC amp.
DC amp.
SF
Pixels
Equivalent noise charge (e⁻)
Row (pixel)
Column (pixel)
ENC (e⁻)