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Exploration of the TPSCo 65 nm CMOS imaging process for building wafer-scale, thin and flexible detection layers for the ALICE Inner Tracking System upgrade (ITS3)

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The ALICE experiment is planning next upgrade of the Inner Tracking System (ITS3) during the LHC Long Shutdown 3 (LS3) in 2025 –2028. The main aim of this upgrade is to reduce material budget of the three innermost layers from 0.3% X_0 to 0.05% X_0 per layer. Such a significant improvement is within the reach if segmented layers of the current detector would be replaced with truly cylindrical layers made of wafer-scale, thin and flexible stitched CMOS pixel sensors.

The 65 nm CMOS imaging process by Tower Partners Semiconductor Company (TPSCo) provides stitching of 300 mm wafers allowing to produce CMOS pixel sensors as large as ˜27×9 cm2. After thinning to 50 µm or below each sensor can be bent to a radius as low as 18 mm to form a half of the cylindrical detection layer. Therefore, six stitched sensors are sufficient to construct three new innermost layers made essentially of only thin silicon.

In order to start the exploration of the TPSCo 65 nm CMOS process the first test production run (MLR1) was submitted in 2021. Among multiple test structures and prototype circuits included in MLR1 the following three sensor types were specifically designed to evaluate the charged particle detection performance of the technology. Analogue Pixel Test Structure (APTS) chips are the simplest ones: they feature 4×4 pixel matrix with fast analogue readout of each pixel individually. CE65 chips have larger matrix of 64×32 pixels with rolling shutter analogue readout. Finally, Digital Pixel Test Structure (DPTS) chips have 32×32 pixel matrix with one channel digital readout.

The present contribution will cover the results of performance measurements of APTS, CE65 and DPTS chips obtained in the laboratory and with particle beams in 2021 and 2022. Finally, the outlook for the next submissions towards the final sensor will be given.

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