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Development of CoRDIA: An Imaging Detector for next-generation Synchrotron Rings and Free Electron Lasers

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Currently the landscape of Synchrotron Radiation sources is experiencing a major change by planned or ongoing machine upgrades: Most storage rings reach the diffraction limit, causing an expected increase in brilliance by about two orders of magnitude. Most FEL sources increase repetition rates to around 100kHz. This also holds true for the European XFEL, where a change from the train mode (with 27kHz average rate) to CW operation at around 100kHz could be imaginable.

To fully exploit the increased performance of these sources, also imaging detectors need to be upgraded – from today's imagers at storage rings and low rate FELs, capable of a few-kHz continuous frame rate, to ≥100kHz. The ASICS of most imaging detectors for the European XFEL (like AGIPD or LPD) can cope with image recording at up to 4.5MHz, but lack the readout bandwidth required for continuous rates faster than ≈10kHz. Furthermore the pixel size of these detectors is severely compromised by their in-pixel memory, not needed for continuous operation. However, the new requirements of diffraction limited storage rings and upgraded FELs overlap enough to be catered by a common detector system:

CoRDIA, the Continuous Readout Digitising Imager Array, developed by a collaboration between DESY and Bonn University.
Design goals are continuous operation at ≥100kframe/s, single-photon sensitivity at 12keV or less, a dynamic range up to 10^4 photons at the same energy, and a pixel pitch of 100µm. Complete detector systems will be composed as an array of hybrid assemblies, consisting of several readout ASICs bump-bonded to a sensor. This ASIC will be compatible with different sensor materials and types:

- p-doped Silicon for the central (≈10keV) energy range,
- high-Z materials for higher energies, and
- LGAD sensors (with built-in amplification) for soft X-rays.

To achieve an (almost) dead time free operation, the ASIC implements a pipelined signal processing chain: While one image is digitised, the next one is integrated by the preamplifier, and the preceding one is read out. This readout is based on the principle of the GWT-CC solution developed by Nikhef for Timepix4.
Basic circuit blocks have been manufactured on 2 MPW chips in TSMC 65nm technology and are currently being tested:

- An adaptive-gain charge integrating preamplifier, building on the experience of the AGIPD detector
- A sampling stage with charge injection compensation
- A Correlated Double Sampling (CDS) stage capable of operation in different topologies.

Four variants of an SAR ADC developed by Bonn University

After verification and characterisation of these building blocks, we will follow a gradual approach with a first generation ASIC focusing on the 'time domain'i.e. reaching the specifications for pixel pitch and readout speed, while a 2^{nd} generation chip will focus on 'analogue specs'optimising noise and extending the dynamic range to the final goal. This way unforeseen effects like crosstalk and substrate coupling as well as 'scale effects'will be known and can be countered on the 2^{nd} generation chip.

We will present the CoRDIA ASIC's architecture along with test strategies and results from the MPW prototypes.

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