

3D integration approaches for SiPM: from BSI to TSV

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01

FBK SiPM technology

FBK SiPM technology roadmap
and motivation for 3D integration

02

BSI SiPM for NIR

03

TSV interconnections for
VUV/NUV SiPM

04

Conclusions

01

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BSI SiPM for NIR

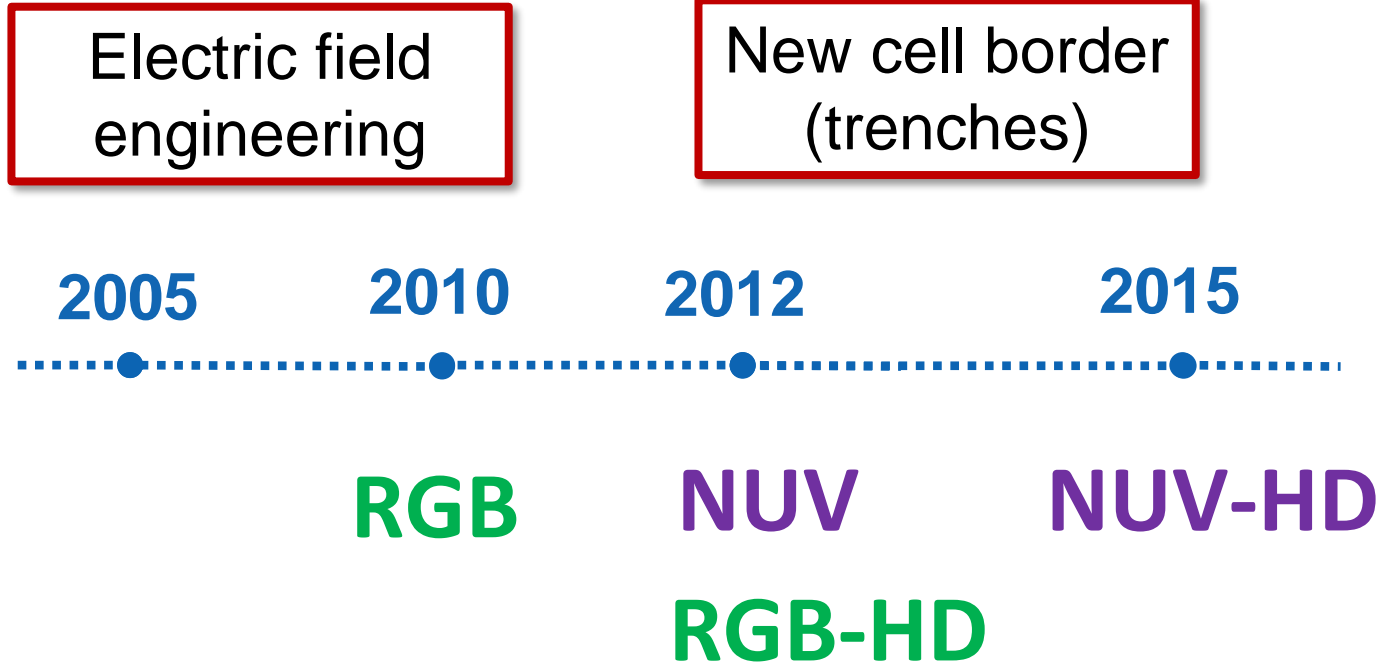
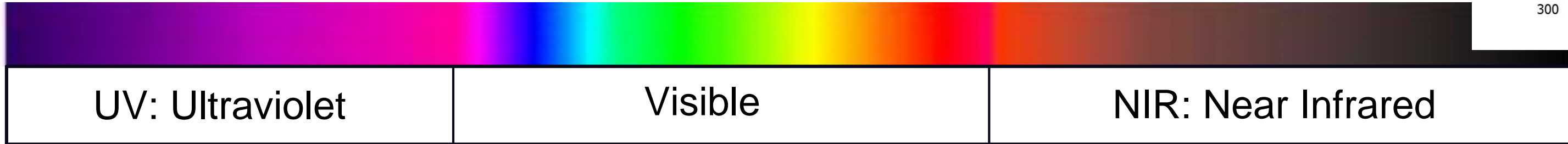
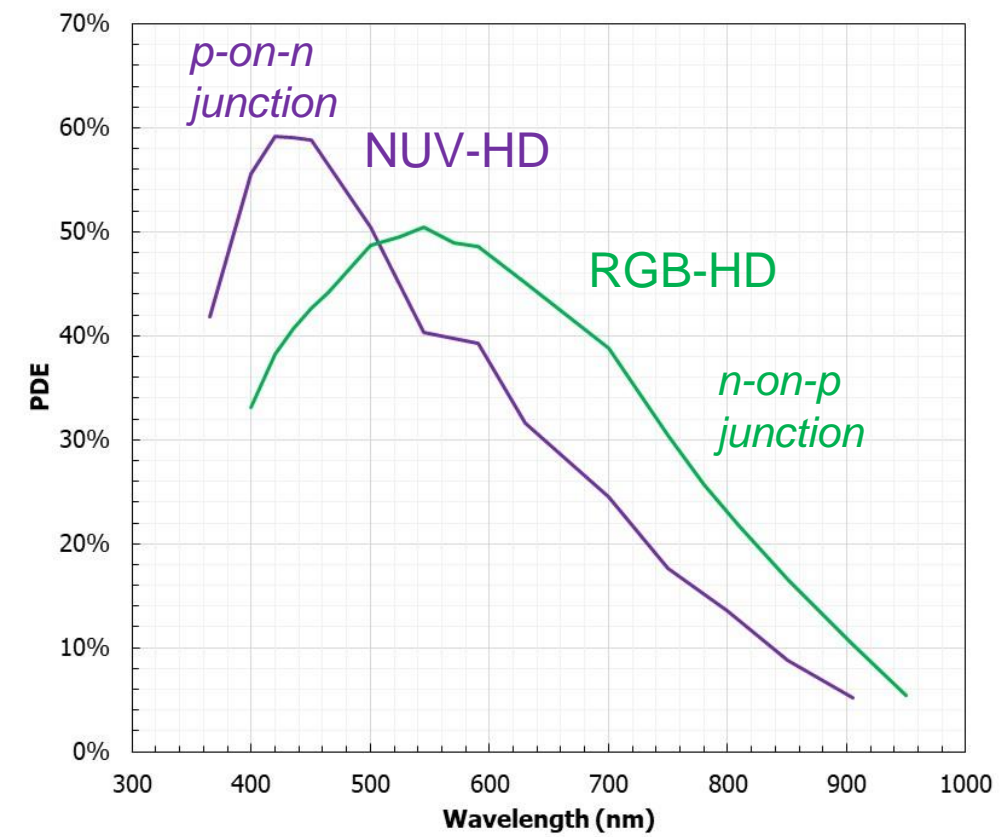
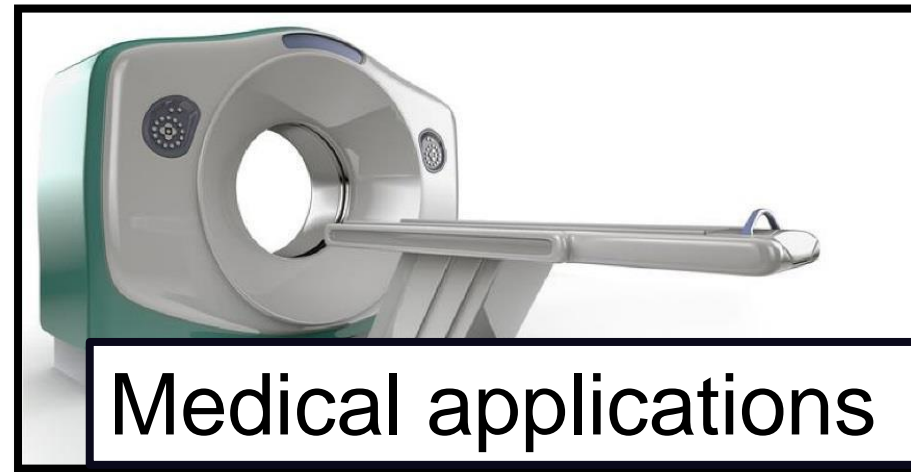
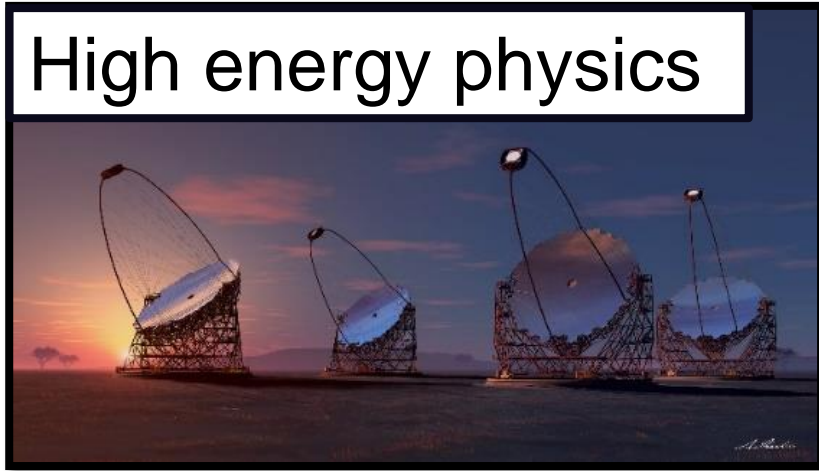
03

TSV interconnections for
VUV/NUV SiPM

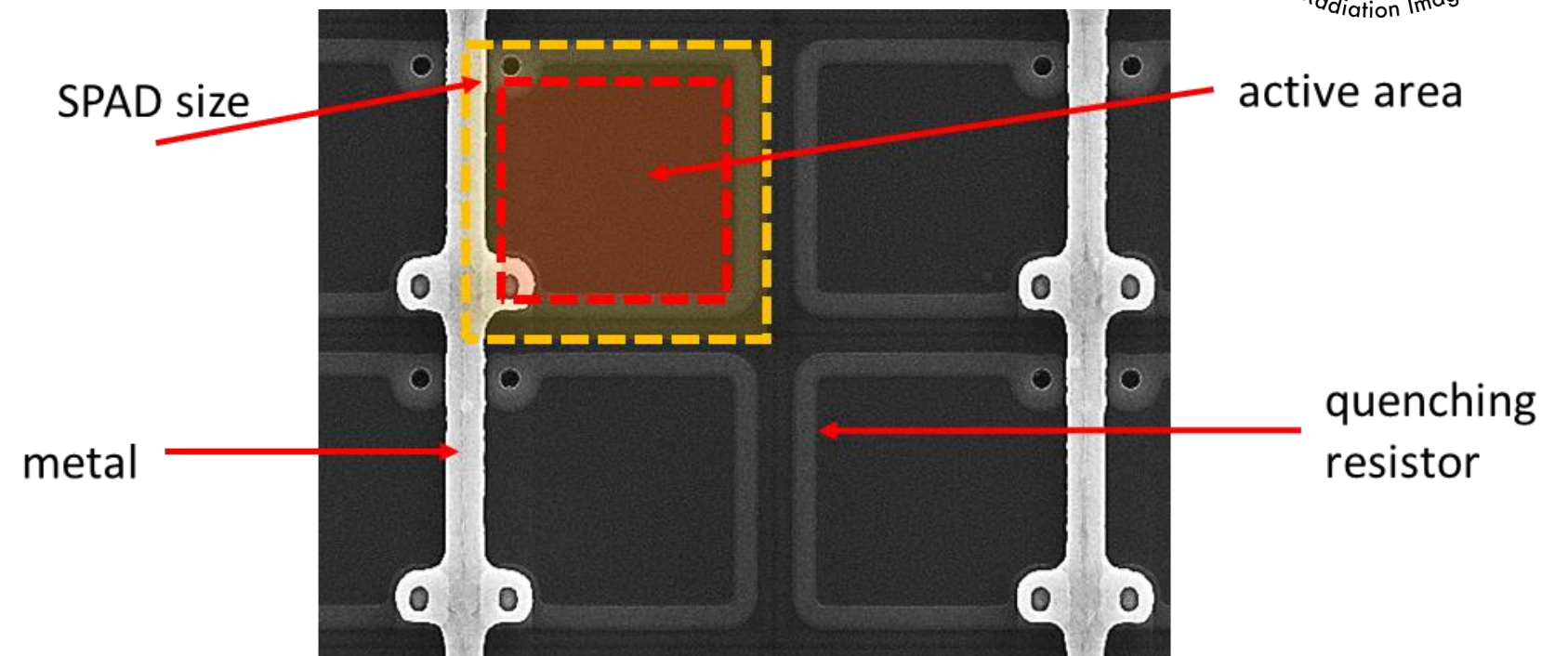
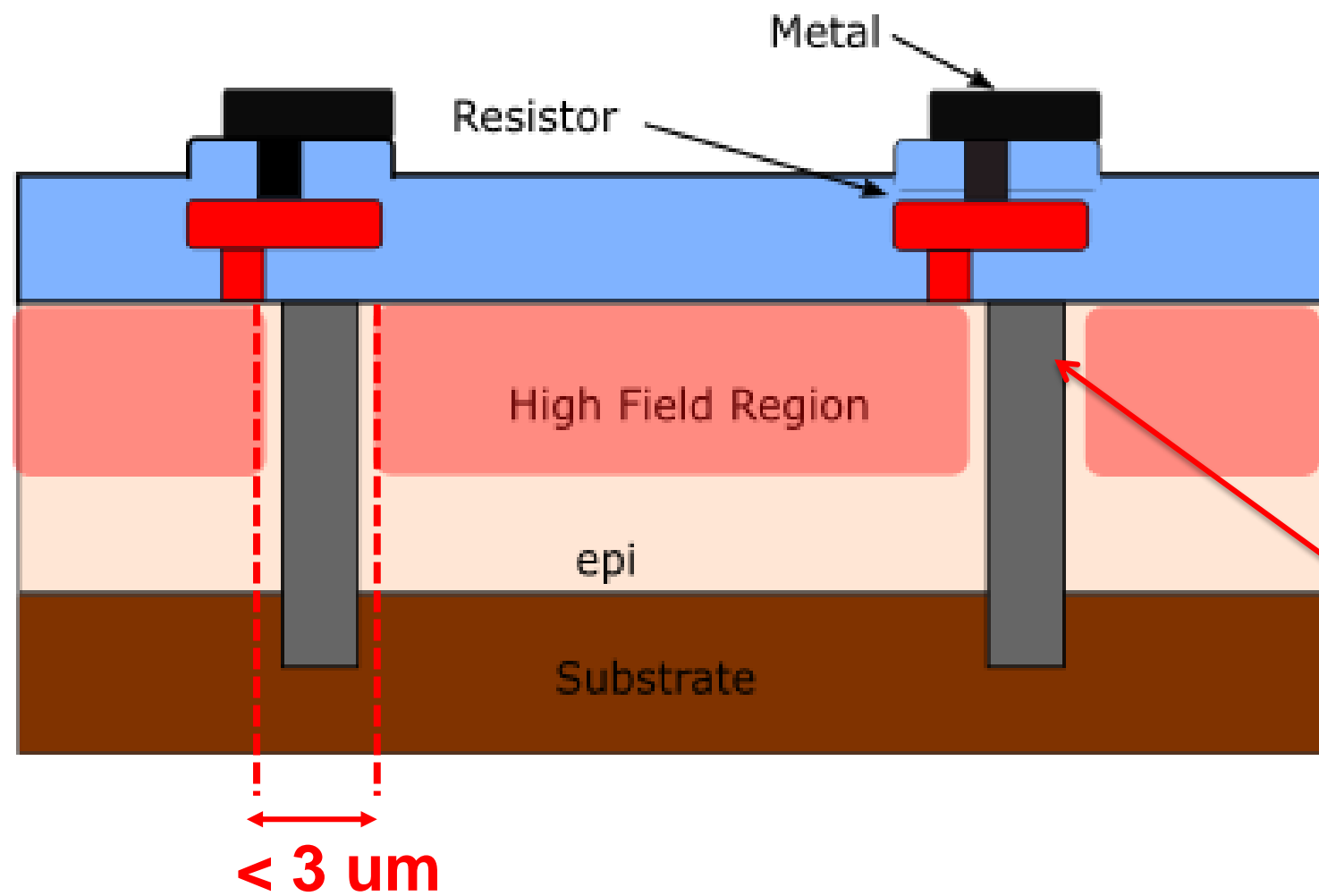
04

Conclusions

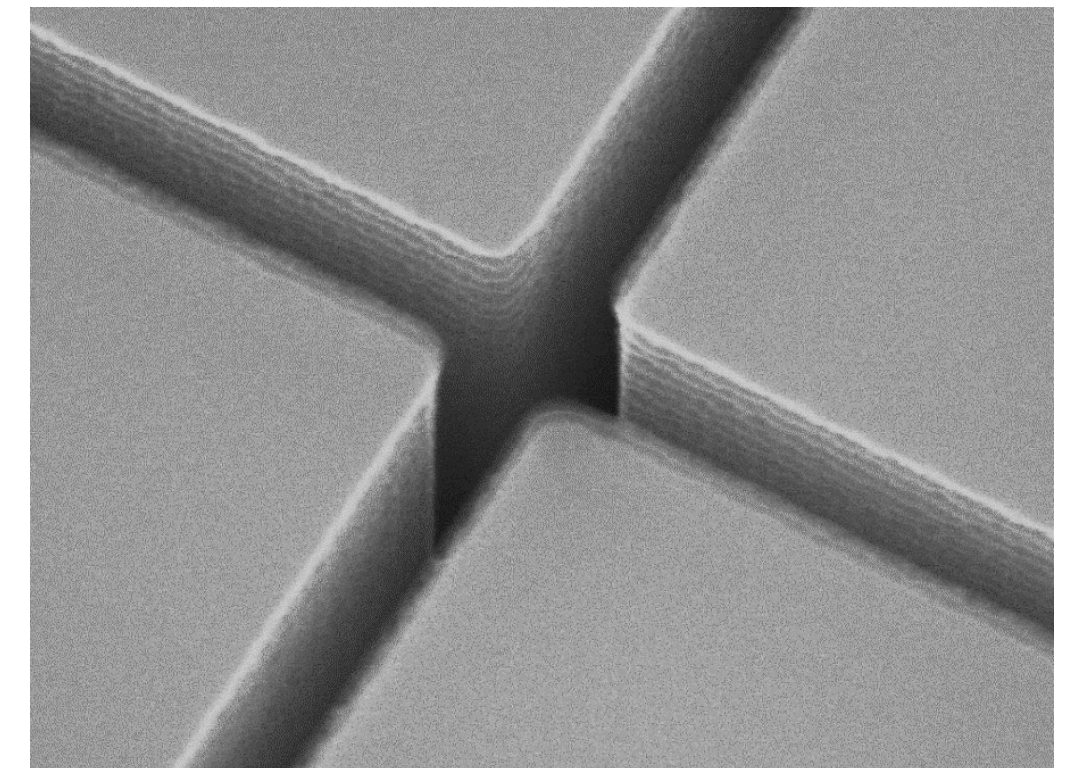
FBK SiPM technology



HD Silicon Photomultiplier Technology

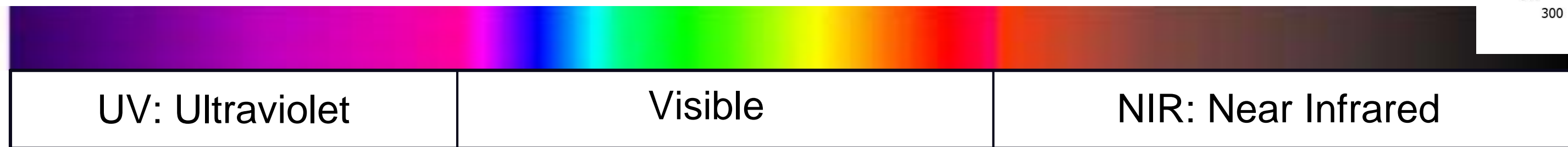
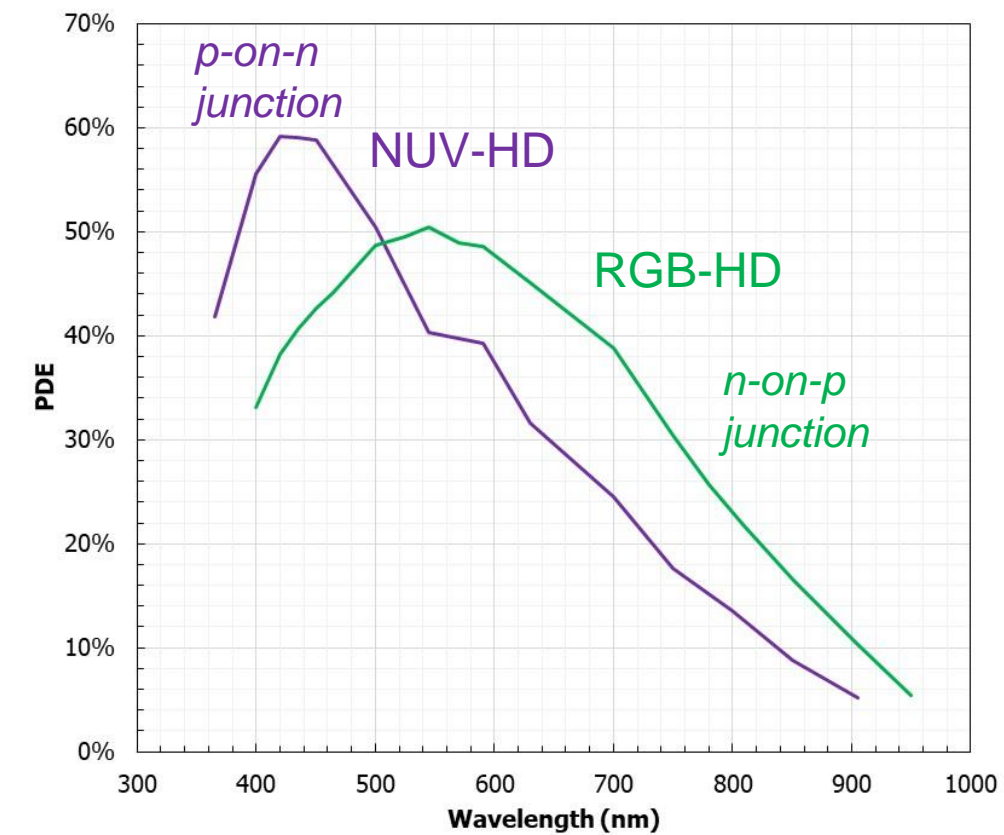
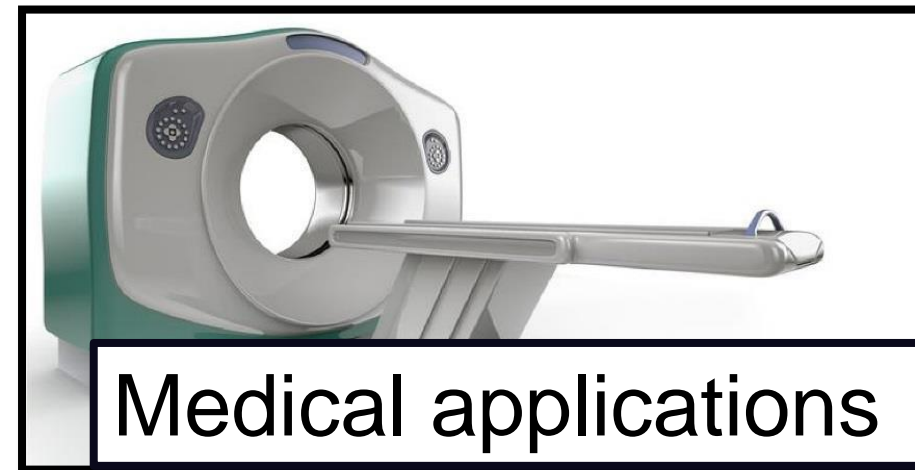
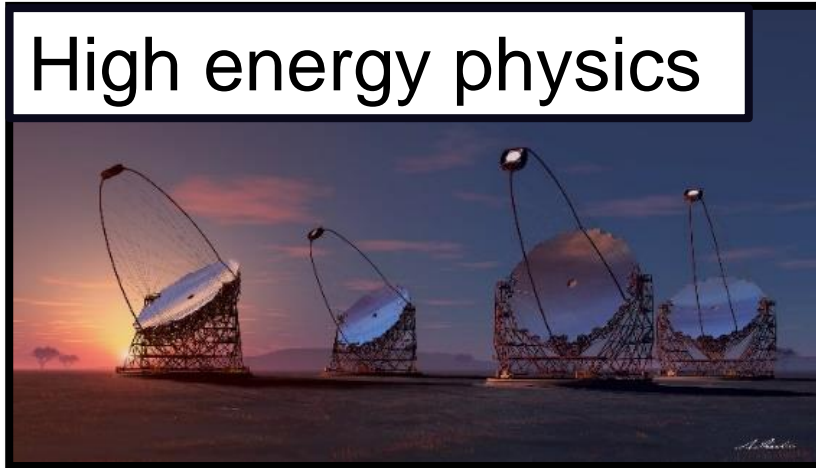


Deep Trench



- Trenches between cells → Lower Cross-Talk
- Cell pitch: 15 – 40 μm
- Narrow dead border region → Higher Fill Factor (>80%)
- Make it simple: 9 lithographic steps

FBK SiPM technology



Electric field engineering

New cell border (trenches)

NUV-HD-Cryo

Ultra high cell density (very small cells)



RGB

NUV

NUV-HD

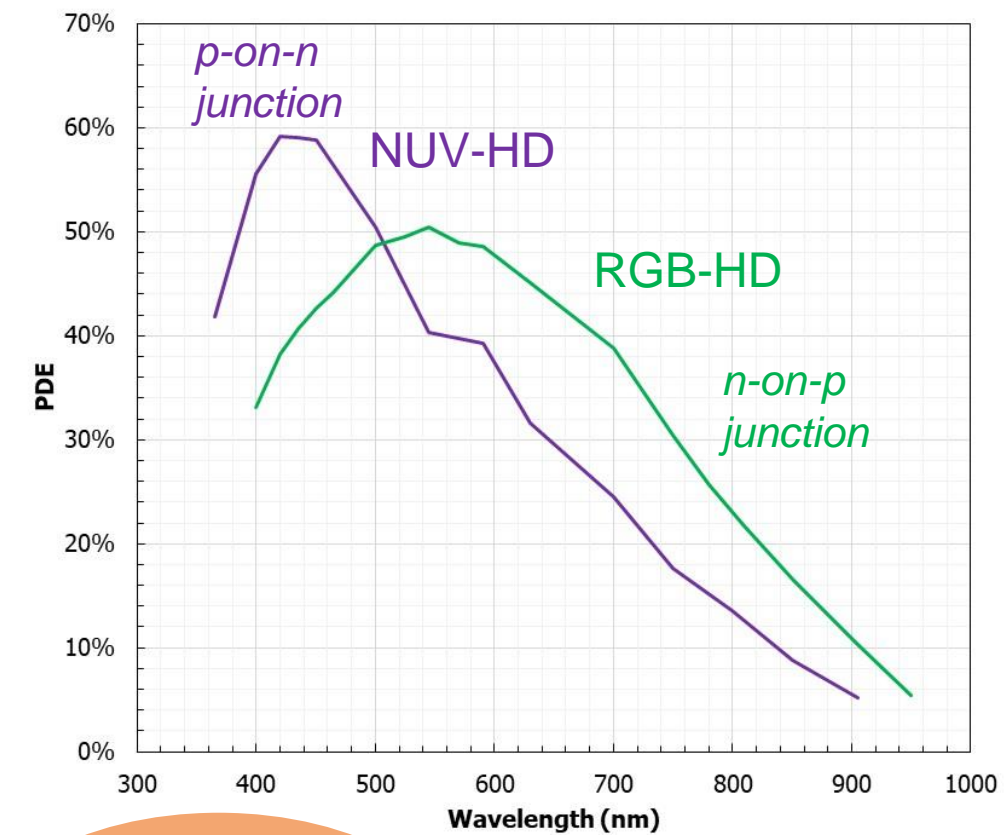
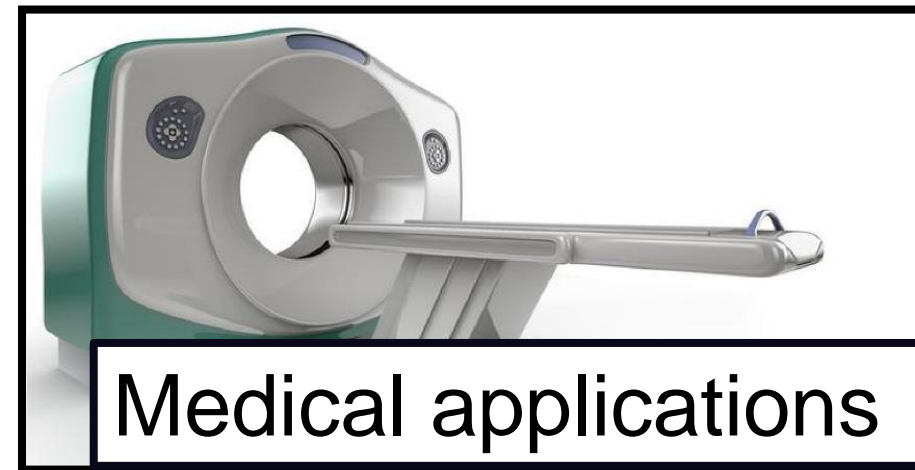
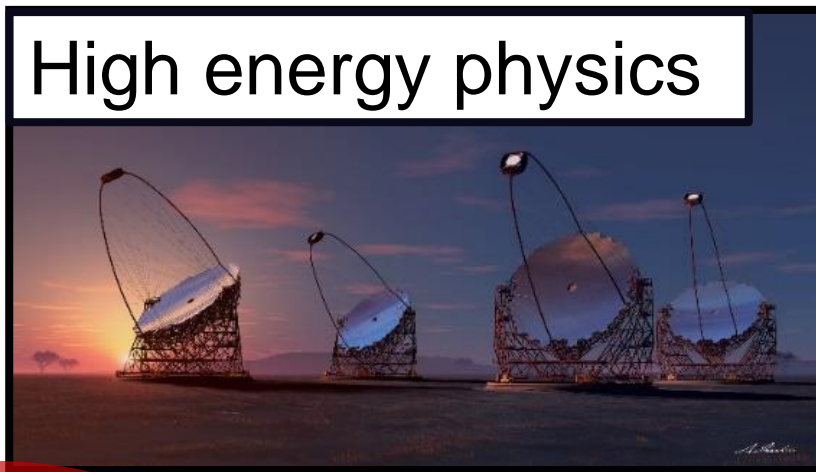
2016

RGB-UHD

RGB-HD



FBK SiPM technology



VUV

UV: Ultraviolet

Visible

NIR: Near Infrared

NIR

Electric field engineering

New cell border (trenches)



NUV-HD-Cryo

NIR-HD

2005

2010

2012

2015

2017

2019

RGB

NUV

NUV-HD

2016

RGB-UHD

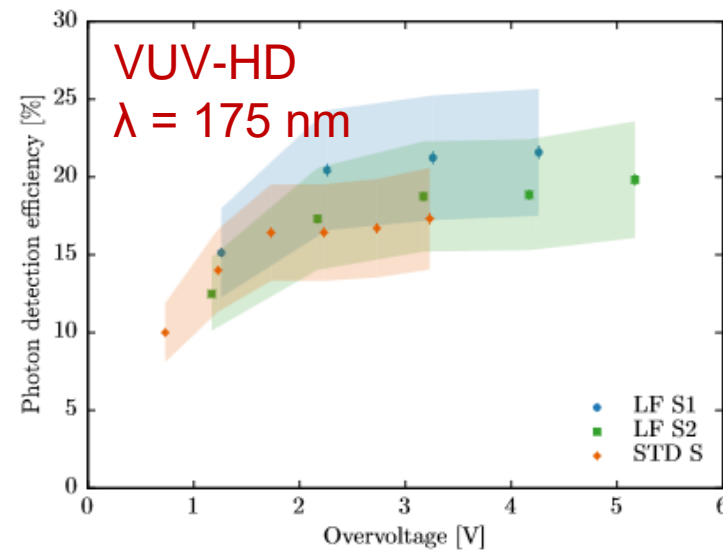
2018

VUV-HD

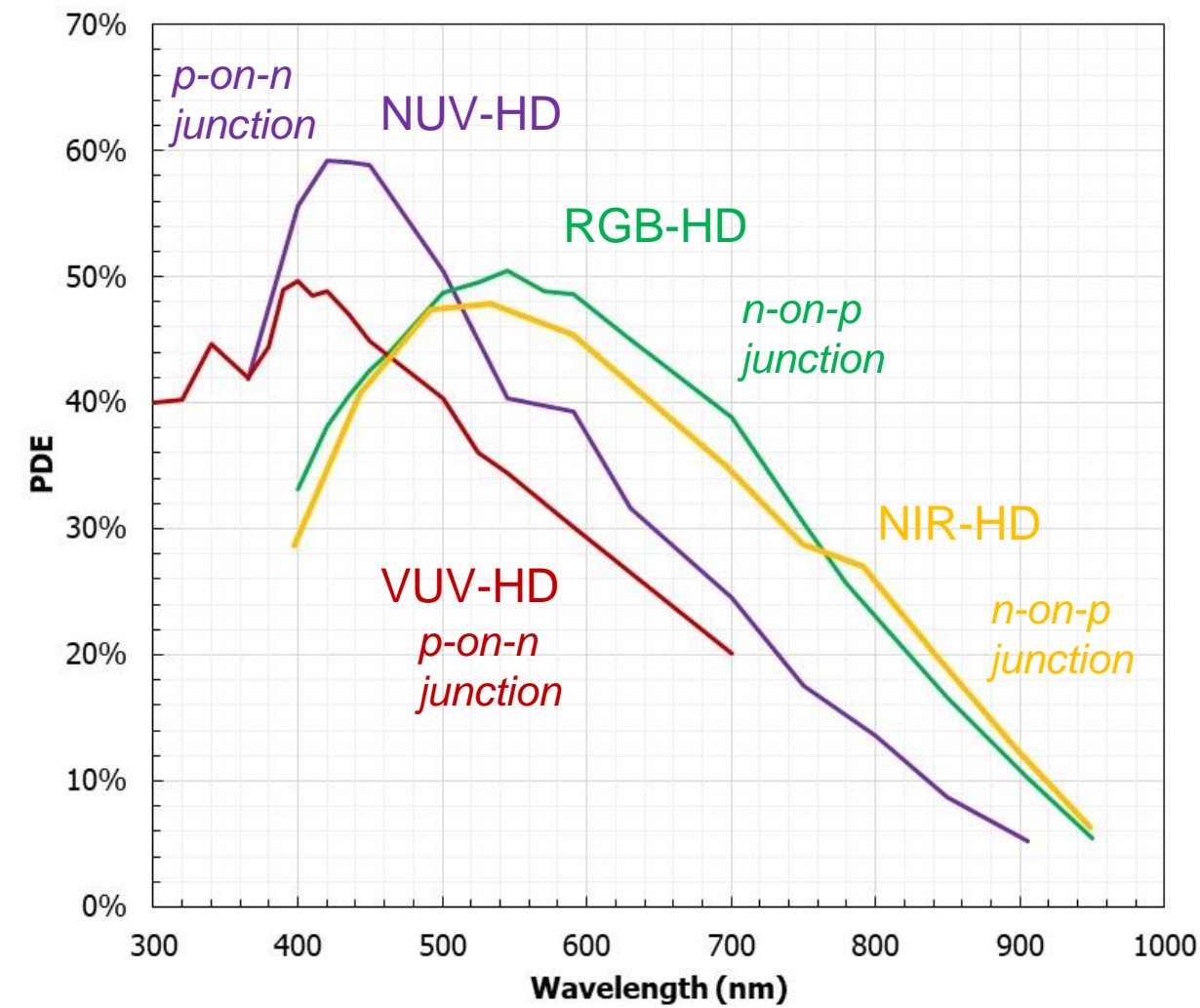
Ultra high cell density (very small cells)



FBK SiPM technology



Jamil, A., et al. "VUV-sensitive silicon photomultipliers for xenon scintillation light detection in nEXO." *IEEE Transactions on Nuclear Science* 65.11 (2018): 2823-2833



Electric field engineering

New cell border (trenches)

2005

2010

2012

2015

NUV-HD-Cryo

2017

NIR-HD

2019

RGB

NUV

NUV-HD

2016

RGB-UHD

2018

VUV-HD

Ultra high cell density (very small cells)

Ongoing Developments

3D integration

Hybrid SPAD arrays/SiPM

BSI NIR-HD

TSV VUV-HD

3D Integration: Hybrid SPAD array/SiPM

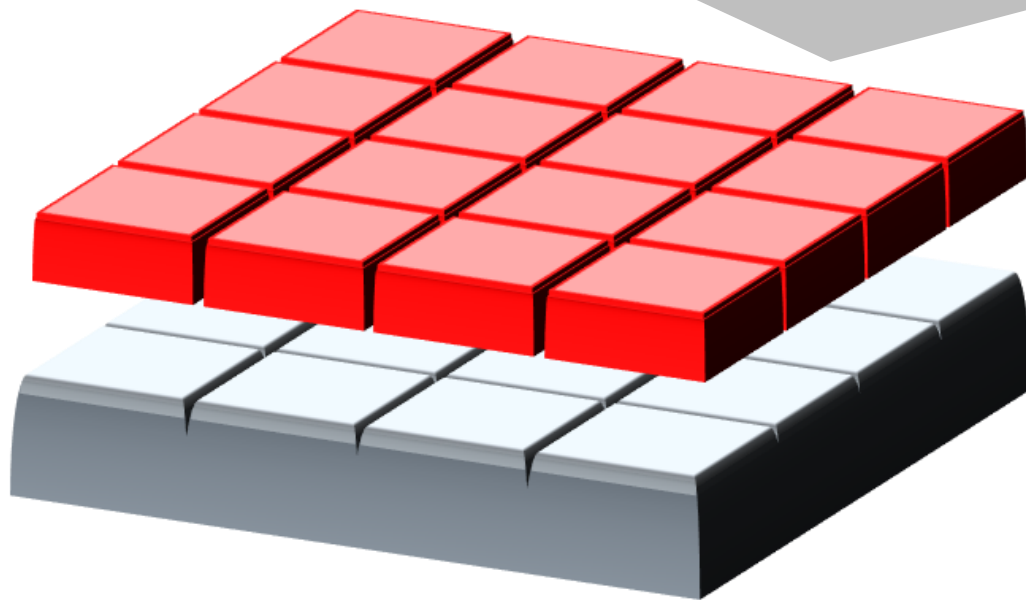
In the Framework of IPCEI project, FBK proposed an R&D aimed at developing an **hybrid sensor** integrating:

- SPAD in Custom Technology
- CMOS read-out electronics

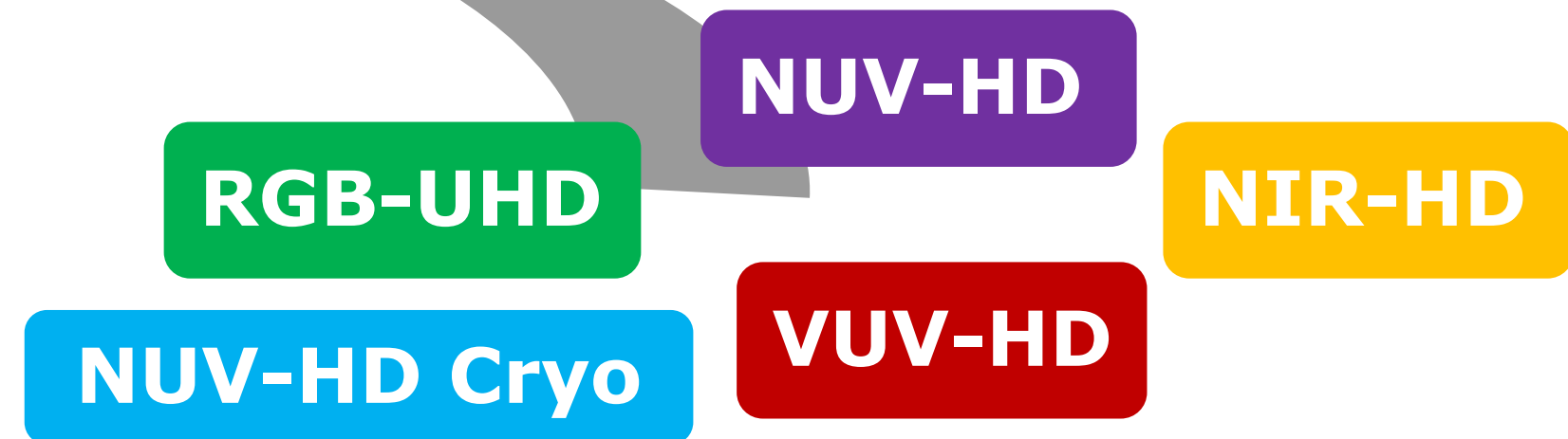
Main Advantages:

- Preserving the performance in terms of PDE and DCR of SPADs in custom technology
- Adding some functionality at pixel level and further electronics at chip level

CUSTOM SPAD array/SiPM



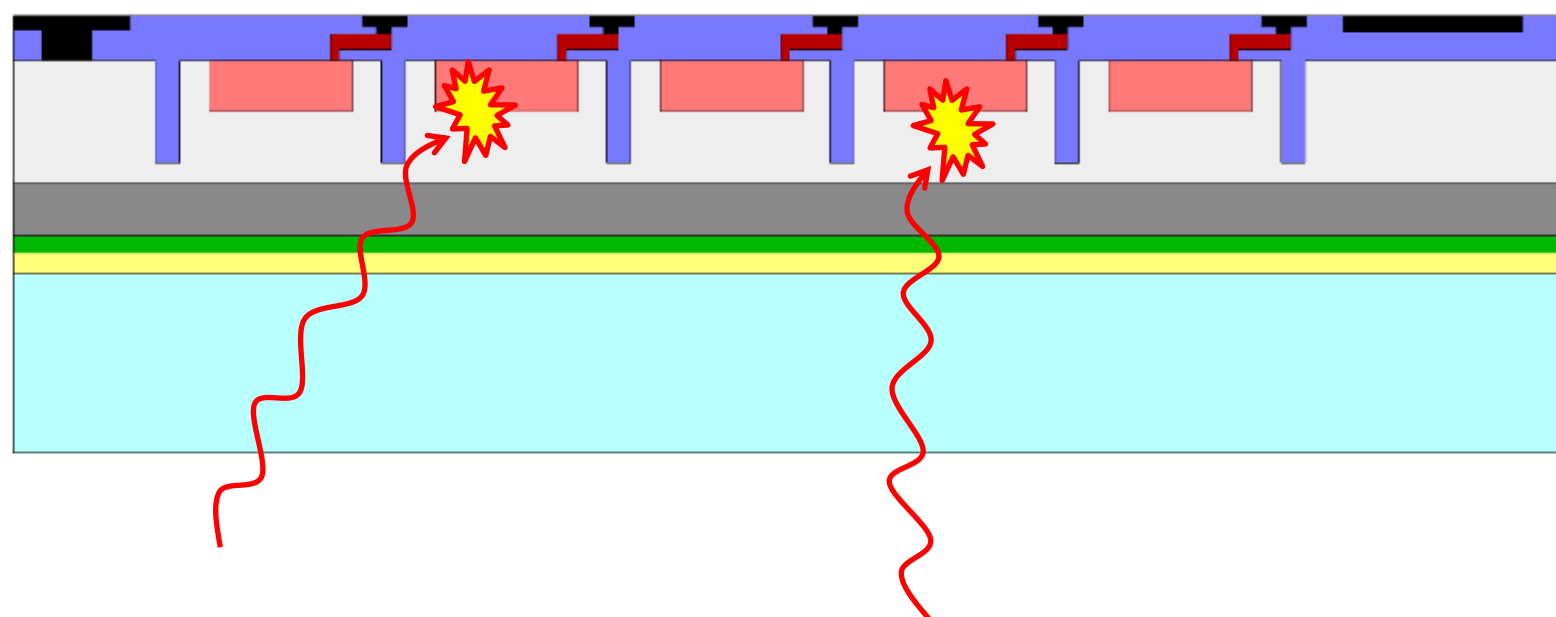
CMOS read-out electronics



- Ultra-Versatile Technology platform
- It combines all the advantages of a sensor in custom technology with the advantages of an integrated CMOS readout

3D Integration schemes

Back Side illumination for Visible/NIR



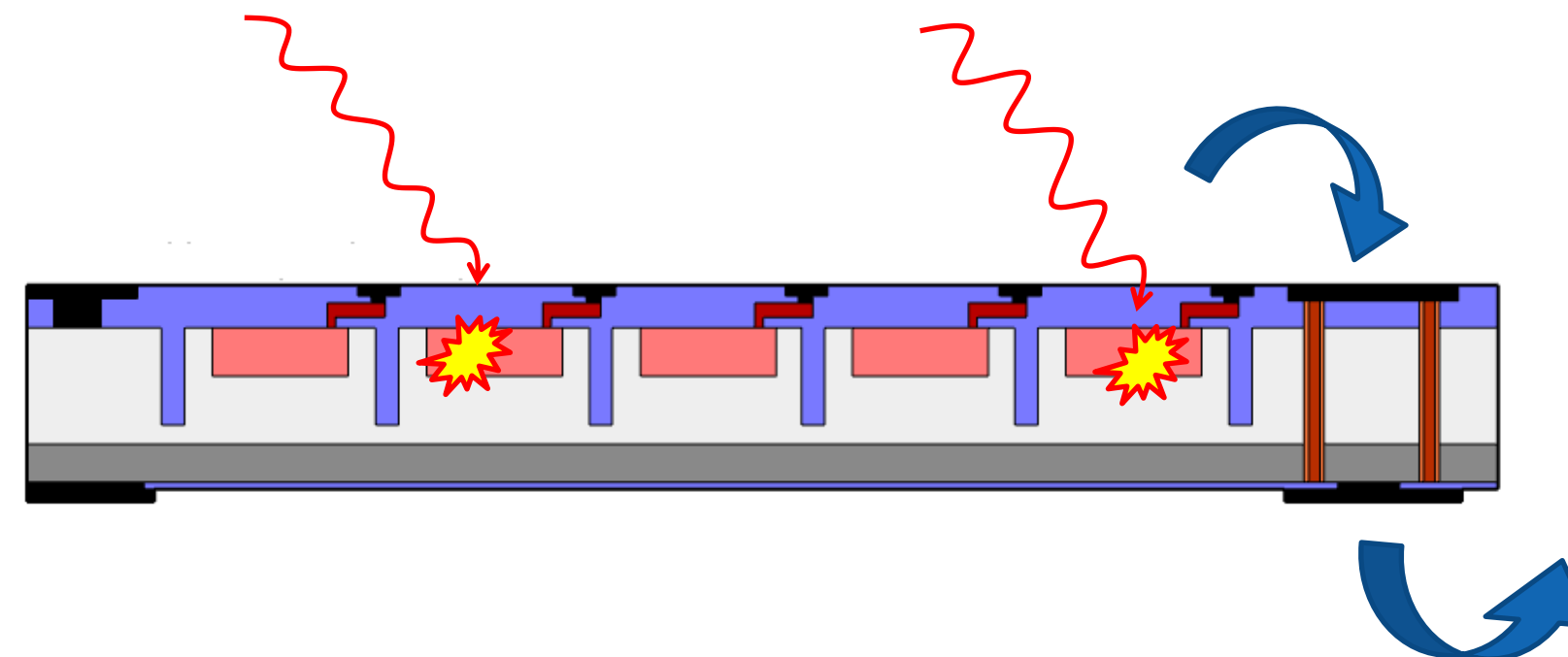
Pro:

- 100% FF
- TSV-free

Cons:

- Very thin sensor devices

Front Side Illumination for NUV/VUV



Pro:

- Much shallower junction depth
- Unaffected device performance

Cons:

- TSV connections
- FF losses due to TSV and BEOL

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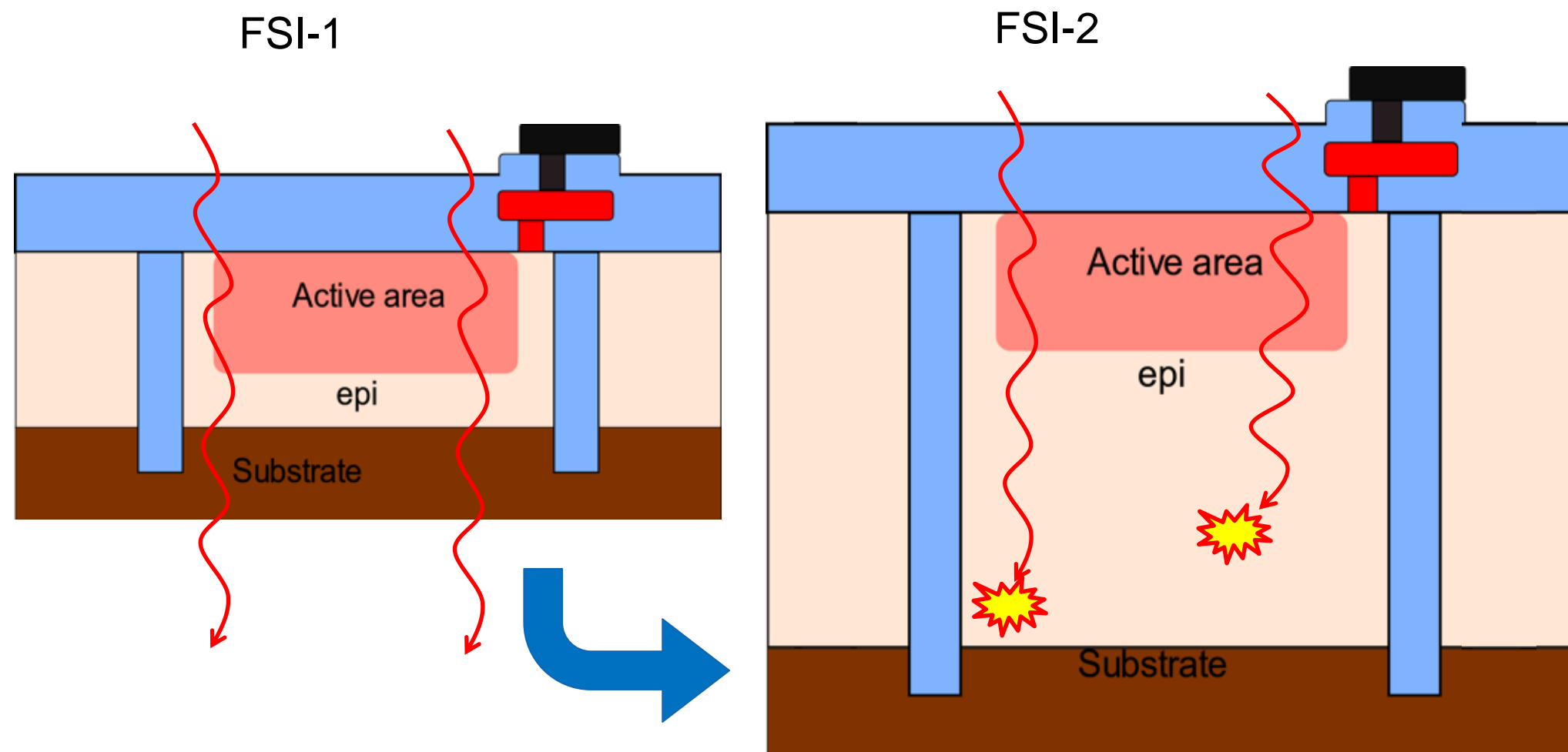
TSV interconnections for
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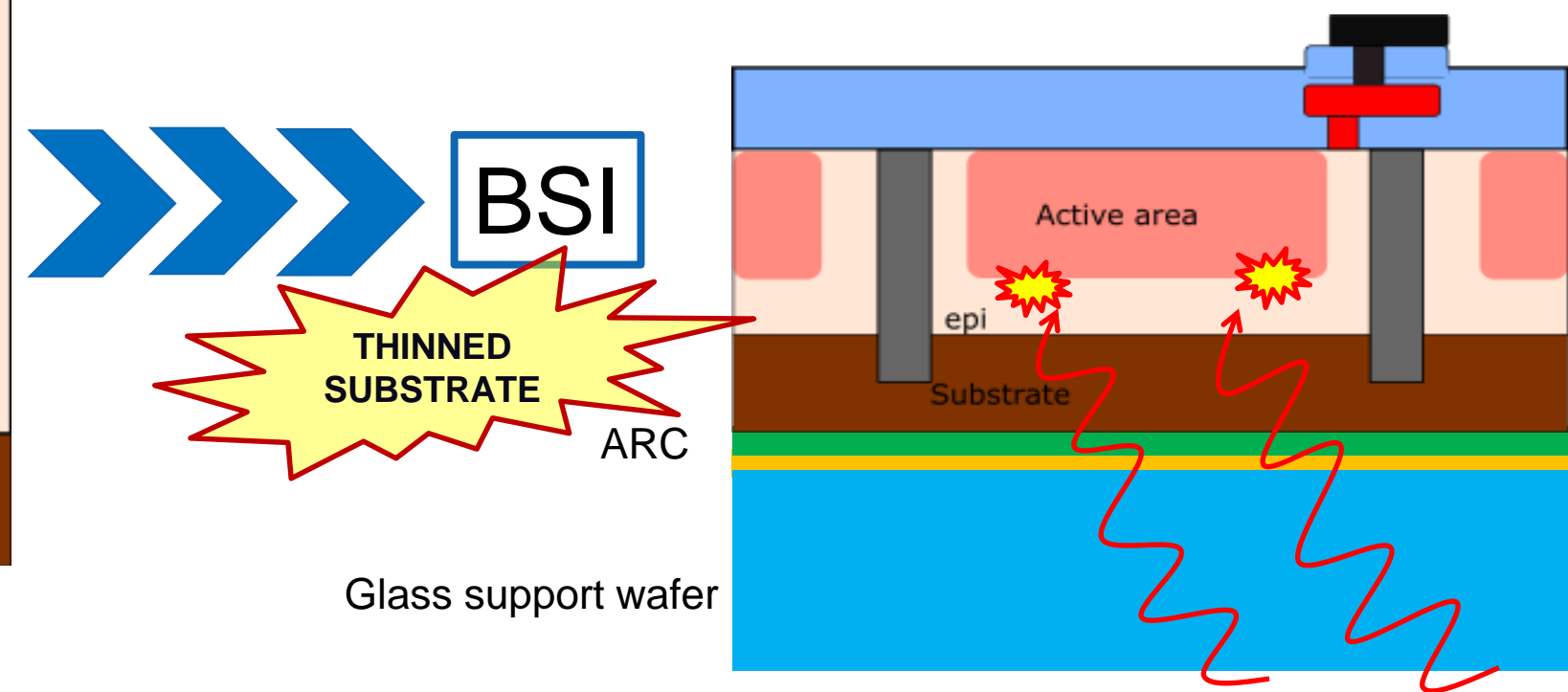
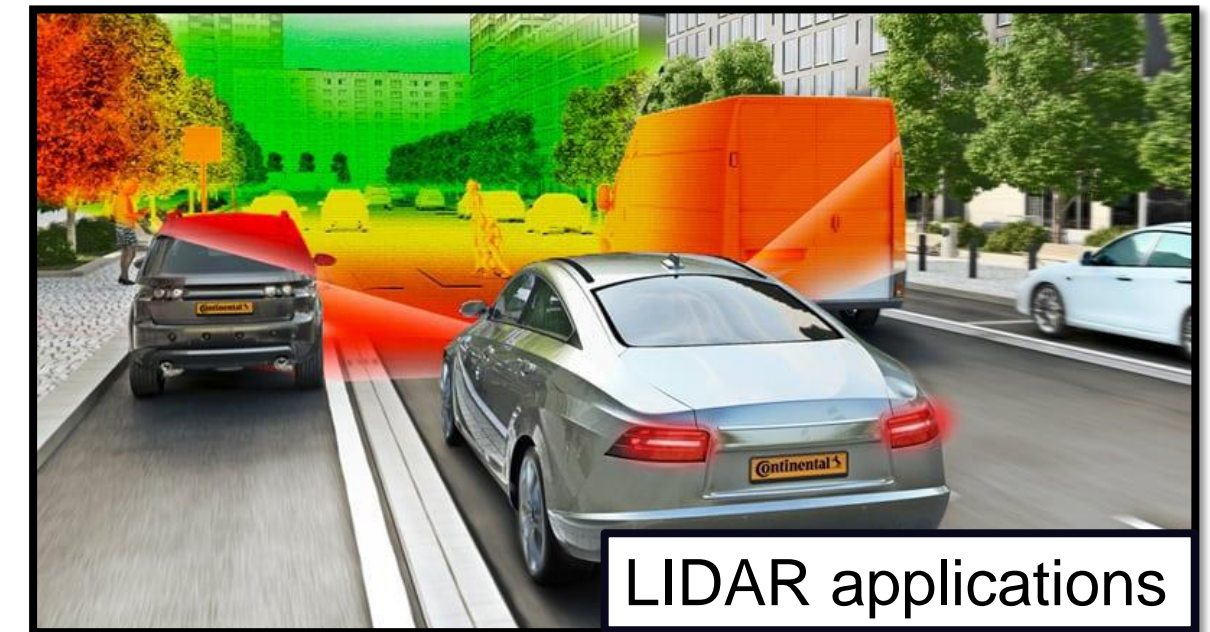
Conclusions

FSI vs BSI NIR SiPM

NIR light with energy close to the Si bandgap interacts deeper in the substrate

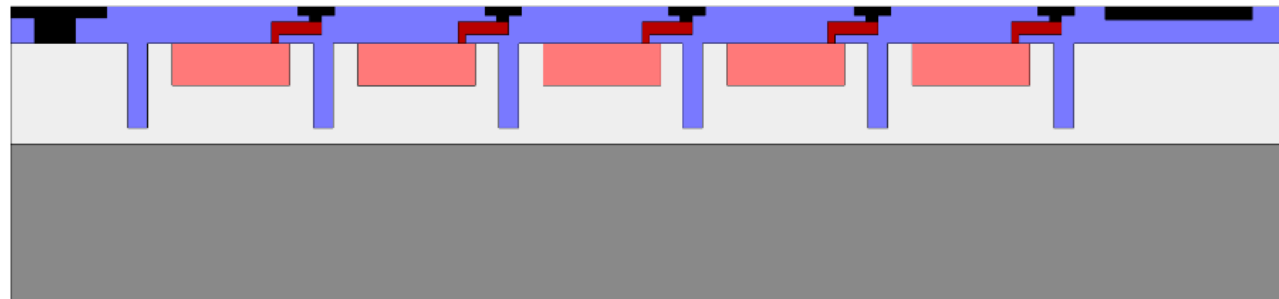


Thicker epi-Silicon is used to increase absorption

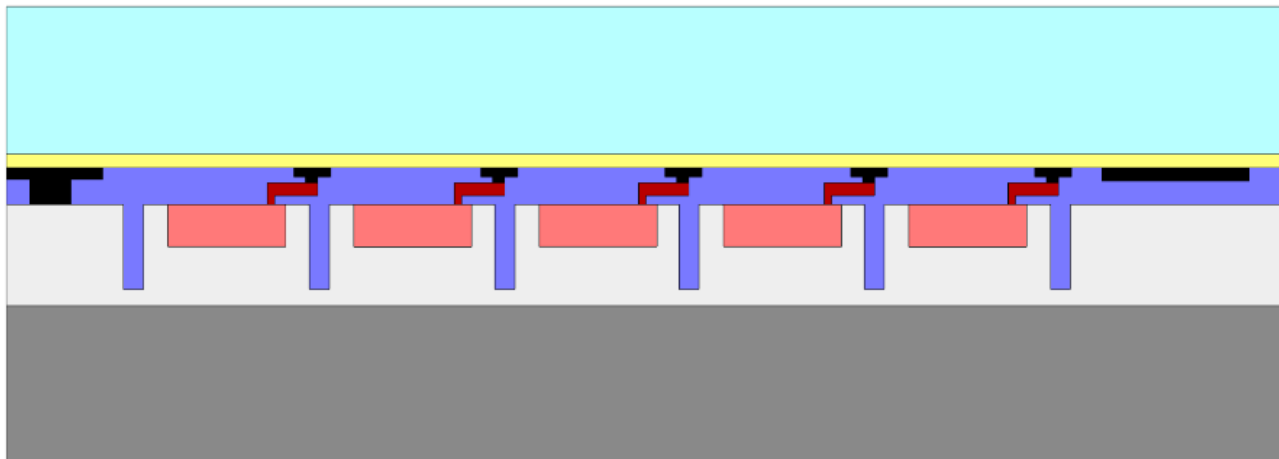


BSI NIR SiPM process flow

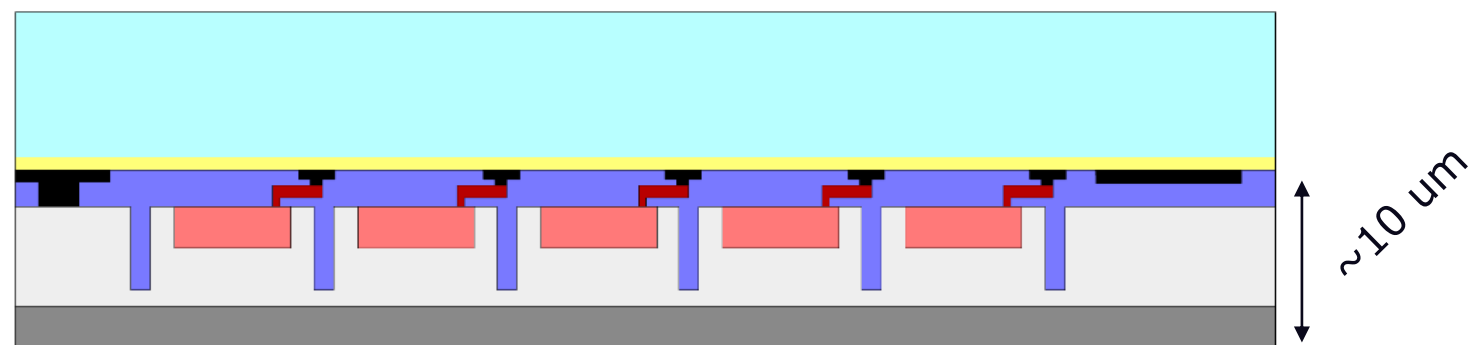
1. SiPM Wafer



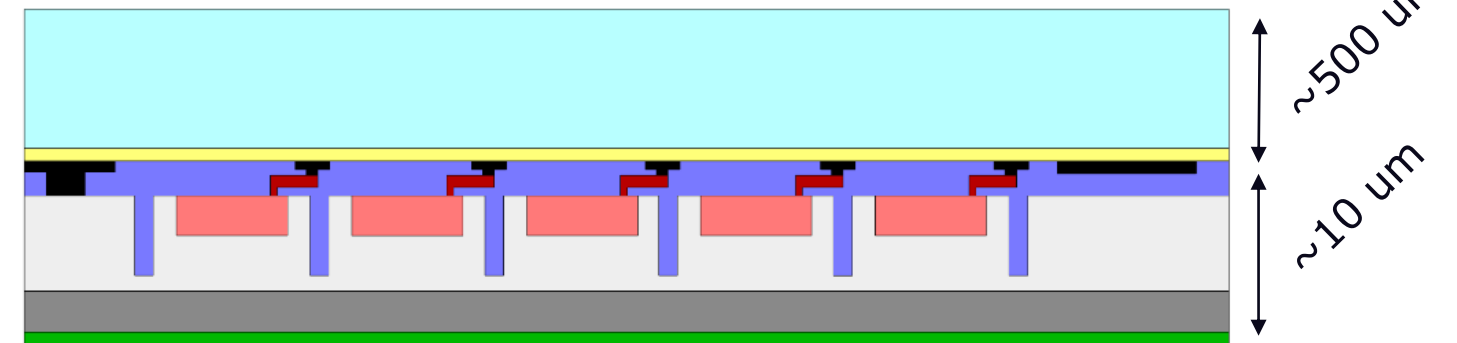
2. Temporary Bonding



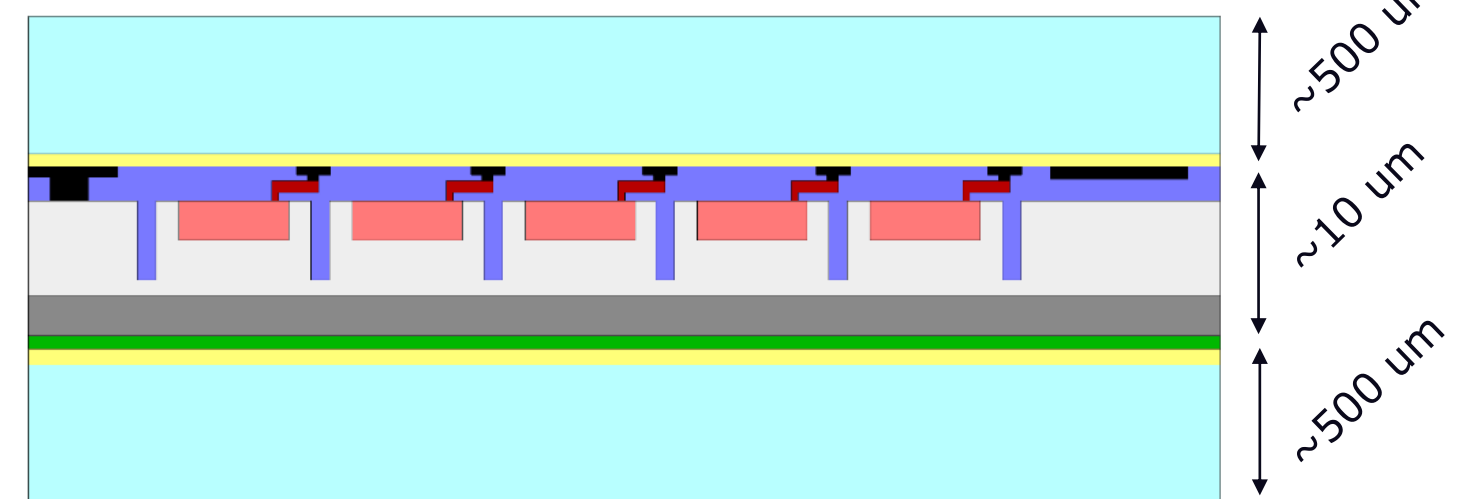
3. Grinding & Polishing



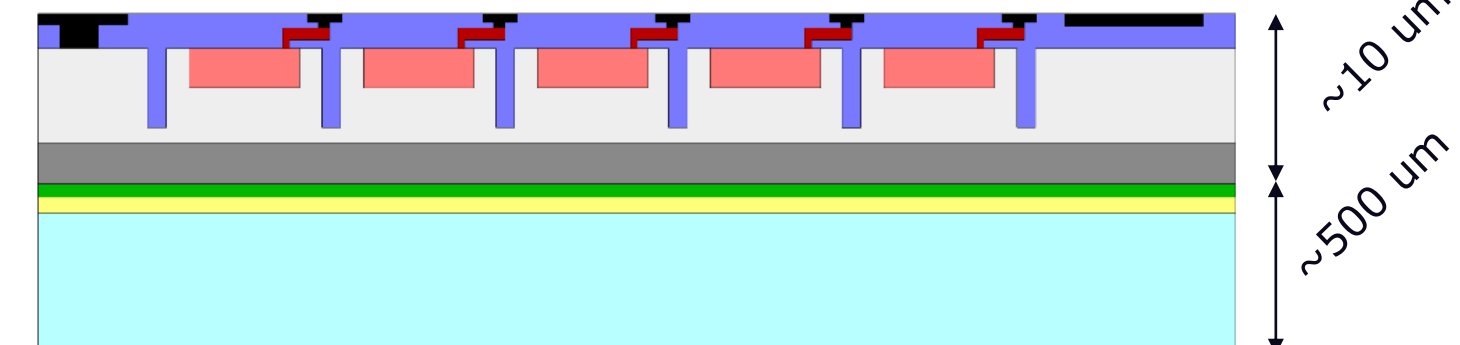
4. Backside processing



5. Permanent Wafer Bonding



6. Wafer Debonding



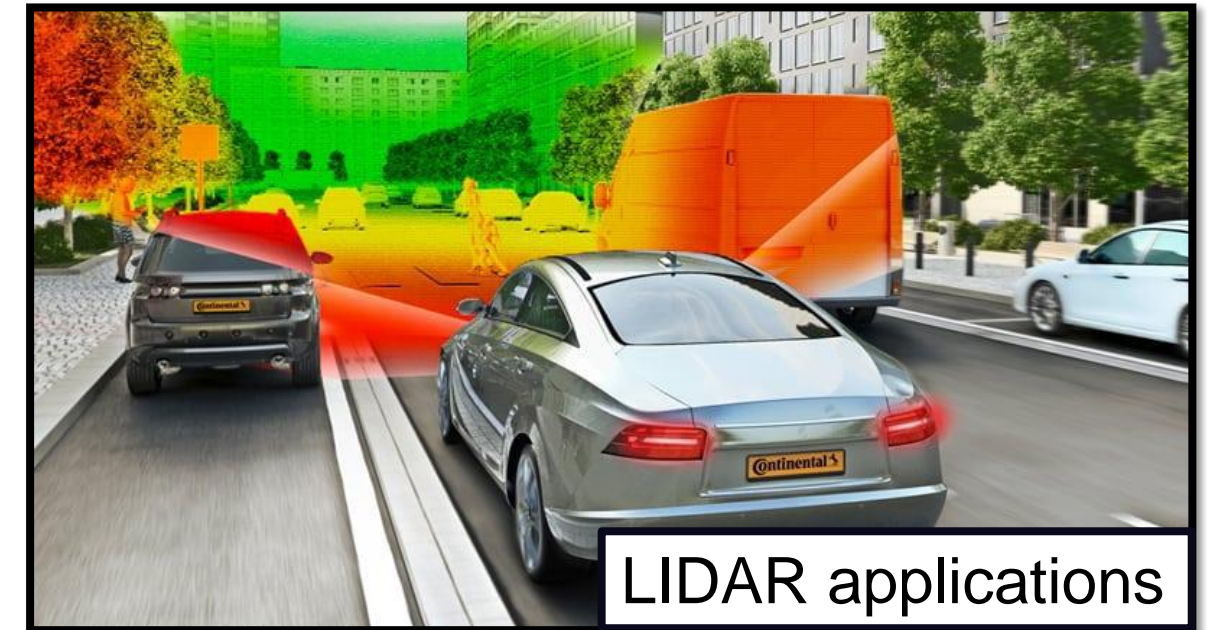
BSI NIR SiPM

Advantages

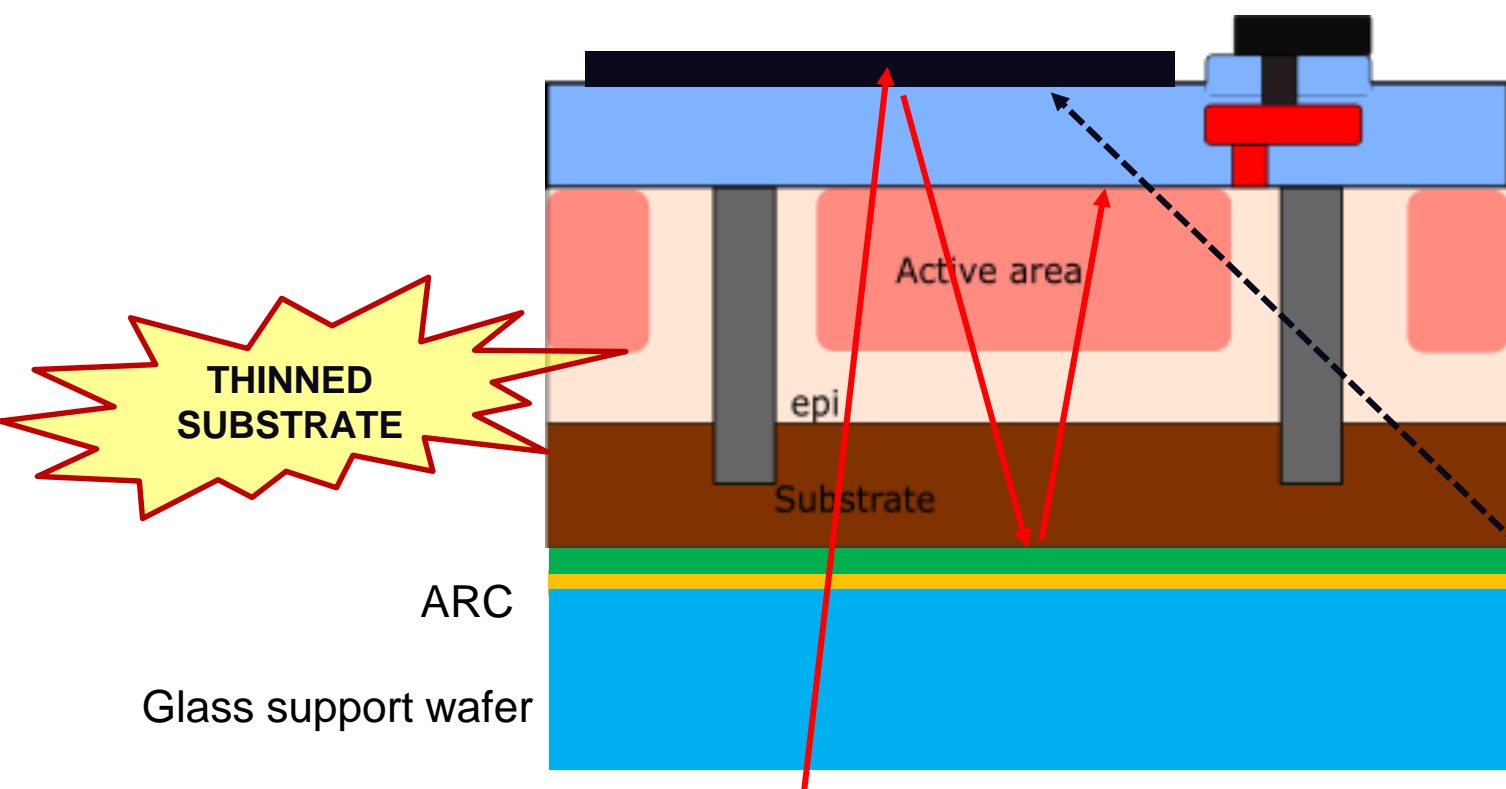
- 100% FF
- Increase the absorption thanks to light trapping
- Ready to be 3D integrated

Challenges

- Absorption depth of NIR photons in silicon ~30 μm



LIDAR applications



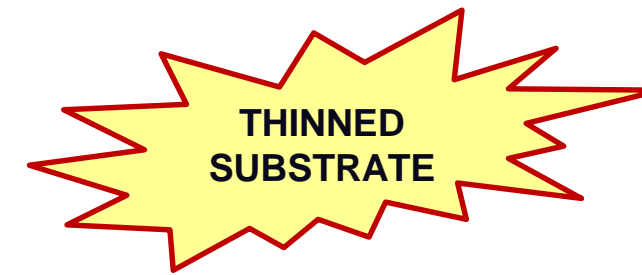
Photons reflected at the entrance surface
 Photons absorbed in the residual substrate
 Photons escaping from the front surface
 Photons absorbed in the active area
 Photons back reflected at the front surface (light trapping)

lost

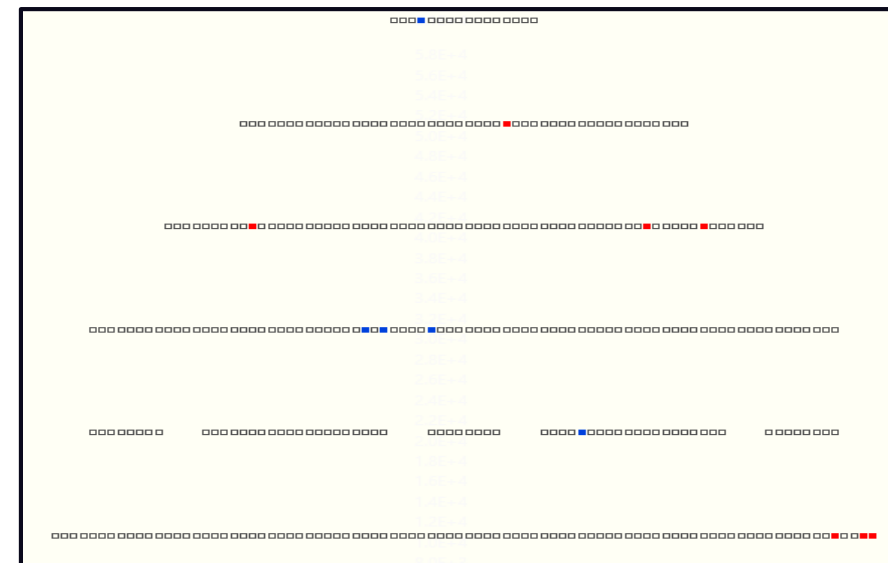
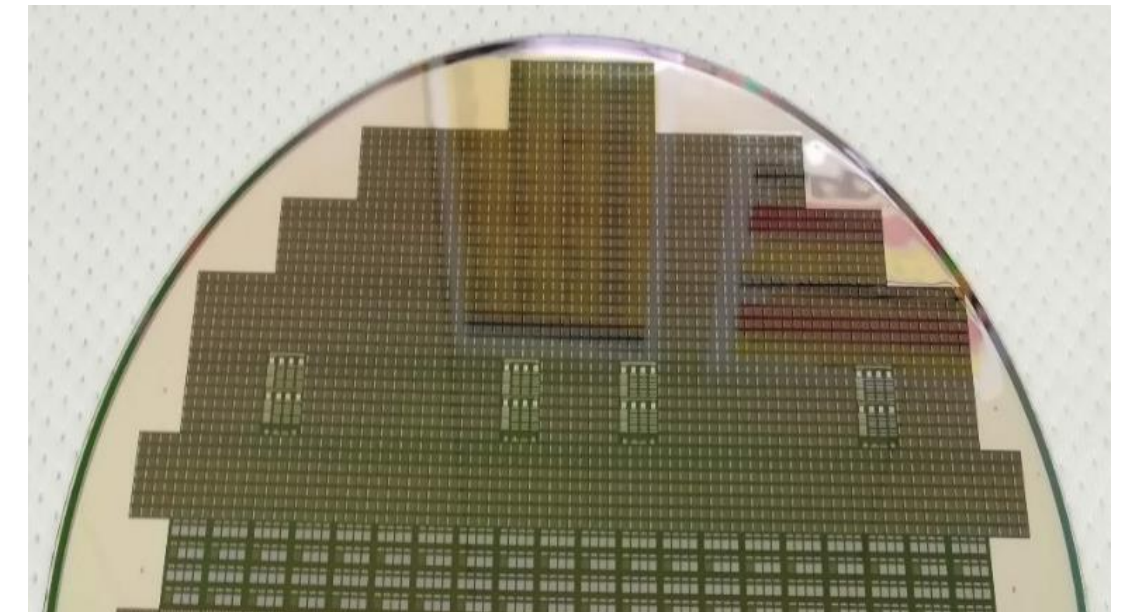
counted

Including metal plate on the top surface can enhance the light trapping

Results on BSI SiPM for NIR



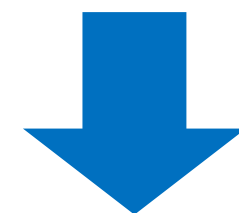
Ultrathin substrate (~ 10 um)



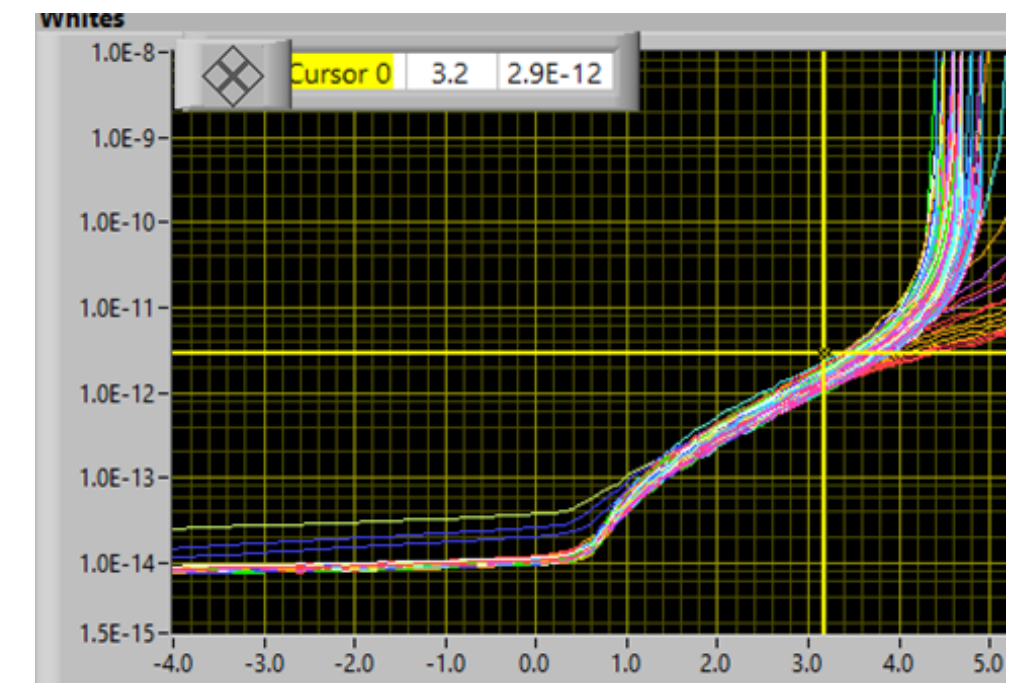
Electrical characterization

- Automatic I-V measurements after ultra-thinning
- 180 SiPMs (1 mm²) have been measured on a 6" wafer
- 169 working SiPMs (~ 95% yield).

- Compilation of I-V curves from a single back-thinned wafer
- Same BD voltage and same dark current w/o and with thinning

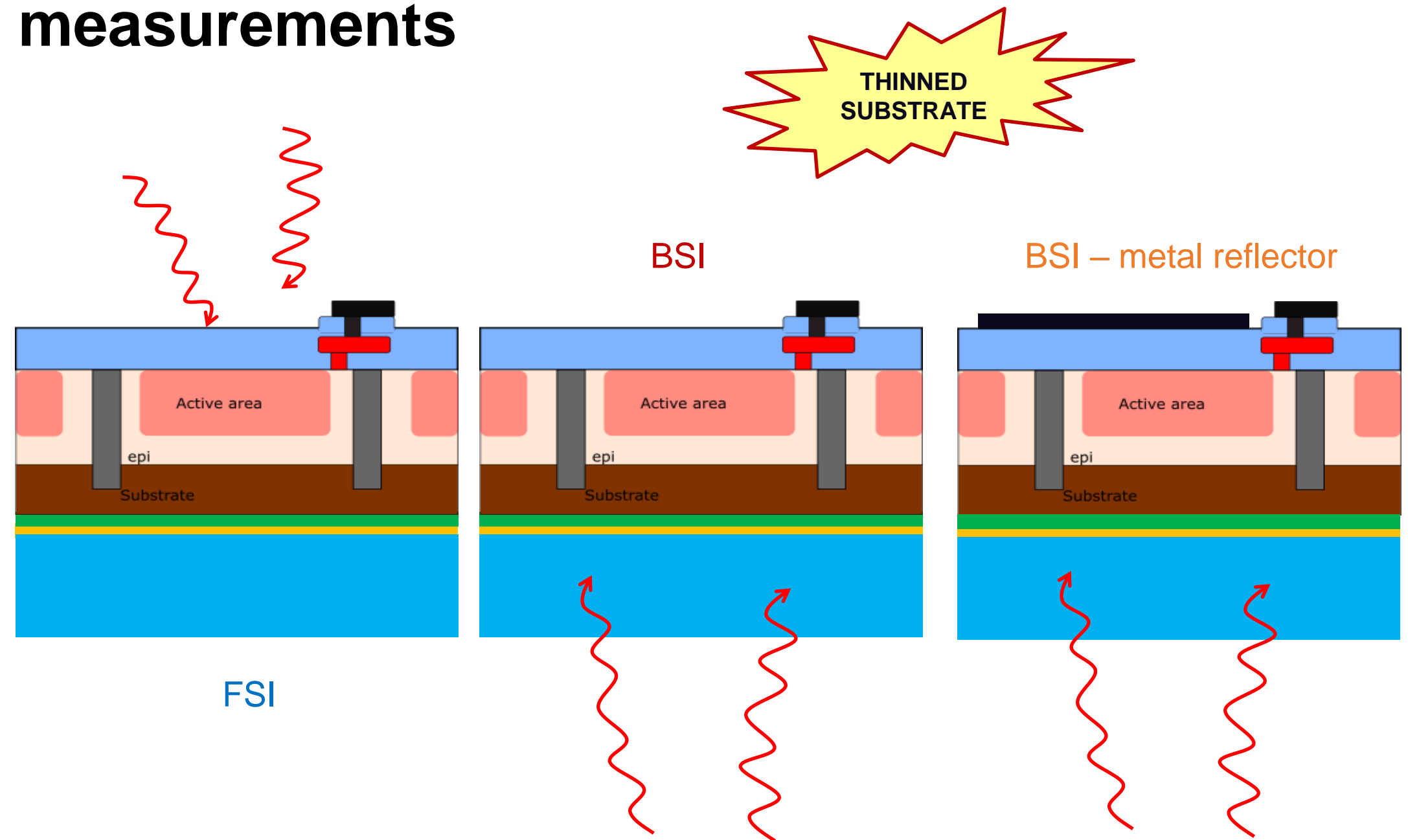
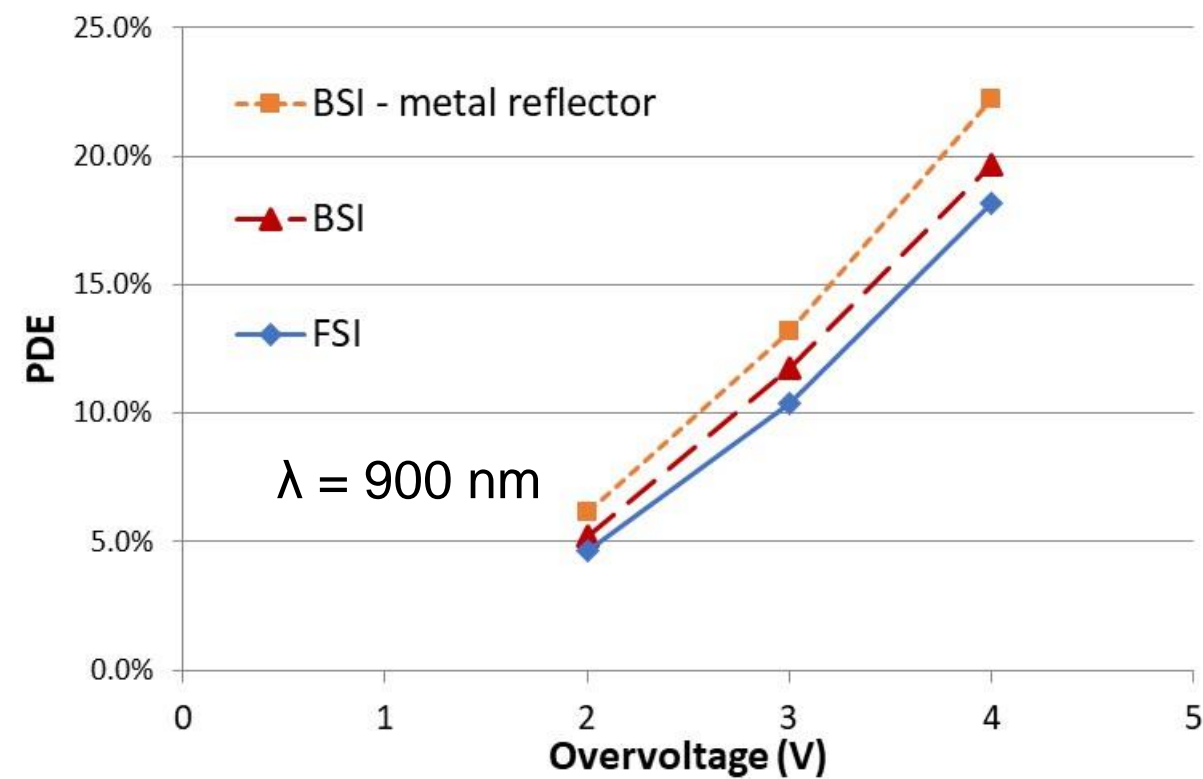


- The thinning process does not degrade the electrical and noise performance of the device at a low excess bias voltage



Results on BSI SiPM for NIR

Photon detection efficiency measurements



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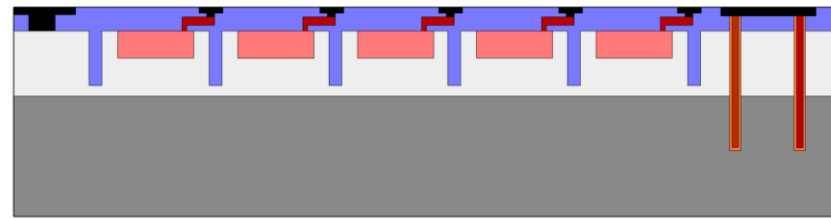
03 TSV interconnections for
VUV/NUV SiPM

04 Conclusions

Through Silicon Vias

Via Mid

- SiPM fabrication + TSV formation

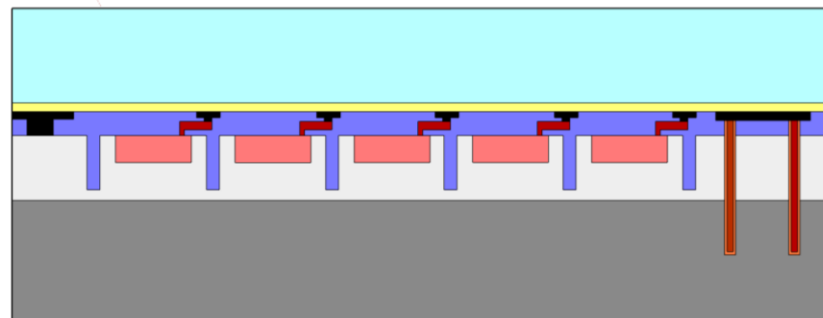


High thermal budget allowed (high quality and conformal material deposition)

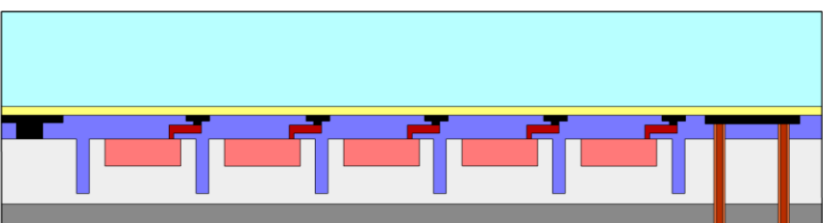


Necessity to adapt the device process flow
→ Critical lithography needs to be carried out after the TSV fabrication

- Edge Trimming + BONDING

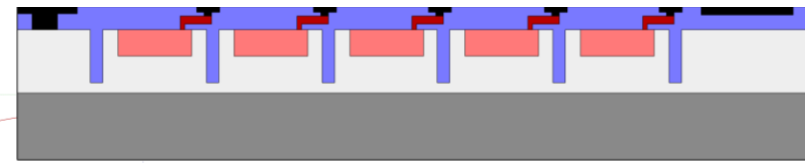


- THINNING



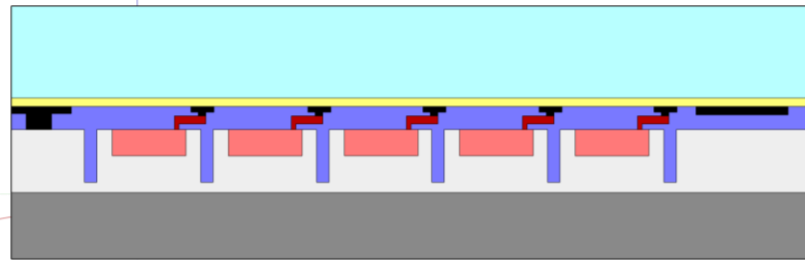
Via Last

- SiPM fabrication

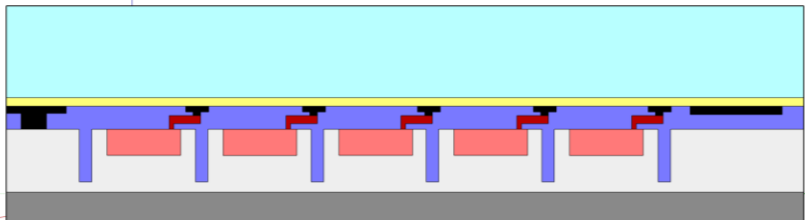


Front end of line is unchanged

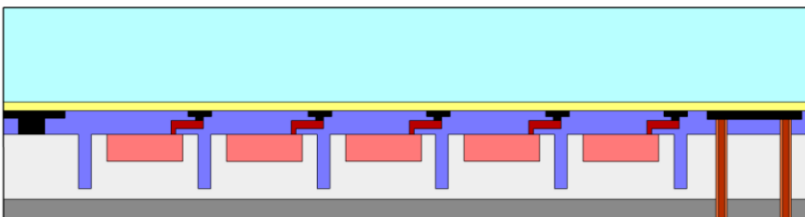
- Edge Trimming + BONDING



- THINNING

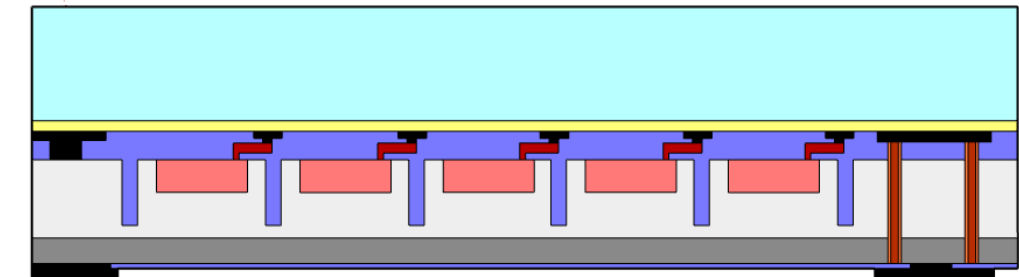


- TSV formation

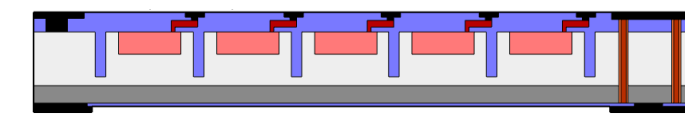


Low thermal budget allowed during the TSV formation at the back end of line

- Contacts formation

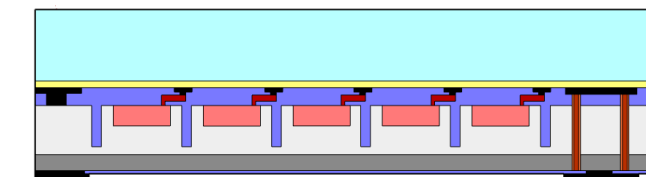


- DEBONDING

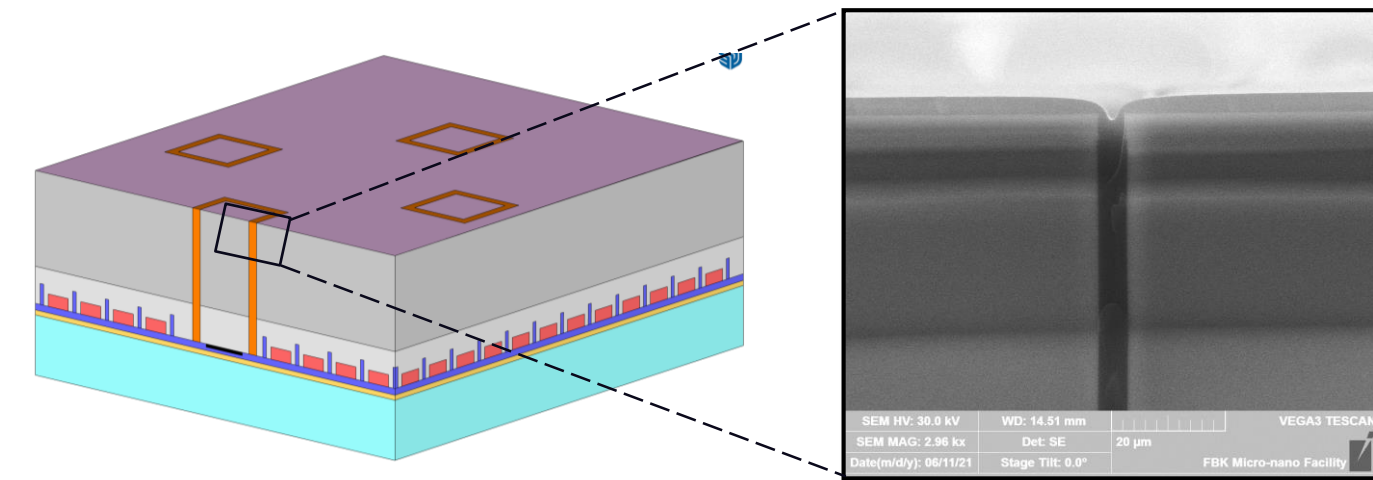


Thickness at least 150 um

- NO-DEBONDING



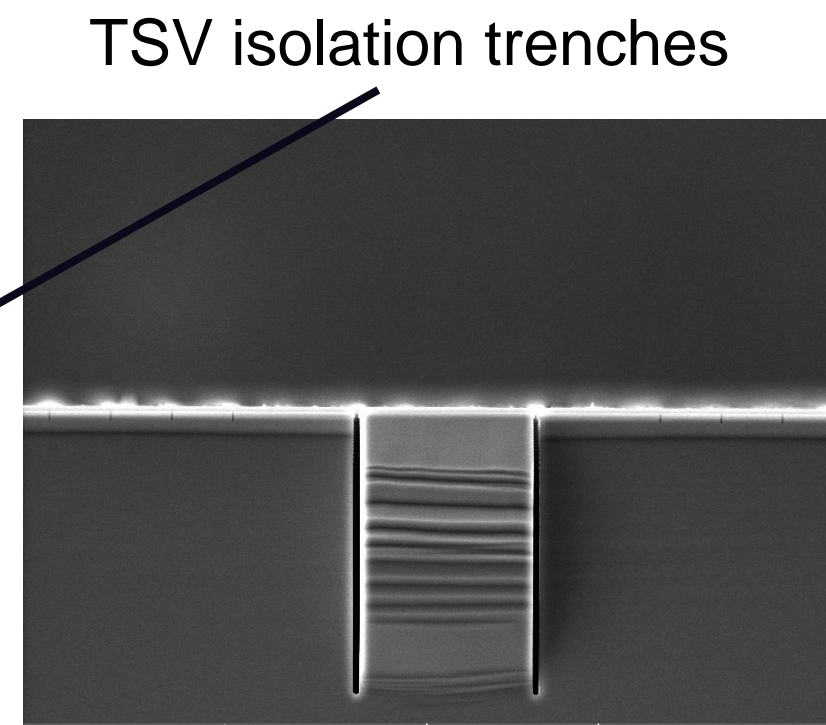
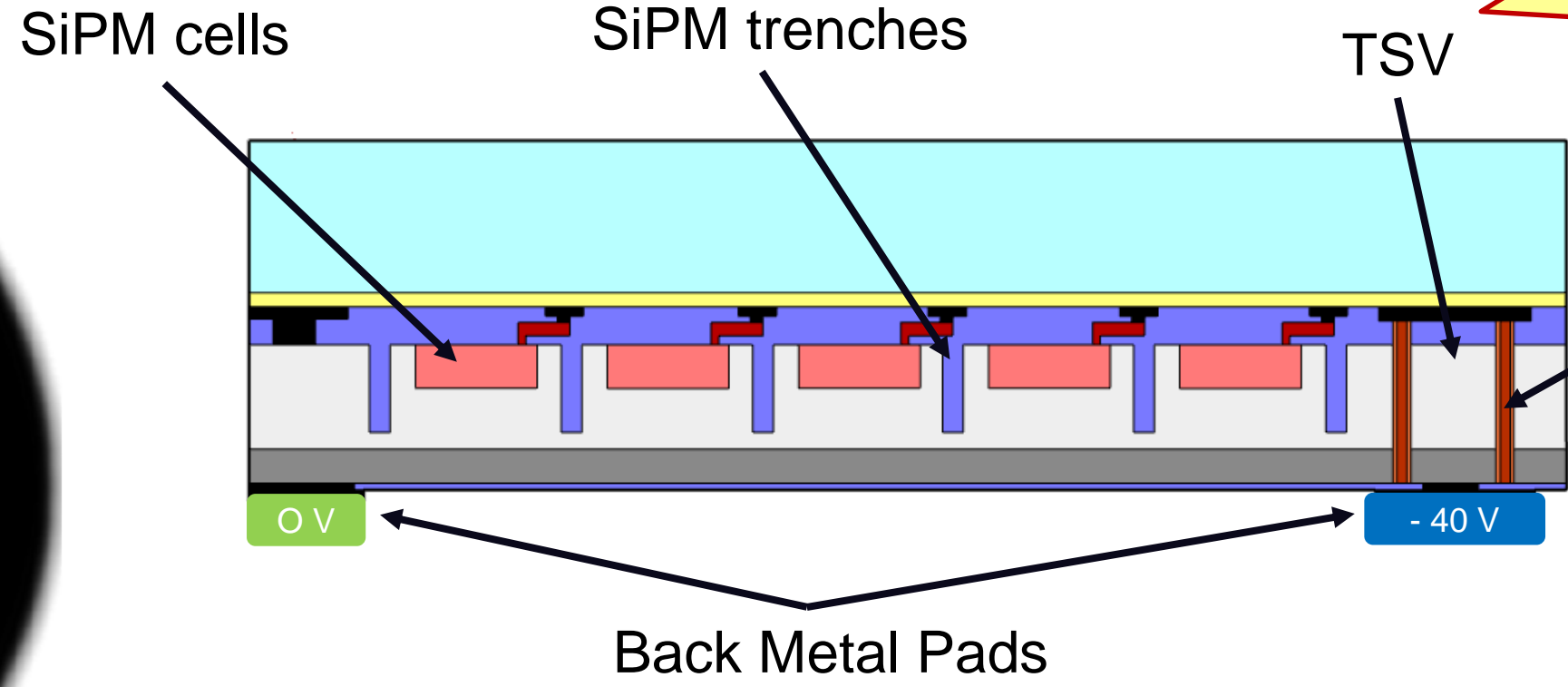
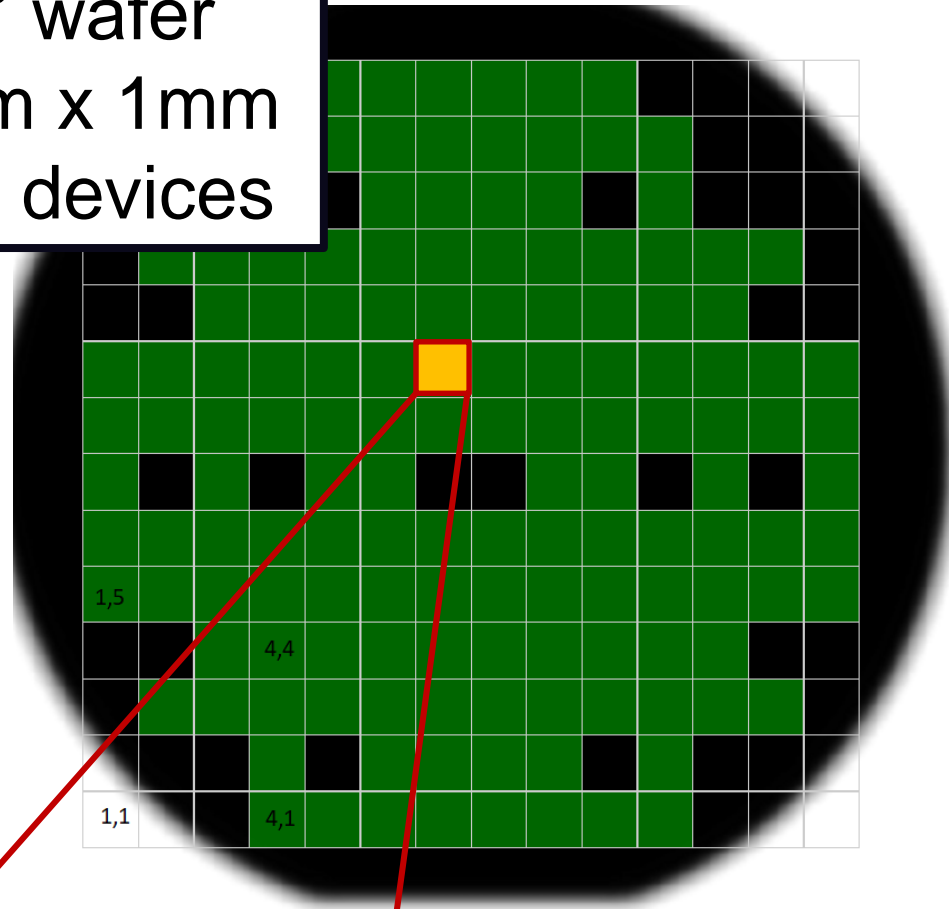
Thickness 10-50 um



SiPM with TSV for VUV/NUV – Via Mid

Silicon thickness: 150 μm

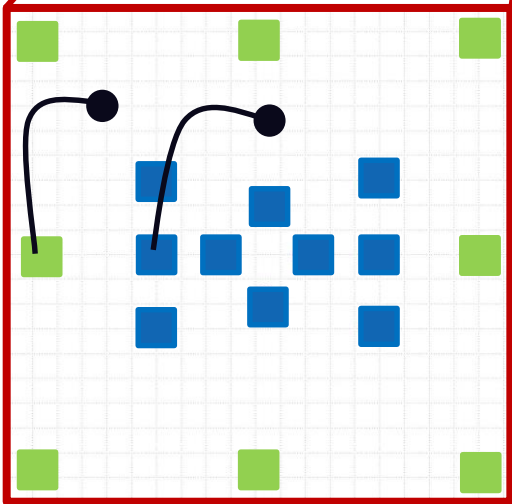
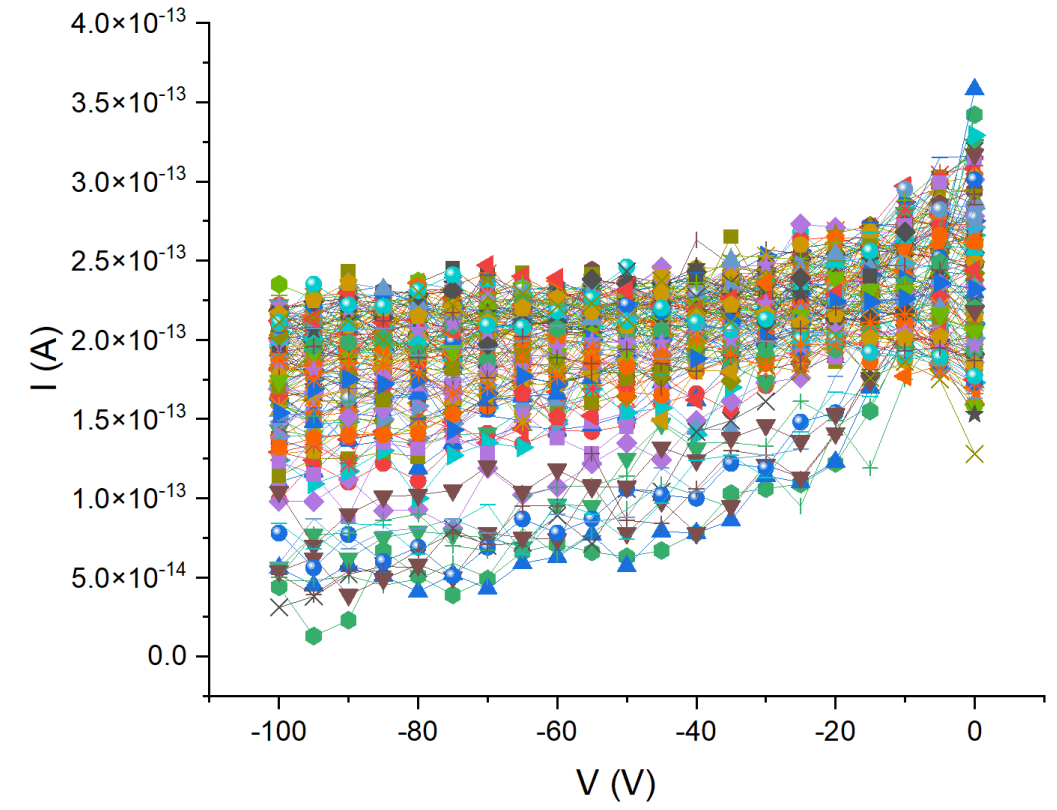
6" wafer
1 mm x 1mm
142 devices



At **-100 V** of bias applied the intensity varies from **30 to 200 fA**



Trough Silicon Vias – Via Mid are isolated from the bulk silicon contact



■ Silicon bulk pad
■ TSV pad

Back side of the SiPM



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Conclusions

- FBK is working on 3D-integration approaches to develop **Hybrid SPAD arrays/SiPM** in the framework of IPCEI Microelectronic project

Back Side Illuminated SiPM for NIR detection

- **95% of yield** for SiPM with **10 um silicon thickness** were realized and an increase of the PDE at 900 nm for BSI NIR SiPM with metal reflectors compared with the FSI technology was measured

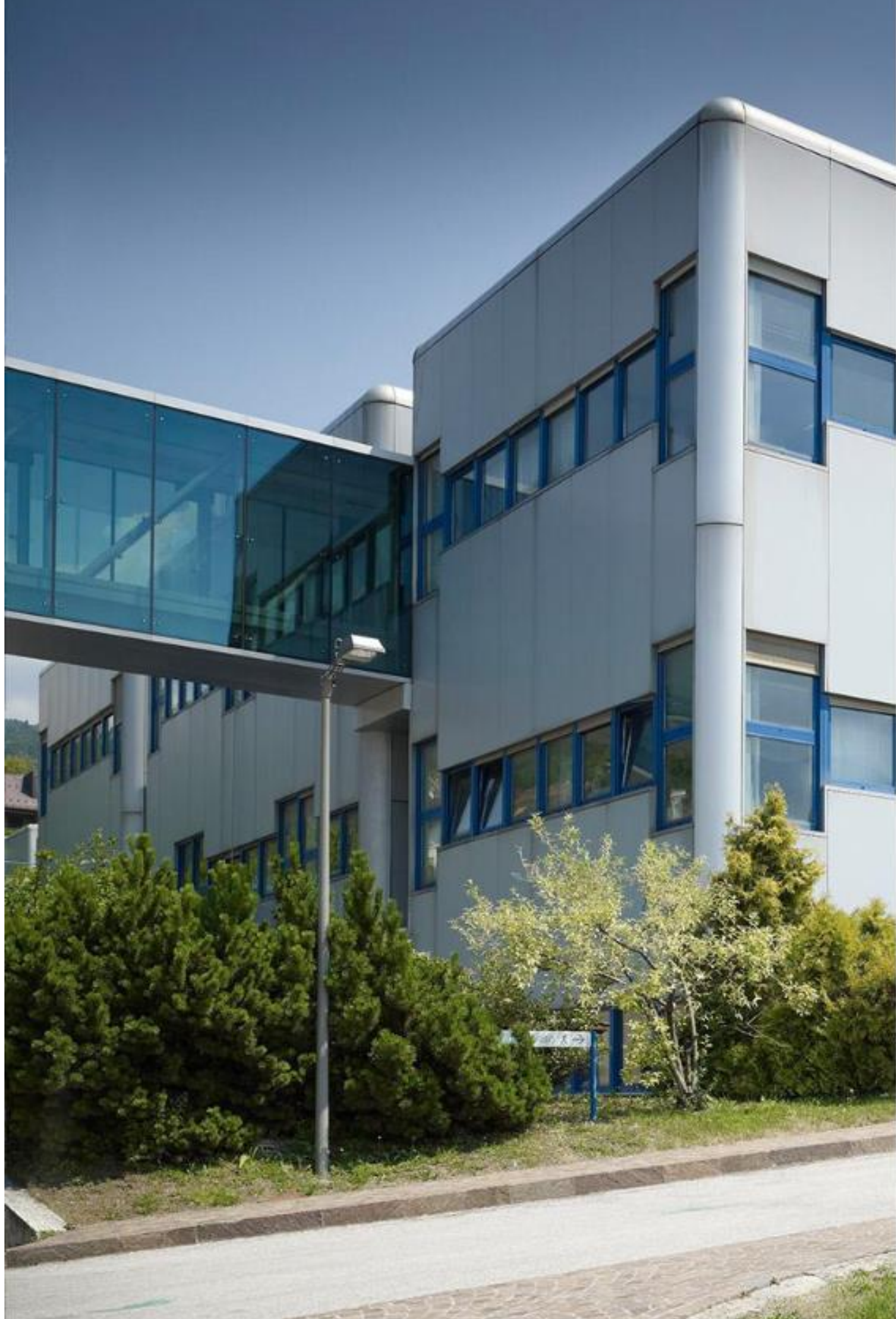
Trough Silicon Vias interconnections for VUV/NUV SiPM

- Preliminary results on the **Via Mid** approach show good quality and yield regarding the TSV isolation
- Thanks to the no limitation on thermal budget we have been able to use high quality and conformal materials for a proper TSV isolation leading to a very **robust process flow**

Ongoing and future work

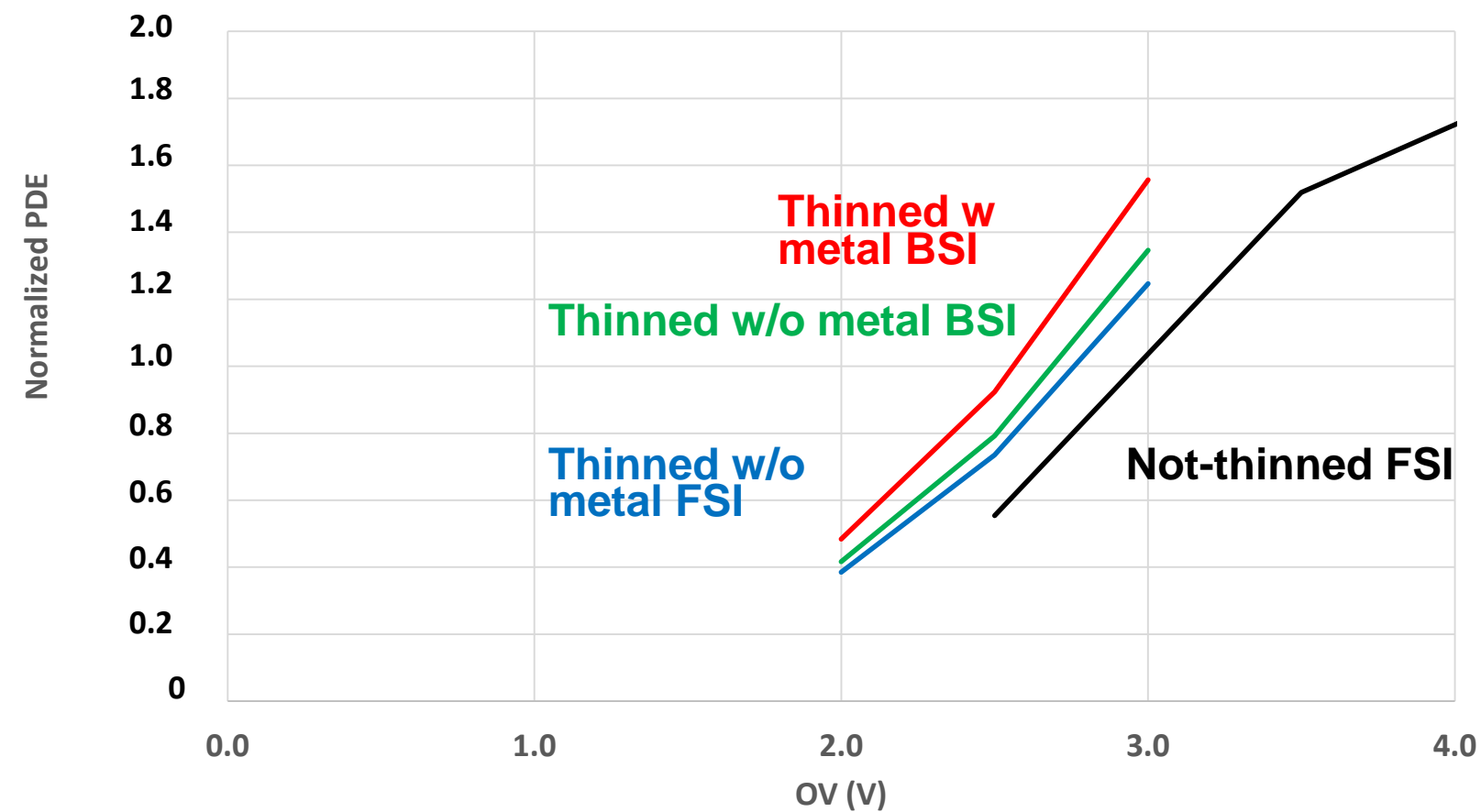
- Improved SiPM BSI for NIR detection are currently being fabricated with new p-n junction configurations and new bonding process
- TSV Via Last are being realized and the TSV resistance will be measured

Thank you



Results on BSI SiPM for NIR

PDE measurements



Type	Normalized PDE @ 905 nm 3V OV
Ref. not thinned	1 (normalized)
Thinned no metal FSI	+ 24%
Thinned no metal BSI	+ 34%
Thinned metal BSI	+ 50%