Development of TimePix4 Readout for Experiments at Synchrotrons and FELs

J. Correa, S. Fridman, H. Graafsma, A. Ignatenko, S. Lange, D. Pennicard, S. Smoljanin

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HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

DESY.

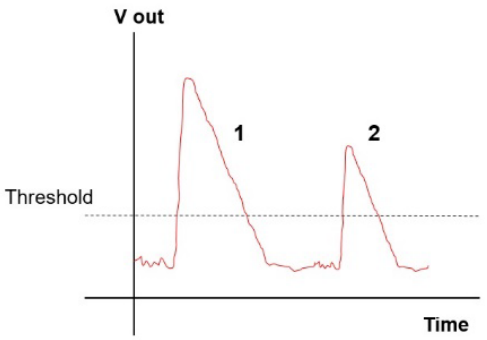
Overview

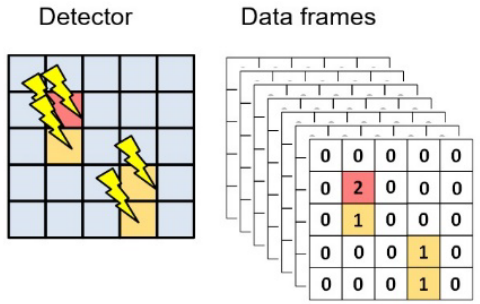
- Comparison with TimePix3 and MediPix3
- Potential applications of TimePix4
- Single-chip system with high-speed readout
- Long-term plans – multi-chip systems

Frame-based & data-driven readout

Frame-based

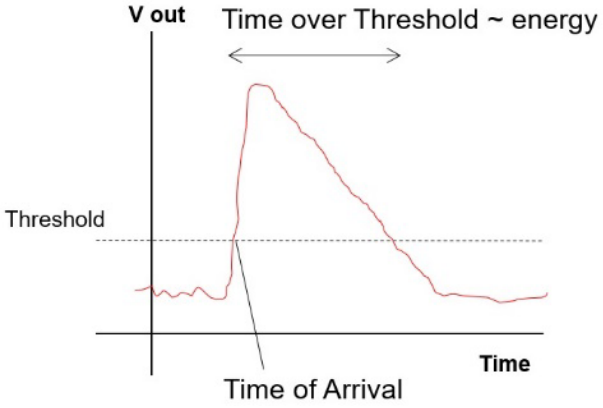
- Single threshold
- Frame rate up to 40 kHz, 8/16 bit depth
- 5×10^9 hits/mm^2/s

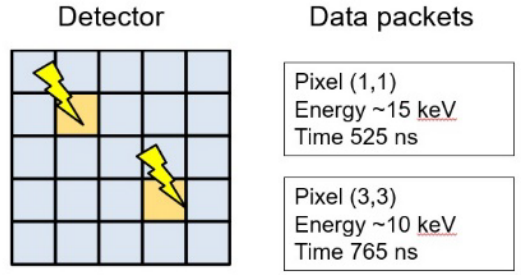




Data-driven

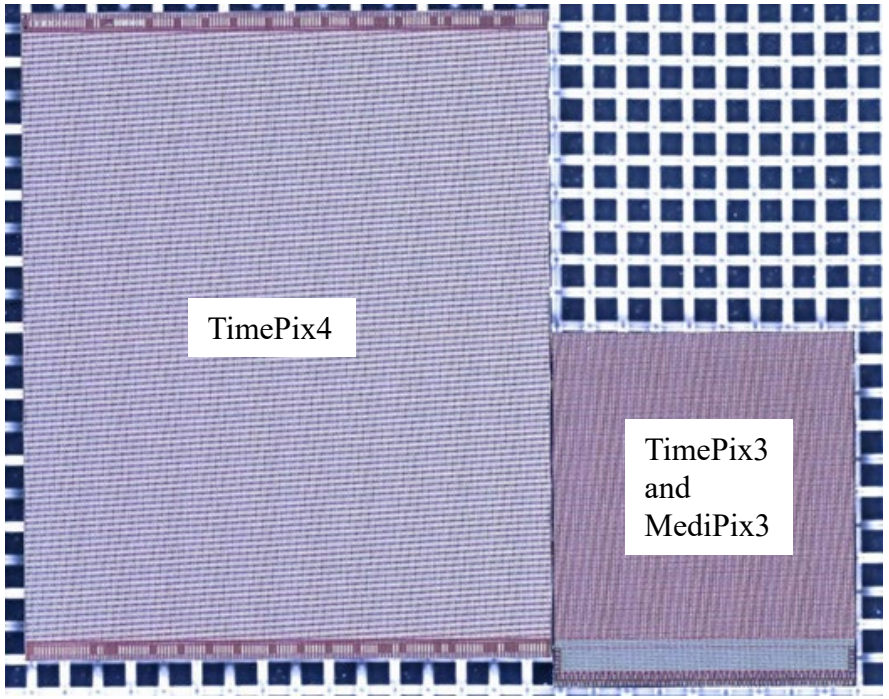
- Time of Arrival (ToA) with time resolution up to 200 ps (sensor dependent, ~ 5 ns for X-rays with 300 µm thick Si sensor)
- Time over Threshold (ToT) with ~1 keV resolution
- Max hit rate 2.48×10^9 hits/s, active area 6.94 cm^2





TimePix4 vs MediPix3 and TimePix3

	MediPix3	TimePix3	TimePix4
Tech. node, nm	130	130	65
Year	2013	2014	2019
Pixel size, µm	55	55	55
Pixels	256 × 256	256 × 256	448 × 512
Time resolution	N/A	1.6 ns	195 ps
Readout architecture	Frame-based (sequential or continuous R/W)	Data-driven or frame-based (sequential R/W)	Data-driven or frame-based (sequential or continuous R/W)
Number of sides for tiling	3	3	4



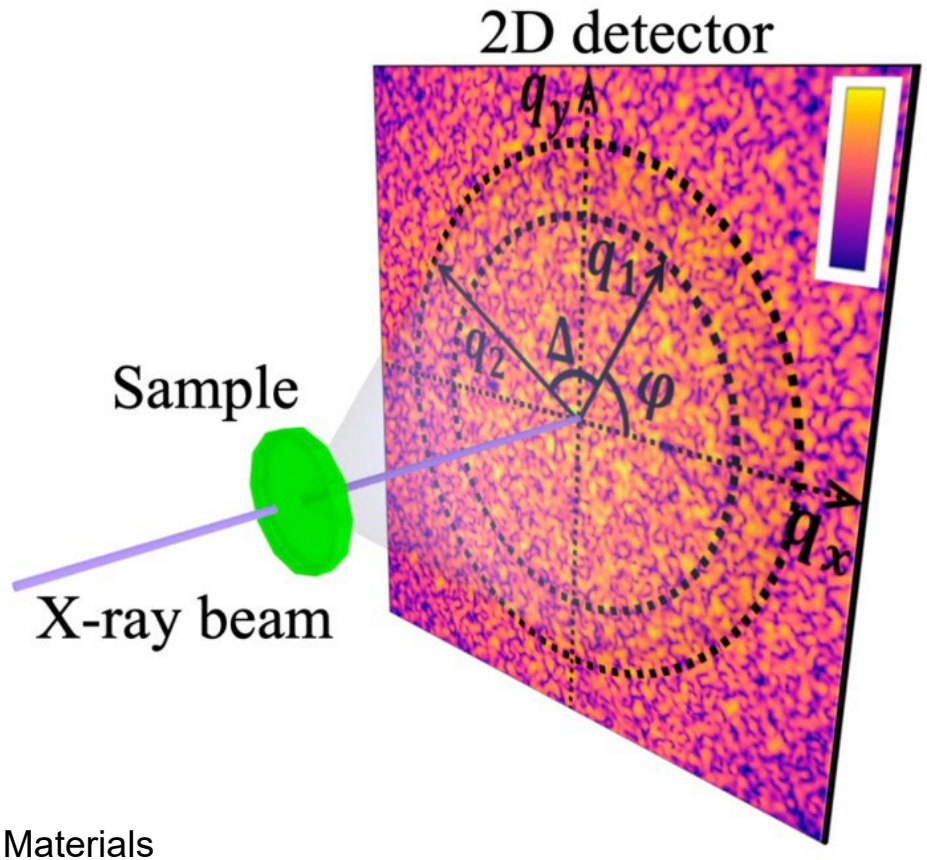
TimePix4 vs TimePix3

			Timepix3 (2013)	Timepix4 (2019)	
Technology			130nm – 8 metal	65nm – 10 metal	
Pixel Size			55 x 55 µm	55 x 55 µm	
Pixel arrangement			3-side buttable	4-side buttable	
			256 x 256	512 x 448	3.5 x
Sensitive area			1.98 cm^2	6.94 cm^2	
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA		
		Event Packet	48-bit	64-bit	
		Max rate	0.43x10^6 hits/mm^2/s	**3.58x10^6 hits/mm^2/s**	8 x
		Max Pix rate	1.3 KHz/pixel	**10.8 KHz/pixel**	
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)	
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)	
		Max count rate	~0.82 x 10^9 hits/mm^2/s	~5 x 10^9 hits/mm^2/s	6 x
TOT energy resolution			< 2KeV	**< 1Kev**	2 x
TOA binning resolution			1.56ns	**195ps**	8 x
TOA dynamic range			409.6 µs (14-bits @ 40MHz)	**1.6384 ms** (16-bits @ 40MHz)	
Readout bandwidth			≤5.12Gb (8x SLVS@640 Mbps)	**≤163.84 Gbps (16x @10.24 Gbps)**	32 x
Target global minimum threshold			<500 e^-	<500 e^-	

Potential applications for TimePix4

Existing applications of Medipix3 can benefit from the improved photon counting mode (~ **6** times faster)

- Small-angle X-ray scattering (SAXS)
- Wide-angle X-ray scattering (WAXS)
- Powder diffraction
- Crystallography



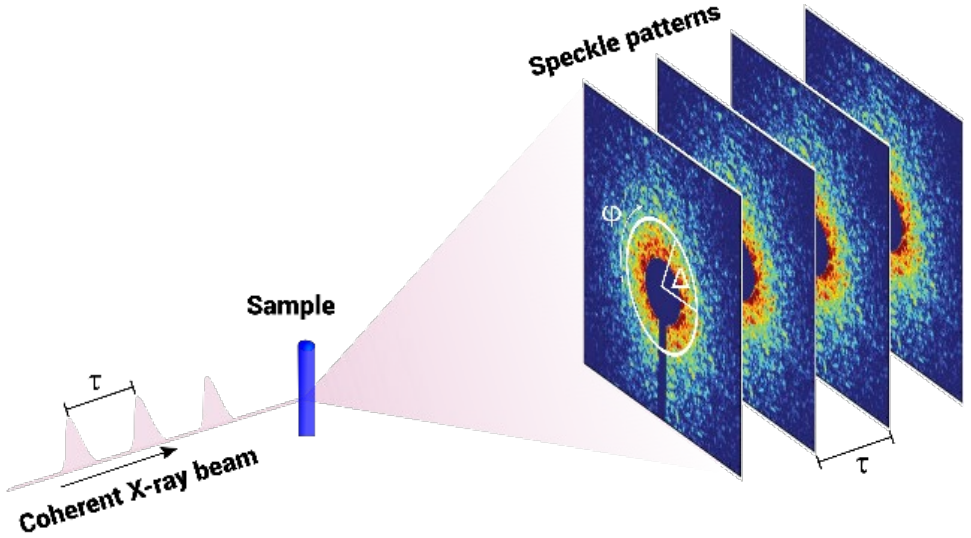
I. Zaluzhnyy et al, Materials 12(21), 3464, 2019

Potential applications for TimePix4

TimePix4 can replace its predecessor TimePix3

Correlation experiments: X-ray photon correlation spectroscopy (XPCS), X-ray cross-correlation analysis (XCCA)

- aim for increasingly high time resolution with higher frame rates
- small amount of pixels have signal, would be more efficient to timestamp each photon



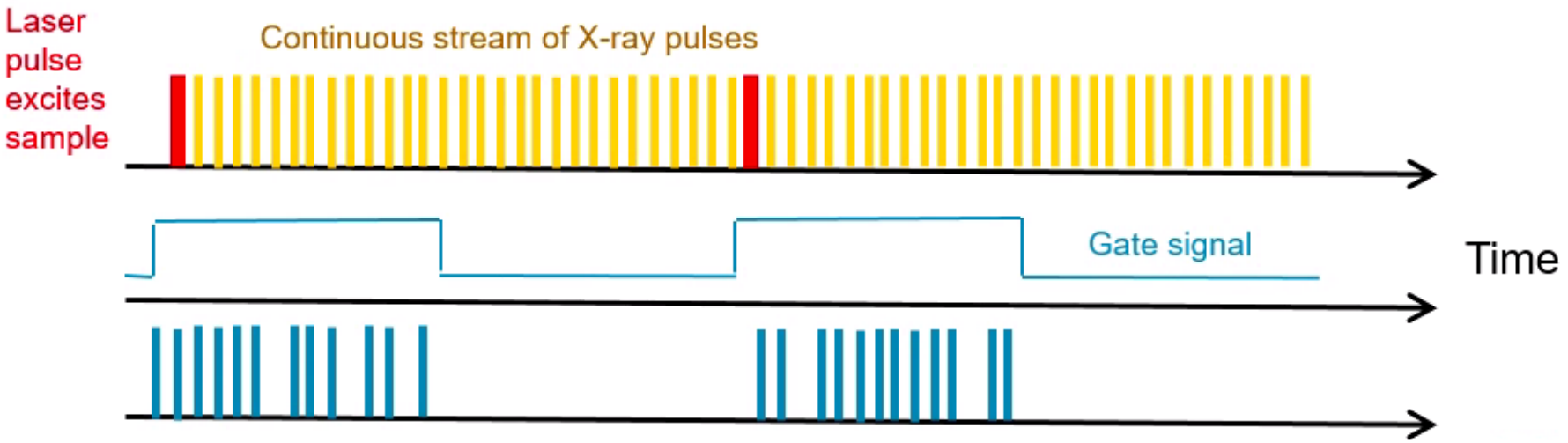
Time-resolved experiments with single-bunch time resolution (>4 ns) at the PETRA IV Storage Ring Facility

Potential applications for TimePix4

TimePix4 can replace its predecessor TimePix3

Pump-probe diffraction experiments at FELs

- Timestamping could allow to measure the full time series simultaneously

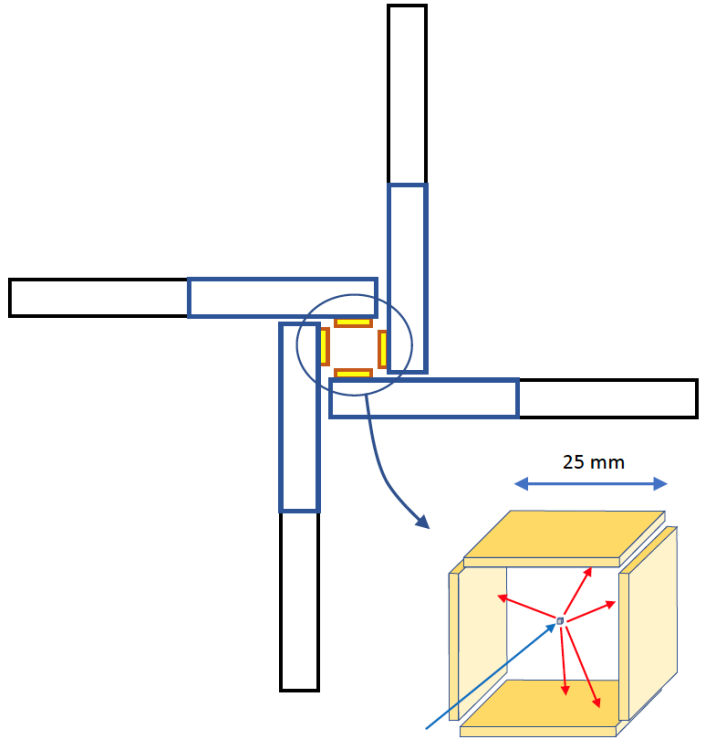


Potential applications for TimePix4

New applications, e.g. quantum imaging

- ~1 keV energy resolution
- High-Z material sensor (e.g. CdTe) to increase quantum efficiency
- Improved timing capability and time resolution
- Coverage of large solid angle

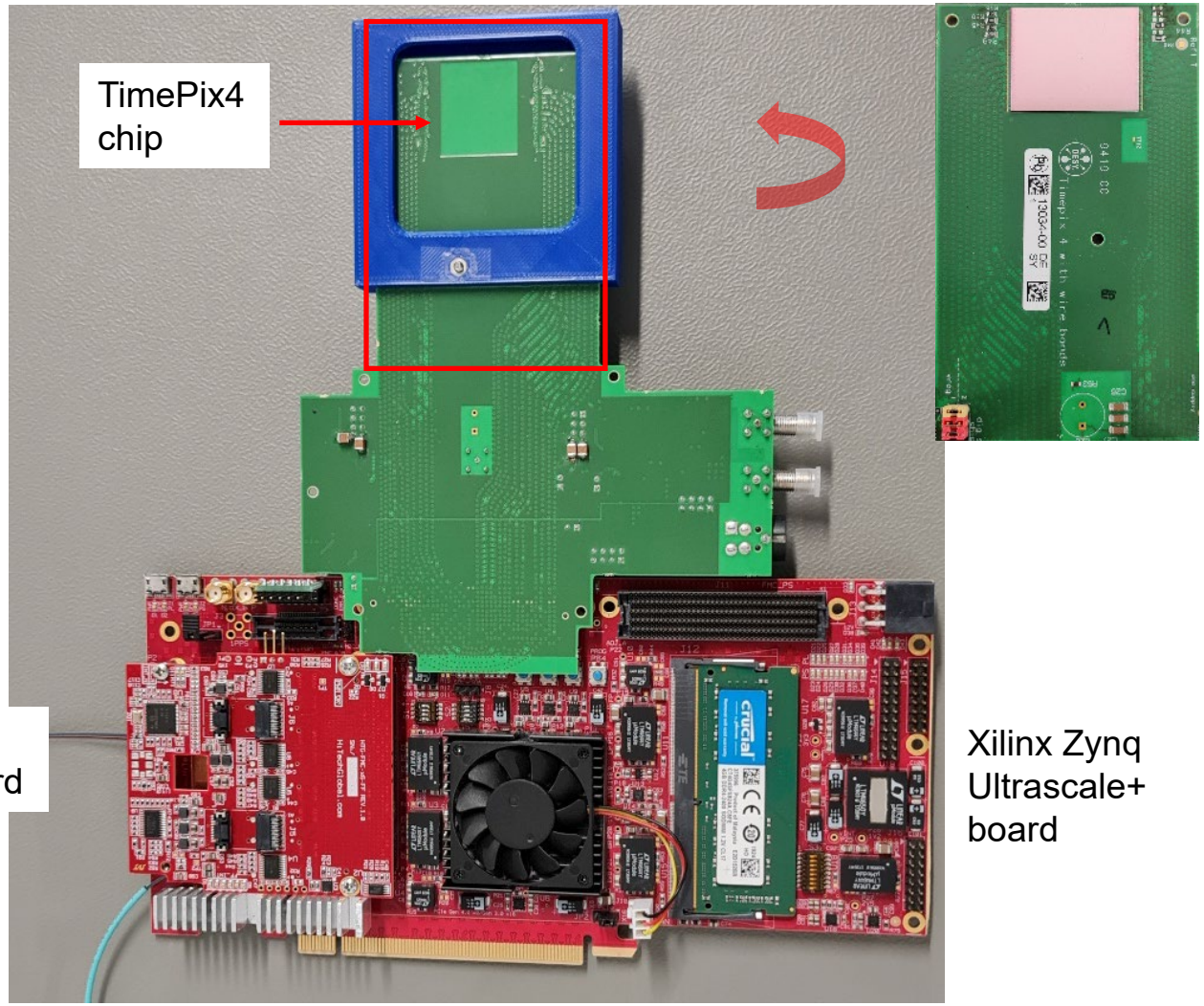
“Correlated X-ray photons for incoherent diffraction imaging” June 28, 15:30



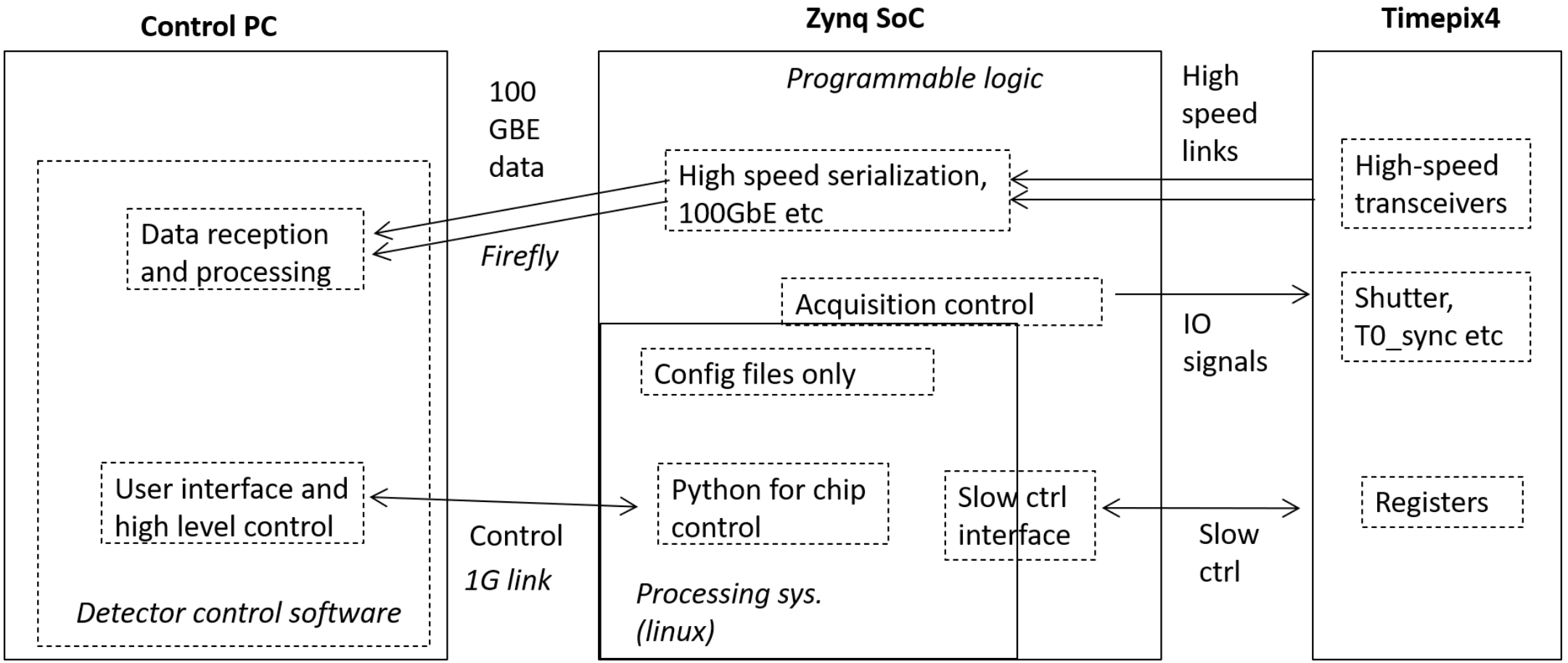
Single-chip system with high-speed readout

Single-chip system development

- custom TimePix4 board
- Xilinx Zynq Ultrascale+ board with FPGA fabric
- high-speed readout (up to 160 Gbit/s – 16 high-speed links from chip), daughterboard with Firefly optical output

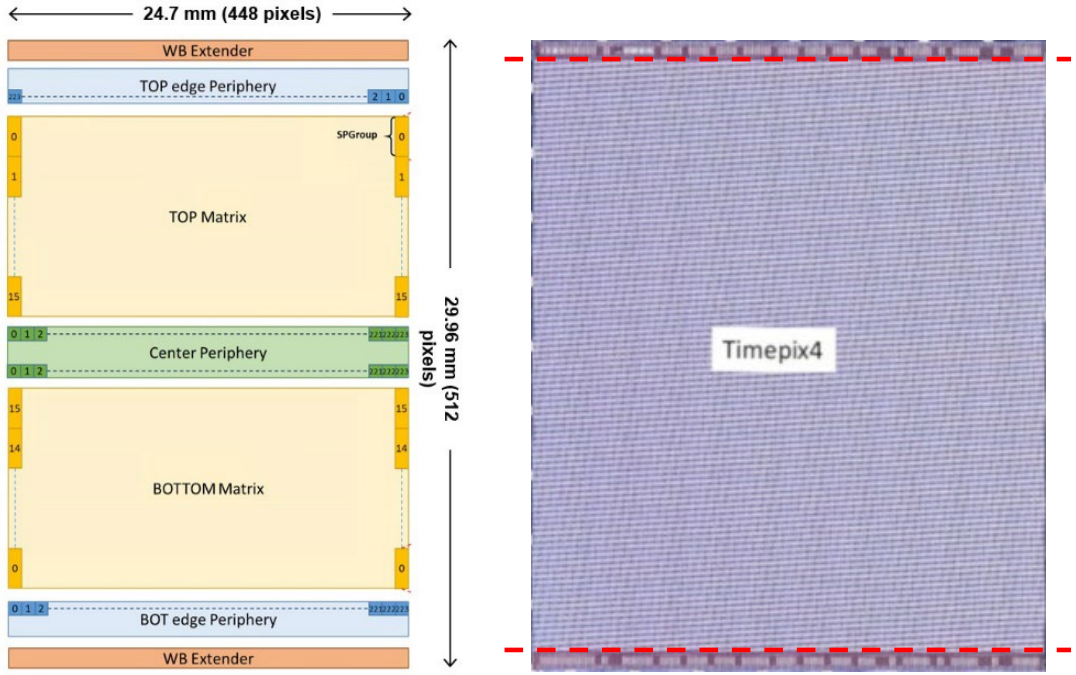


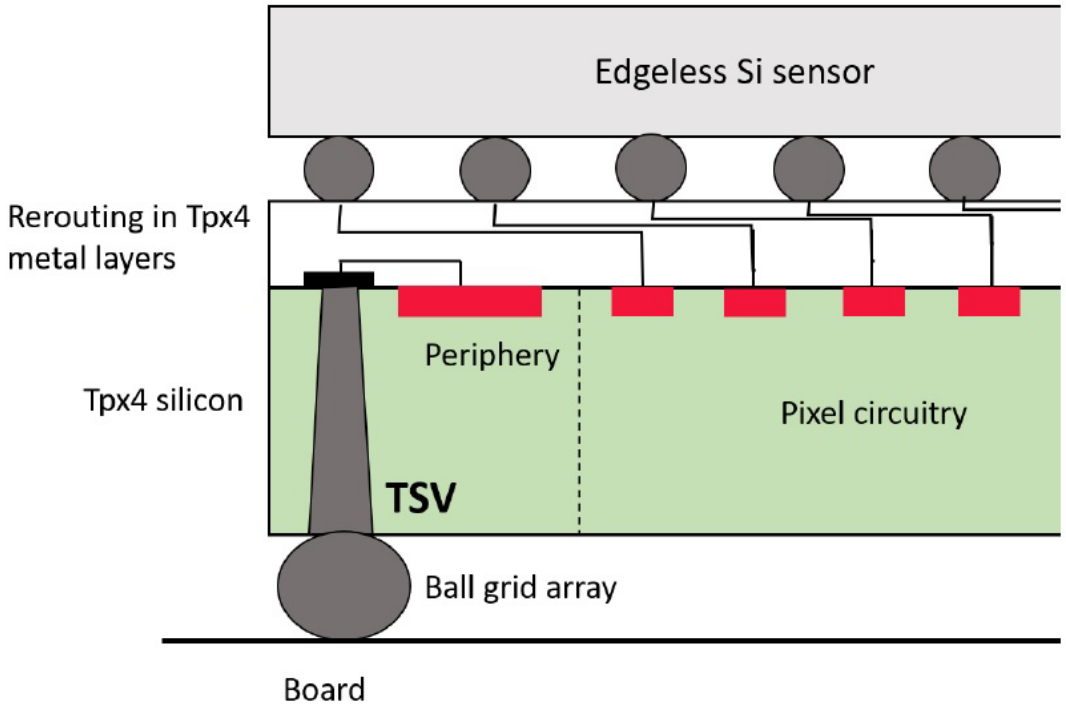
Firmware and software



4-side buttable design with Through Silicon Vias (TSV)

- With TSVs full chip surface is covered with pixels
- Wire bond pads can be diced off

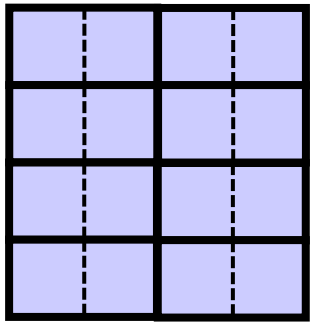


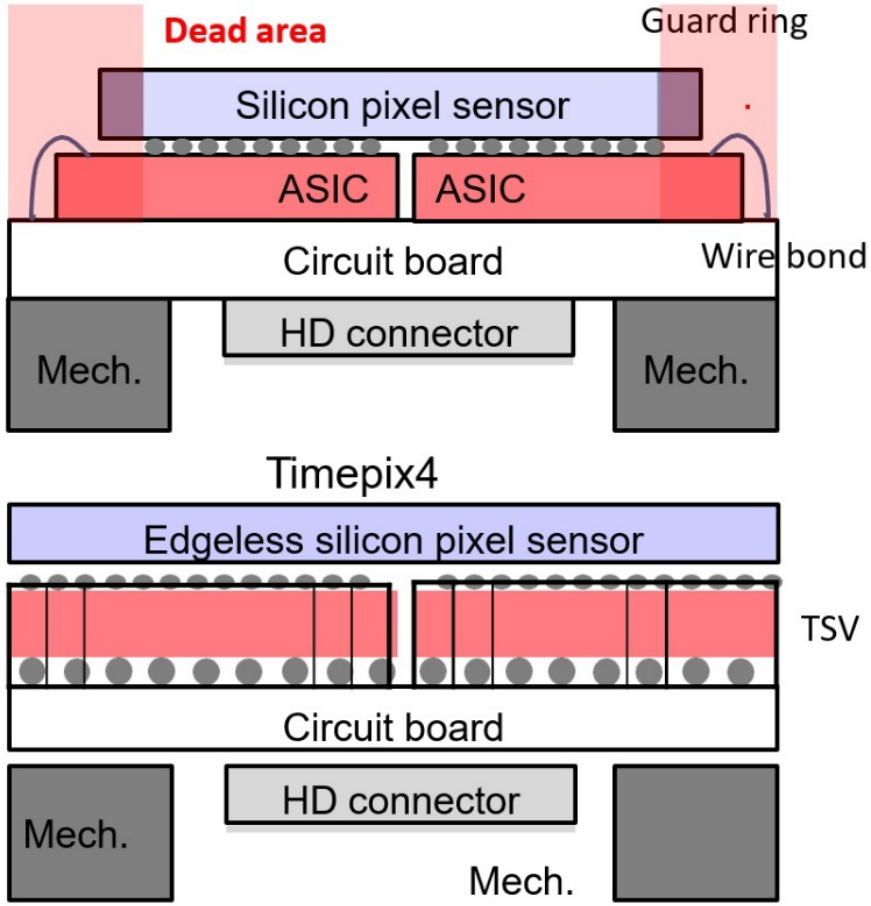


Tilable modules

- With TSVs full chip surface is covered with pixels
  - rerouting in metal layers creates space for periphery
  - improvements of TSV design

Tiled multi-chip detector



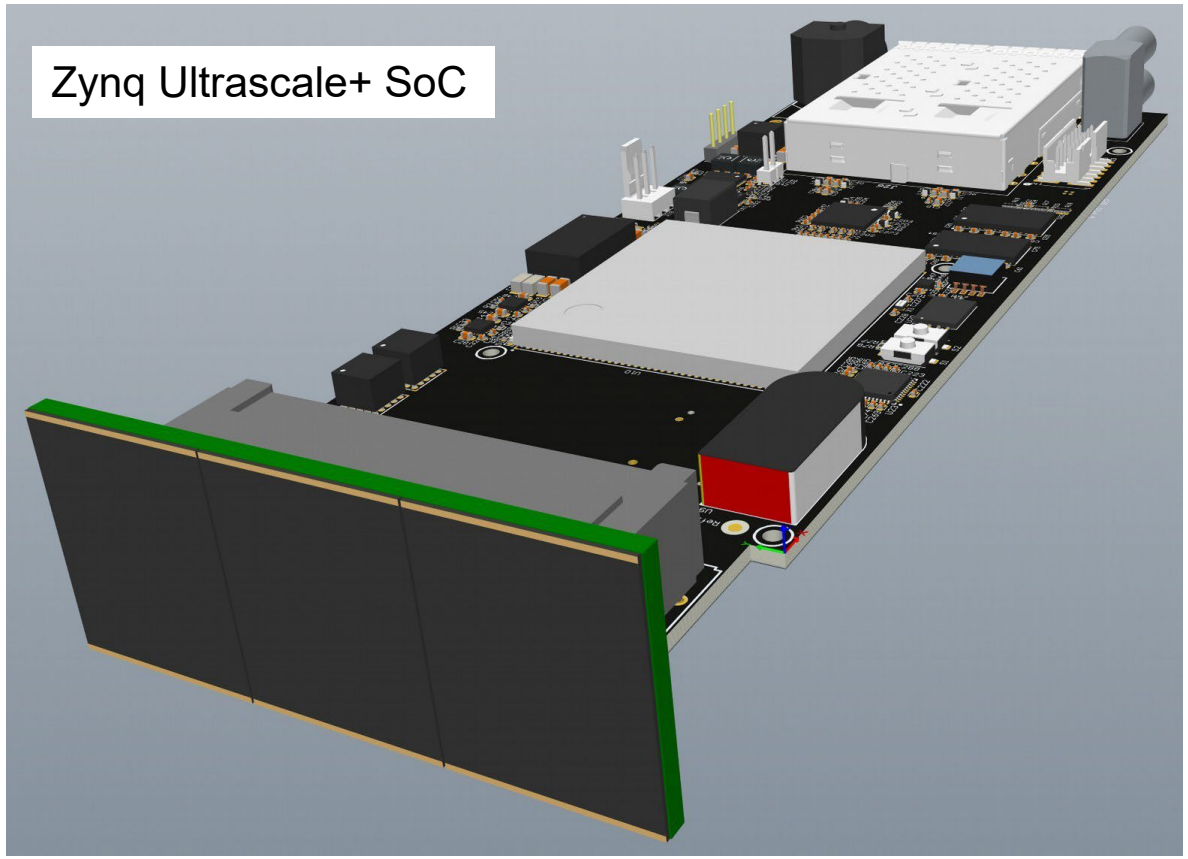


Large systems with tilable modules

Need for large continuous detector

- TSV to eliminate wire bonds
- Tilable building block: 3-chip module
- Readout boards with Zync Ultrascale+ SoC,
  3 × 100 GbE readout

4 × 100 GbE cages



3-chip detector head
1344 × 512 pixels

Summary

- **Detectors with TimePix4 chip are able to replace detectors carrying MediPix3 and TimePix3 in their existing applications**
- **Improved time resolution can be beneficial for some new applications for detectors with TimePix4 chip**
- **Single-chip system with high-speed readout is under development**
- **Long-term plans – multi-chip systems**

Thank you for your attention!