Quality Control (QC) of FBK 3D Si Sensors from the ATLAS ITk Preproduction

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INFN

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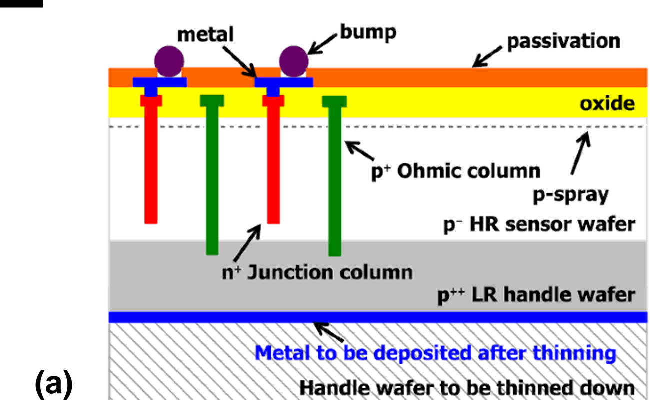
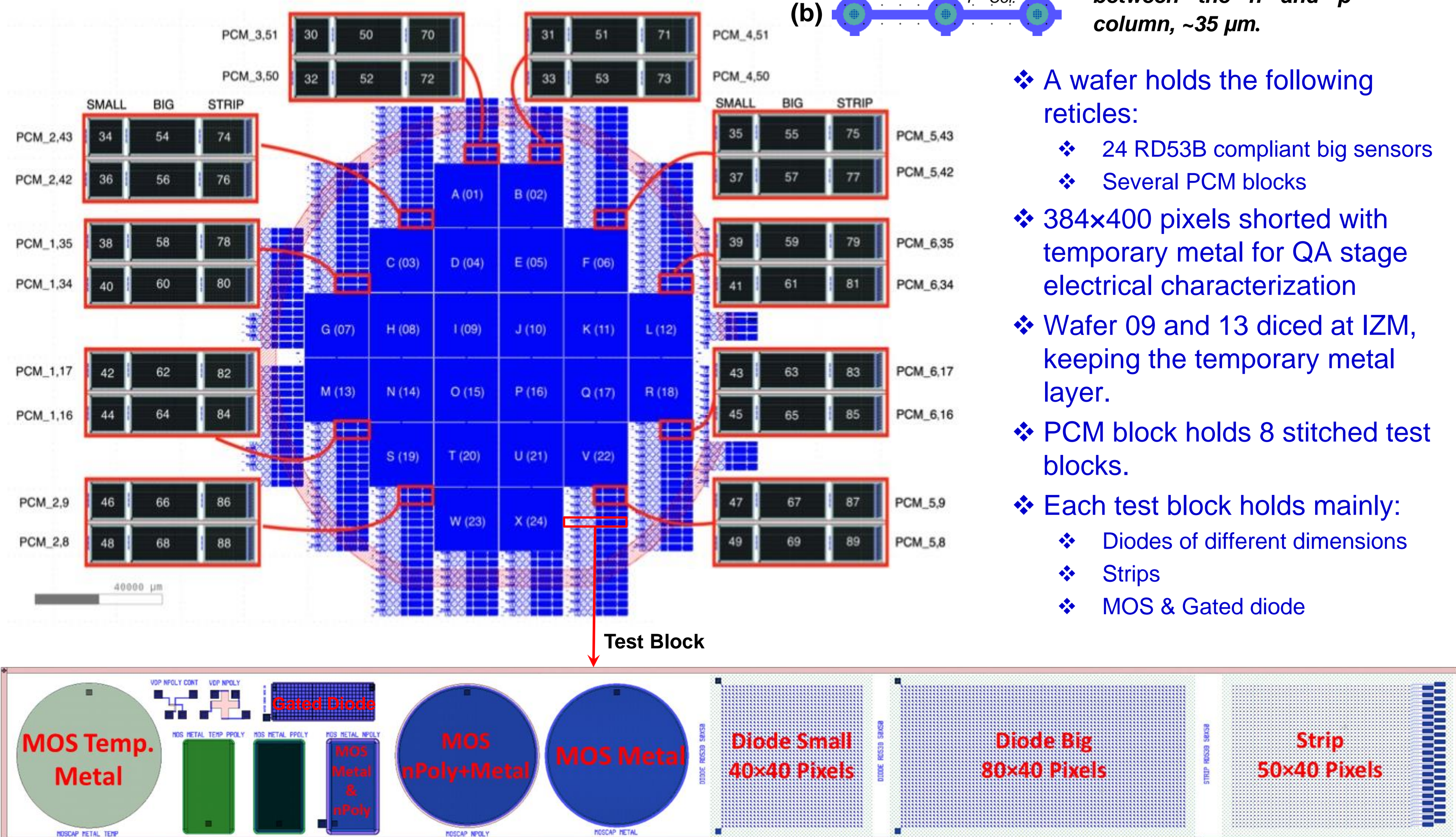
Preface

- Fabricated on Si-Si wafer, having high resistive active thickness ~150 μm.
- Both N+ and P+ columns filled with Poly-Si
- N+ column kept ~25 μm away from the low resistive substrate. (*higher breakdown*)
- Finally, the sensor will have to be thinned and back metalized (*note: probing candidates have not been thinned and metalized*)
- A few QC requirements for qualifying sensors:
  - Leakage current below 2.5 μA/cm²
  - Depletion Voltage (V_{depl}) is less than 10 V
  - Breakdown Voltage : V_{depl} + 20 V



(b)

Figure 1: (a) A cross schematic (not to scale), and (b) a micrograph of 50×50 um² layout geometry. 'L' denotes the interelectrode distance between the n and p column, ~35 μm.



- A wafer holds the following reticles:
  - 24 RD53B compliant big sensors
  - Several PCM blocks
- 384×400 pixels shorted with temporary metal for QA stage electrical characterization
- Wafer 09 and 13 diced at IZM, keeping the temporary metal layer.
- PCM block holds 8 stitched test blocks.
- Each test block holds mainly:
  - Diodes of different dimensions
  - Strips
  - MOS & Gated diode

Figure 2: A wafer layout details.

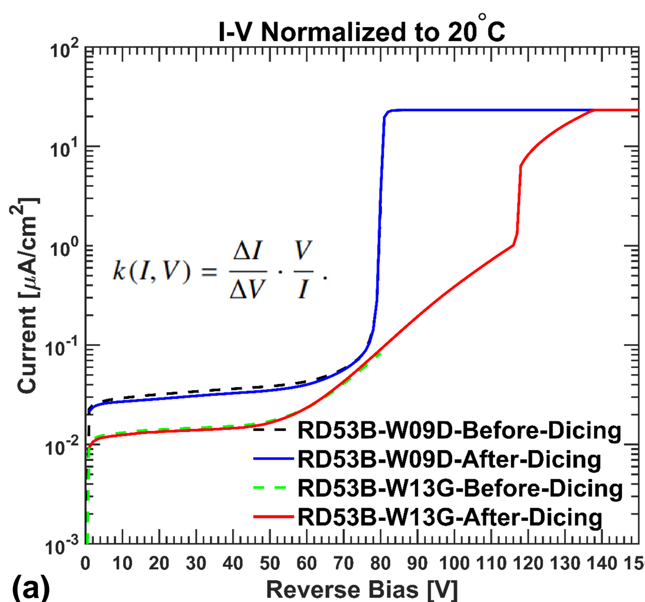
Trento Probing Setup

Figure 3: Experimental setup.

- A manual probing station and Keithley 4200 SCS analyzer were used to acquire probing data.
- Sensirion SHT4x sensor and SEK bridge were used for logging temperature and humidity.
- No dry-air supplied.
- No temperature-dependent measurements were performed.

QC Results

Leakage Current



(b) DEVICE LEAKAGE CURRENT [A] @ Vrev = 30V

Dev ID	Leakage [A]	VBD [V]	GOOD?
A_3,6	1.26E-07	96.0	Y
B_4,6	1.00E-04	4.0	N
C_2,5	1.52E-07	62.0	y
D_3,5	1.49E-07	72.0	Y
E_4,5	1.00E-04	4.0	N
F_5,5	1.00E-04	2.0	N
G_1,4	1.27E-07	67.0	Y
H_2,4	1.00E-04	3.0	N
I_3,4	2.81E-08	52.0	Y
J_4,4	4.43E-08	31.0	Y
K_5,4	1.00E-04	2.0	N
L_6,4	1.00E-04	6.0	N
M_1,3	4.09E-08	67.0	Y
N_2,3	1.00E-04	1.5	N
O_3,3	2.62E-08	54.0	Y
P_4,3	2.57E-08	51.0	Y
Q_5,3	1.00E-04	4.0	N
R_6,3	1.00E-04	4.0	N
S_2,2	3.01E-08	61.0	Y
T_3,2	3.09E-08	56.0	Y
U_4,2	1.00E-04	4.0	N
V_5,2	5.18E-08	63.0	Y
W_3,1	1.00E-04	4.0	N
X_4,1	3.39E-08	62.0	Y

(c) DEVICE LEAKAGE CURRENT [A] @ Vrev = 30V

Dev ID	Leakage [A]	VBD [V]	GOOD?
A_3,6	1.00E-04	12.0	N
B_4,6	1.00E-04	4.0	N
C_2,5	1.00E-04	1.5	N
D_3,5	1.00E-04	3.0	N
E_4,5	1.00E-04	4.5	N
F_5,5	1.00E-04	0.5	N
G_1,4	6.09E-08	66.0	Y
H_2,4	1.00E-04	5.0	N
I_3,4	1.00E-04	3.0	N
J_4,4	1.00E-04	3.0	N
K_5,4	1.33E-07	79.0	Y
L_6,4	1.18E-07	64.0	Y
M_1,3	1.00E-04	0.5	N
N_2,3	1.00E-04	17.0	N
O_3,3	1.00E-04	3.0	N
P_4,3	1.00E-04	2.0	N
Q_5,3	9.23E-08	67.0	Y
R_6,3	1.82E-07	75.0	Y
S_2,2	3.67E-08	58.0	Y
T_3,2	1.15E-07	75.0	Y
U_4,2	2.98E-08	57.0	Y
V_5,2	1.00E-04	3.0	N
W_3,1	6.29E-08	65.0	Y
X_4,1	1.00E-04	4.0	N

Figure 4: (a) I-V plot of RD53B sensors before and after dicing, and I-V summary: (b) W09 after dicing and (c) W13 after dicing

- RD53B sensors report similar leakage before and after dicing.
- Good sensors (green) show breakdown voltage around 60V, where k(I,V) = 4.
- W13 yield drops to 38% (it was 50% at wafer level) due to dicing-stage driven edge-microcracks and surface damages.

Leakage Stability

- Leakage was observed for 48 hours for the same RD53B reticles for an applied reverse bias of 30V.
- Leakage fluctuation remains below 10%.

$$\frac{max\,(I) - \min(I)}{average(I)}$$

- The logged temperature was ~20.5 ± 1 °C, and the relative humidity was 19.6 ± 3.1 %.

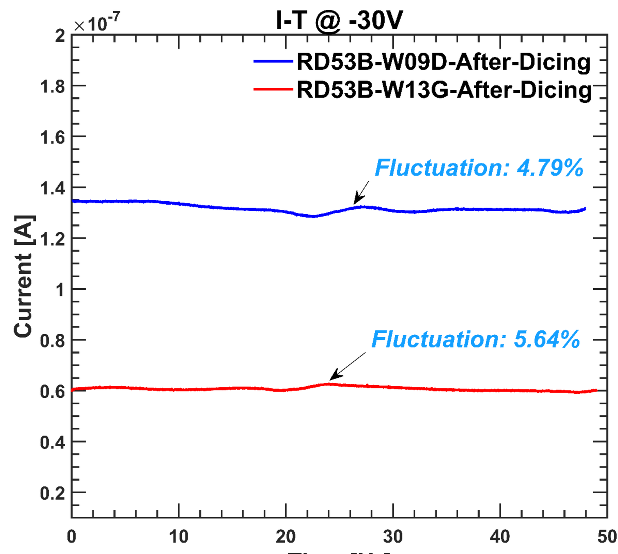
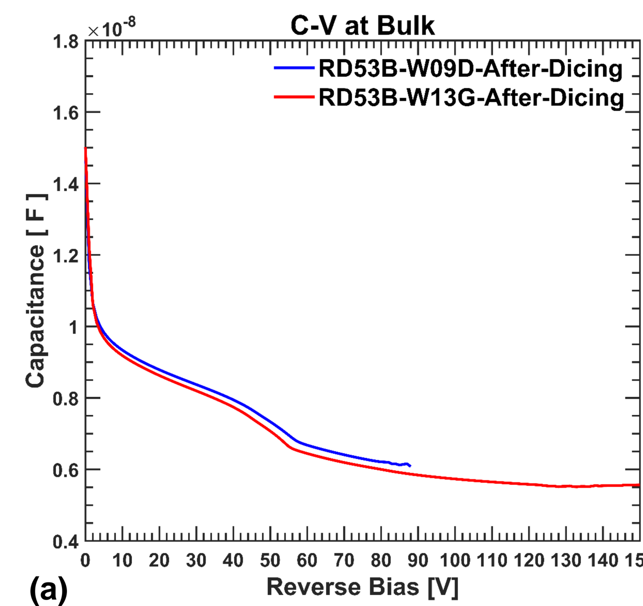


Figure 5: Leakage stability .

Bulk Capacitance



(b) Depletion Details

Dev ID	Lateral Depletion [V]	Depl. Underneath n-tip [V]	GOOD?
A_3,6	2.00	59.0	Y
B_4,6	--	--	N
C_2,5	2.00	61.0	y
D_3,5	2.00	58.0	Y
E_4,5	--	--	N
F_5,5	--	--	N
G_1,4	3.00	58.0	Y
H_2,4	--	--	N
I_3,4	3.00	57.0	Y
J_4,4	3.00	--	Y
K_5,4	--	--	N
L_6,4	--	--	N
M_1,3	3.00	58.0	Y
N_2,3	--	--	N
O_3,3	5.00	50.0	Y
P_4,3	3.00	55.0	Y
Q_5,3	--	--	N
R_6,3	--	--	N
S_2,2	3.00	58.0	Y
T_3,2	3.00	58.0	Y
U_4,2	--	--	N
V_5,2	3.00	58.0	Y
W_3,1	--	--	N
X_4,1	3.00	3.00	Y

(c) Depletion Details

Dev ID	Lateral Depletion [V]	Depl. Underneath n-tip [V]	GOOD?
A_3,6	--	--	N
B_4,6	--	--	N
C_2,5	--	--	N
D_3,5	--	--	N
E_4,5	--	--	N
F_5,5	--	--	N
G_1,4	3.00	57.0	Y
H_2,4	--	--	N
I_3,4	--	--	N
J_4,4	--	--	N
K_5,4	2.00	59.00	Y
L_6,4	3.00	58.00	Y
M_1,3	--	--	N
N_2,3	--	--	N
O_3,3	--	--	N
P_4,3	--	--	N
Q_5,3	3.00	59.00	Y
R_6,3	3.00	57.00	Y
S_2,2	3.00	57.00	Y
T_3,2	3.00	57.00	Y
U_4,2	3.00	58.00	Y
V_5,2	--	--	N
W_3,1	3.00	57.00	Y
X_4,1	--	--	N

Figure 6: (a) Bulk C-V plot of RD53B sensors after dicing, and C-V summary: (b) W09 after dicing and (c) W19 after dicing

- C-V curves of RD53B of the same sensors (as figure 4(a)) reports lateral depletion ~3V.
- A second stage depletion was noticed for all good sensors around ~60V , a complete depletion underneath the n+-column.

Forward Current

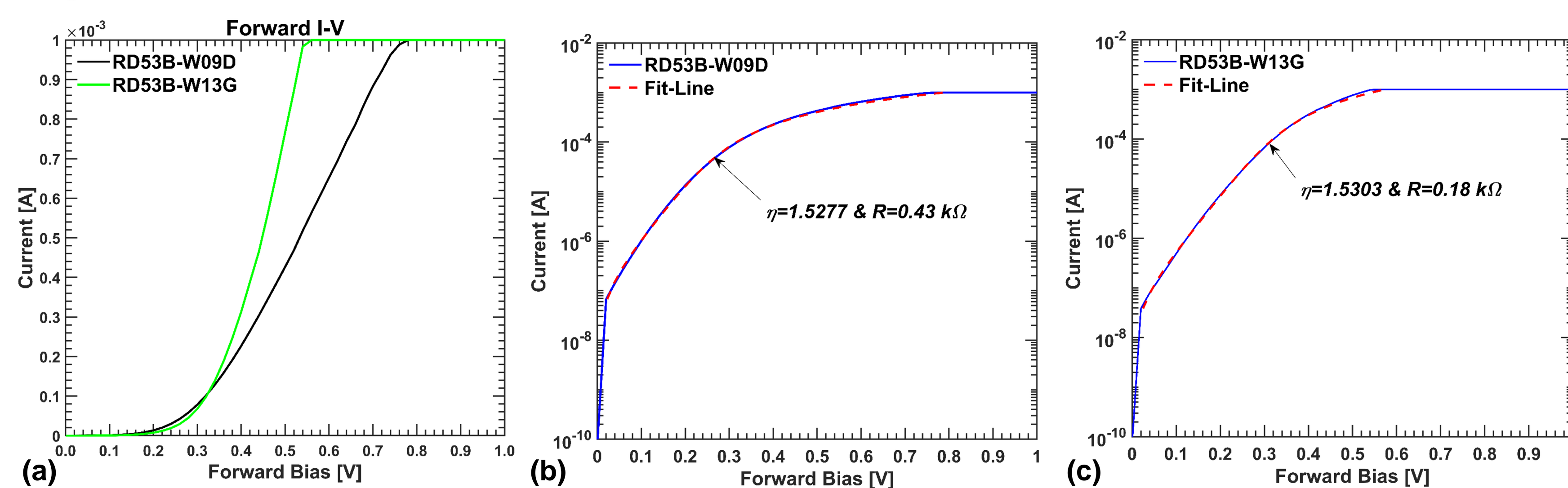


Figure 7: (a) Forward I-V plot of RD53B sensors from both wafers and the numerical model of the parasitic resistance applied on: (b) RD53B-W09D & (c) RD53B-W13G.

- Parasitic resistance 'R' contribution numerically modeled as $f(I_D)$ using MATLAB.
- Starting fit values: Is=1e-14 A, R=100 Ω and η=0.5.
- The model completely fits with the diode measured data for the ideality factor ~1.5.
- The parasitic series resistance presents in the order of several 100 Ω (negligible).

$$I_D = I_S\left[\exp\left(\frac{V_D - (R * I_D)}{\eta V_T}\right) - 1\right]$$

Rearranging,

$$V_D = \eta V_T ln\left[\left(\frac{I_D}{I_S}\right) + 1\right] + RI_D$$

Where, I_S = *Saturation Current* (*typ.* $10^{-15}A$)
V_T = Thermal voltage (0.0254V) at 21 °C
η = *Ideality Factor*
V_D is the applied voltage
I_D is the diode current
R is the parasitic series resistance at bulk

Interpixel Capacitance

- A strip test structure was used to estimate Interpixel capacitance.
- Applied AC signal : 10 kHz, 100 mV.
- Additional floating neighboring strips can add a 10% contribution more to measured data.
- Interpixel capacitance is ~4 fF.

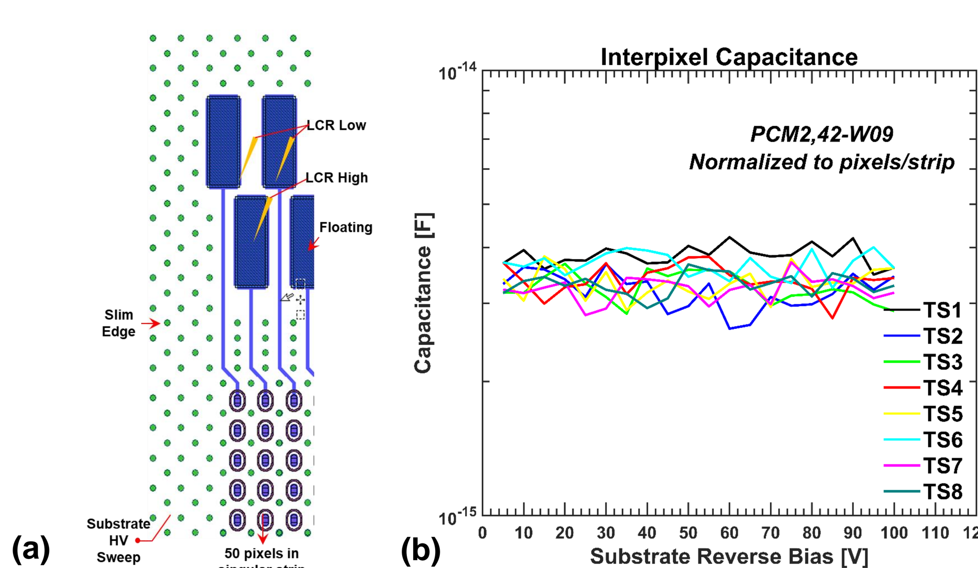


Figure 8: (a) Experimental setup, and (b) Interpixel capacitance of PCM2,42-W09 strip normalized to pixels/strip.

Interpixel Resistance

- A strip test-structure was used to estimate Interpixel resistance. Strip resistance (R_{int}) was normalized to pixels/strip.
- Substrate sweep has been made from -5 V to -60 V.
- Interpixel resistance is several GΩ.
- As expected, no substrate bias dependence was noticed for non-irradiated candidates.

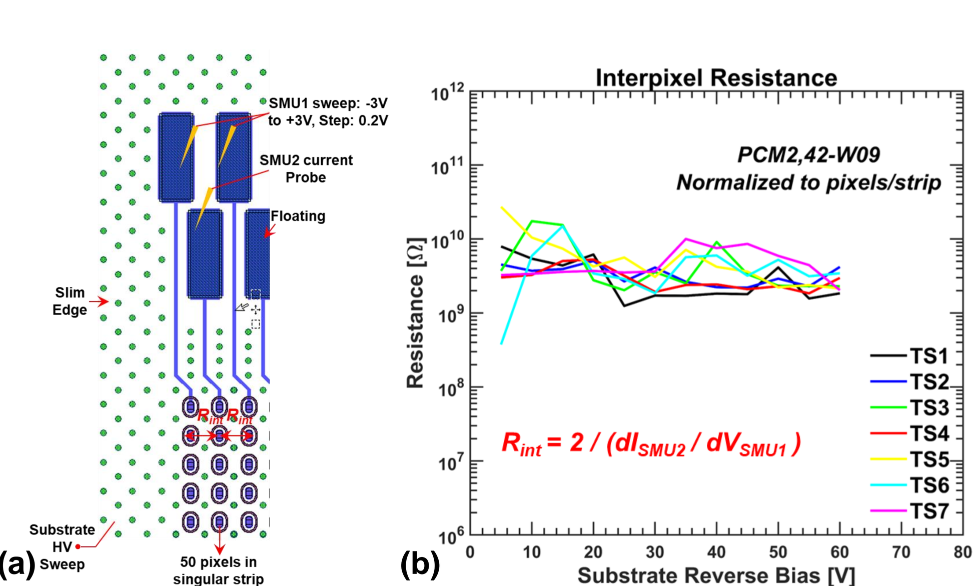
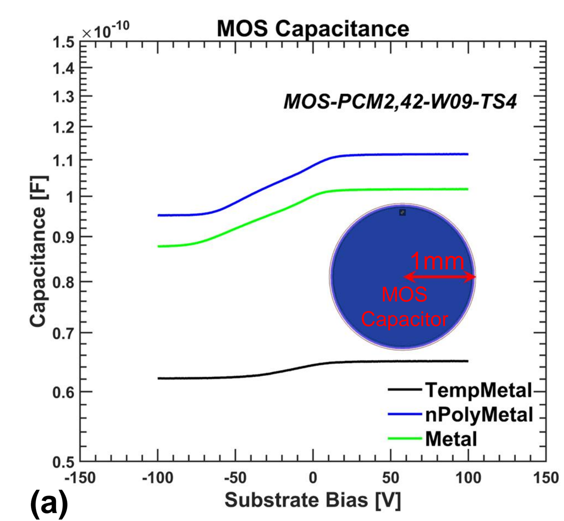


Figure 9: (a) Experimental setup, and (b) Interpixel resistance of PCM2,42-W09 strip normalized to pixels/strip.

Surface Parameters



(b)

OxideThickness [nm]				OxideCharge [cm⁻²]		
MetalOnly	*nPoly+Metal*	*TempMetalOnly*	*ID*	*MetalOnly*	*nPoly+Metal*	*TempMetalOnly*
1066.91	974.60	1664.45	TS1	1.34E+11	5.79E+10	1.58E+11
1065.30	973.38	1667.39	TS2	9.77E+09	4.58E+10	1.69E+11
1064.78	972.49	1668.50	TS3	3.16E+10	4.80E+10	1.23E+11
1063.98	971.03	1667.54	TS4	4.95E+10	5.90E+10	1.10E+11
1062.68	968.68	1669.34	TS5	5.71E+10	5.91E+10	9.22E+10
1060.80	966.51	1670.43	TS6	7.06E+10	4.75E+10	7.54E+10
1059.67	965.44	1669.13	TS7	7.54E+10	3.47E+10	6.45E+10
1058.48	963.43	1665.00	TS8	1.15E+11	2.44E+10	4.67E+10
1063.33	***969.85***	***1668.02***	***Median***	***6.39E+10***	***4.78E+10***	***1.01E+11***
4.39	***6.47***	***2.39***	***Spread***	***4.04E+10***	***1.51E+10***	***5.87E+10***

Figure 10: (a) TS4-MOS capacitance of different types at different bulk bias, and (b) summary of estimated oxide thickness and oxide charge of PCM2,42-W09.

Conclusion

- Investigation of non-irradiated diced sensors' electrical parameters seems to agree with the FBK 3D sensor production line.
- Yield uncertainty from the dicing stage is known. However, diced good sensors leakage and depletion properties are similar to the wafer level QA data.

***Reference:**

1. G.-F. Dalla Betta et al., Development of a new generation of 3D pixel sensors for HL-LHC, DOI: 10.1016/j.nima.2015.08.032

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