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Hybrid Pixel Smart Detector with Integrated RISC-V Microprocessor

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Hybrid single-photon counting pixel detectors have recently been widely used for X-ray and ionizing particle detection in medicine, high-energy physics, and material science. Many different chips have been developed for the readout of semiconductor pixel sensor [1,2]. Usually, developed ASICs have very limited digital logic and do not provide substantial data processing.

In this article, we present a Hybrid Pixel Smart Detector (HPSD) that integrates a matrix of readout channels with a RISC-V-based microprocessor SoC. The designed device has been developed for manufacturing in a CMOS 45nm process with an area of 1.92 mm x 1.92 mm. A layout of the designed integrated circuit is shown in Fig. 1.

Integration of a pixel matrix with the RISC-V-based central processing unit (CPU) significantly improves detector functionality. It enables the device to work independently without external assistive device usage and execute many algorithms, e.g. on-chip calibration, threshold scanning, and data filtering. Communication between the CPU and the pixel matrix is carried out through a dedicated Pixel Matrix Controller (PMC). This specialized peripheral consists of a coprocessor responsible for precise matrix control, data conversions between formats used by matrix and CPU, and control and status registers connected to the core address space and enables fast and independent detector calibration [3]. Another exemplary application of such a solution is intelligent real-time filtering of regions of interest.

The described device is currently at the final stage of the design process, and the integrated circuit will be sent to production at the end of April 2022. The architecture of HPSD is released as an open source project, and its RTL source code, together with developed software were published on GitHub [4].

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[2] R. Ballabriga et al., Review of hybrid pixel detector readout ASICs for spectroscopic X-ray imaging, J. Instrum., vol. 11, no. 1, p. P01007, Jan. 2016.
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[4] P. Skrzypiec and R. Szczygieł, pixel_riscv_soc, https://github.com/agh-riscv/pixel_riscv_soc, 2022.

Primary authors: SKRZYPIEC, Pawel; SZCZYGIEL, Robert

Presenters: SKRZYPIEC, Pawel; SZCZYGIEL, Robert

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