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Development of the Control Plane and Data Path for a 1MHz Continuous Frame Rate Spectroscopic X-ray Imaging Detector System

Tuesday 28 June 2022 12:30 (20 minutes)

The latest iteration of the HEXITEC ASIC, HEXITEC_{MHz} has utilised on-chip digitisation to accelerate frame rates by two orders of magnitude over its analog-readout based predecessor, now with 1 MHz continuous readout [1]. This advancement places significant demand on the capabilities of the accompanying readout hardware; an 80x80 pixel array with 12-bit resolution results in a continuous throughput of over 76 Gbps that must be transferred, processed and stored.

This talk will outline the architecture used to cover the control and data planes. The former—a Xilinx Zynq SoC based embedded Linux board—forms an experimental first application of a new control architecture dubbed LOKI, which aims to provide a flexible solution for hosting the Odin Control framework that can be adapted to future detectors [2].

The latter plane will trace the path of pixel data from packetisation and egress from the ASIC via 20 serialisers (outputting Aurora-encoded scrambled streams at 4.1 Gbps over differential CML) through de-scrambling, reordering, reduction, processing and presentation.

An update on the latest development progress and testing of these external components will also be presented.

[1] M.C. Veale et al., HEXITEC: A high-energy X-ray spectroscopy imaging detector for synchrotron applications, *Synchrotron Radiat. News* 31 (2018) 28

[2] <https://accelconf.web.cern.ch/icaleps2017/papers/tupha212.pdf>

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