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INVITED: Reading 4D pixels at 20 ps in CMOS 28-nm technology

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Inner trackers in high-energy experiments of the next generation must cope with unprecedented high rates and track densities. This poses the need for precise timing information at the pixel level (below 50 ps per hit), high readout frequency (several hundreds of kHz per pixel) and radiation hardness (more than 1 Grad on electronics and more than 1016 1-MeV equivalent neutrons per cm2 on sensors).
While on the sensor side it appears already that such requirements can be met (refer for example to the recent developments on 3D-trench silicon sensors [1, 2, 3]), the challenge is still widely open on the electronics side, where strong area and power density constraints are present. Furthermore, adding precise timing information at the pixel level generates a major amount of information, which imposes extremely high data bandwidth, in the range of hundreds of Giga bit per second per single ASIC. Such value is approximately one order of magnitude more than the present state-of-the-art developments in the field.
28-nm CMOS technology appears having the whole set of characteristics to satisfy the experimental requirements referred above. A first complete 28-nm CMOS ASIC to elaborate technical solutions about the challenging issues of such complex future detectors has been recently developed and tested.
The ASIC, named Timespot1, features a 32x32 channels hybrid-pixel matrix and integrates one analogue front-end, one discriminator and one high-resolution time-to-digital converter per pixel. The system aims to achieve a timing resolution of 30 ps or better at a maximum event rate of 3-MHz per channel with a Data-Driven interface. Power consumption can be programmed to range between 1.2W/cm2 and 2.6 W/cm2.
The present paper intends to deal with the different technological aspects in the challenge for 4D pixels. It will report and discuss on recent studies describing a full set of experimental requirements for 4D tracking. It will also illustrate the experience and the results gained in the design and tests of the Timespot1 ASIC. Other ongoing and possible developments will also be addressed.

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