XVI workshop on Resistive Plate Chambers and Related Detectors (RPC2022)
CERN, 26 - 30 September 2022.

Design of the new RPCs and Front End electronics for the ATLAS High Luminosity LHC program

Luca Pizzimento on behalf of ATLAS muon collaboration

ATLAS RPC Phase-II Upgrade Overview

HL-LHC increased luminosity and much harsher conditions:

- Luminosity = $\mathbf{7,5 \times 10^{34} cm^{-2} s^{-1}}$
- *Pile-up* $\langle \boldsymbol{\mu} \rangle = \mathbf{200}$
- Target: integrate 3000-4000 fb^{-1} (100 times Run-2)
- In these conditions the actual trigger can record only muons with pt>50 GeV

2 main upgrades RPC related are in progress for the ATLAS Muons spectrometer Phase-II

- **The electronics of the ATLAS RPC currently installed will be replaced**

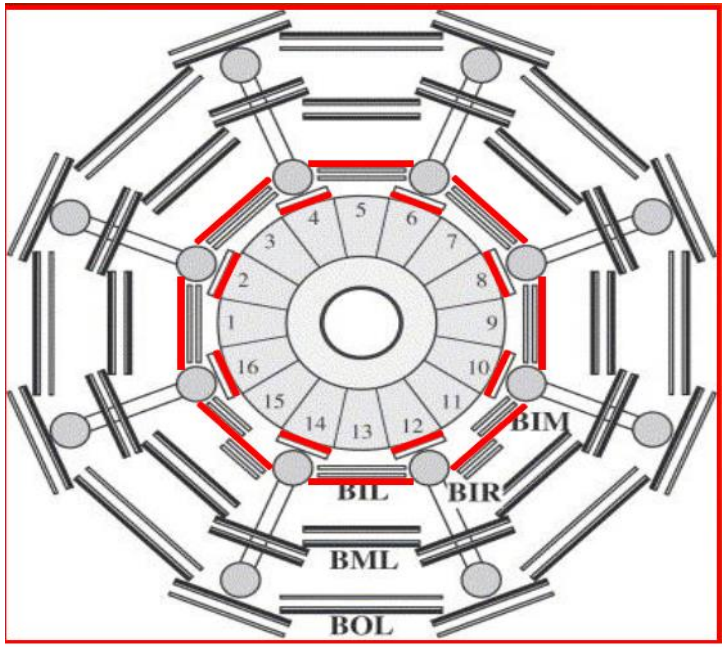
  The present electronics does not meet the Phase-2 specification,
  Readout buffer on the Frontend will not be used. Full information to be sent to backend
  and used in the trigger decision (Including new MDT online reconstruction on MDTTP)

- **BI upgrade; installation of a new RPC system**

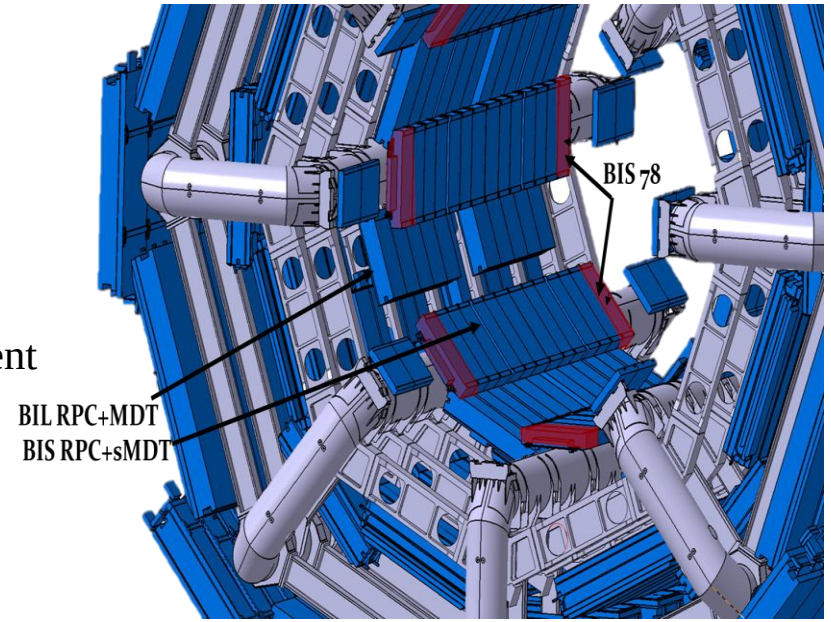
  New RPC detectors installation in the entire inner barrel to improve the RPC trigger coverage and
  new sMDT BIS chambers to gain space for new RPC layers

ATLAS RPC Phase-II – BI project

The BI project will consist in the coverage of the inner barrel of the ATLAS experiment with 272 triplets made of the new generation of RPC detectors



- More Redundancy (6->9layers)
- Longer lever arm (2.3 m->4.5 m)
- Increased acceptance (80%->96%)
- Improved tracking and trigger capability wrt current system
- Good time resolution enabling high-performance TOF



The new Front-End electronics represents one of the main upgrades for the ATLAS Phase-II RPC

- Improved signal-to-noise ratio which allows the reduction of the average charge per count in the detector of one order of magnitude wrt the currently installed system, leading to an improvement of the rate capability from **1 KHz/cm^2 to 10 KHz/cm^2**

BI RPC Challenges

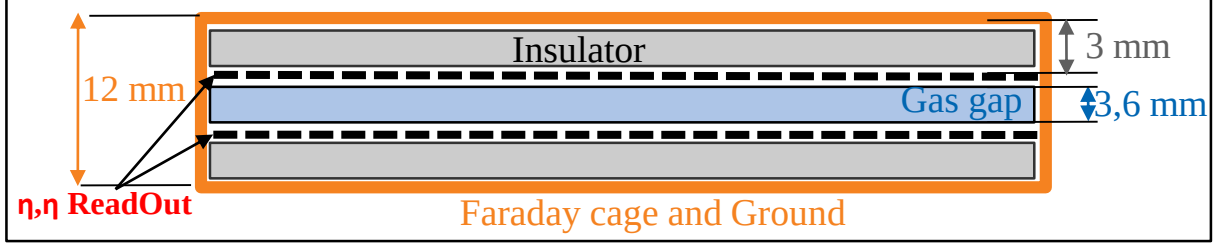
The main challenges to be faced by the RPC BI project:

1. **Physical encumbrance:**
   The spaces available inside the Inner Barrel of ATLAS for the installation of these RPCs is very limited → Redesign of the entire structure of the detector itself (and relative components) in order to fit in the inner barrel

2. **Detector rate capability:**
   The ATLAS currently installed RPCs are certified to work at 100Hz/cm^2 for 10 years. The measured rate capability of these detectors is around 1 kHz/cm^2. The actual RPC performance cannot be guaranteed in the harsher conditions of HL-LHC → The BI RPC detectors will exploits the new electronics to overcome this problem and improve the rate capability by an order of magnitude.

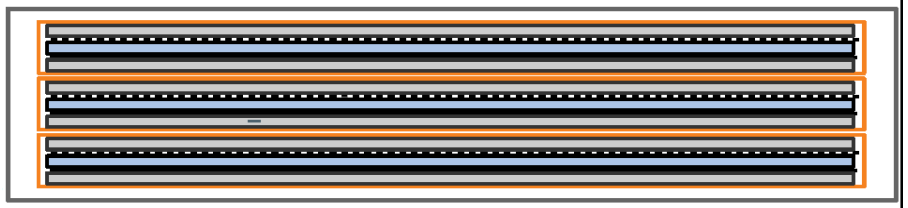
BI RPC Challenges – Physical encumbrance & new detector structure

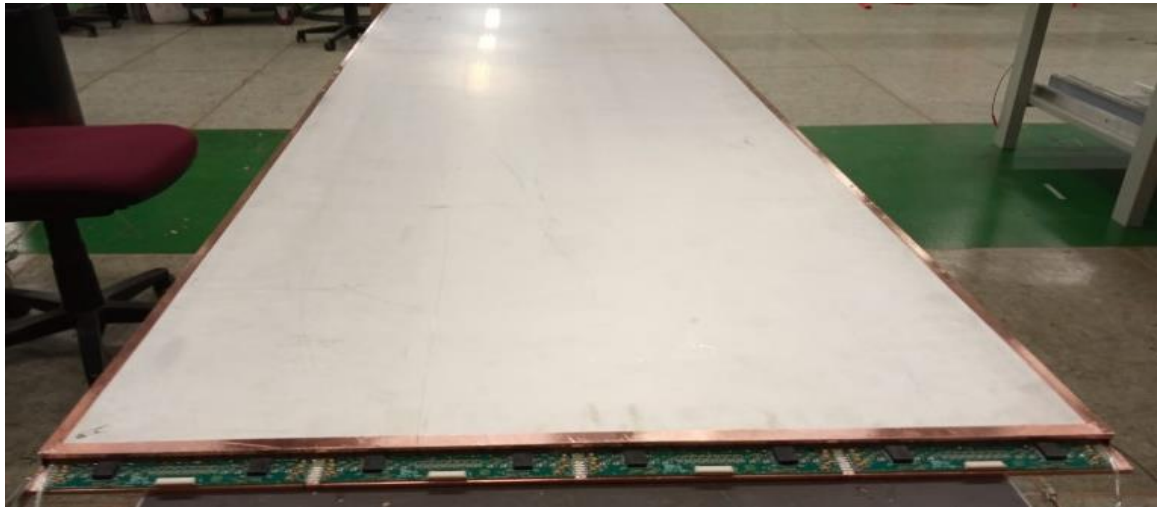
BI RPC singlet layout



RPC triplet layout

- 3 independent singlets
- 6 x 32/48 η FE chs





The available space in the ATLAS muon-spectrometer inner barrel implies mainly:

- Few centimeters space (in the orthogonal direction wrt the beam) for the full detector placement along with most of its services
- Some fully inaccessible zones

Detector and services structures re-design

- No room for the electronics on the detector phi side due to geometrical factors and impossibility to overlap BIS chamber

Parallel strips readout (second coordinate measured with the time arrival difference at the detector edges)

	ATLAS RPC currently installed	ATLAS New generation RPC
Detector	Mono gas gap	Mono gas gap
Gas Gap width	2 mm	1 mm
Electrode Thickness	1.8 mm	1.2 mm
Gas Mixture	95% TFE, 4.7% i-C4H10, 0.3% SF6	95% TFE, 4.7% i-C4H10, 0.3% SF6
Time Resolution	1 ns	0.4 ns

The time resolution < 100 ps of the TDC embedded in the FE allows the reconstruction of the second coordinate with 1 cm space resolution.

BI RPC Challenges – Physical encumbrance & new detector structure

Bakelite: FDR done, next step pre-production

Gas gaps: FDR next week, next step pre-production

Strip panels: FDR next week, FR4 procured, next step pre-production

Singlets assembly will be done initially without the FE (to be added later), starting beginning of next year

Production foreseen to end by 2025, first chamber requested by ATLAS for installation mid 2026

RPC detector and high-radiation environment

The **RPC rate capability** is mainly limited by the current that can be driven by the high resistivity electrodes.

$$V_{el} = V_a - V_{gas} = IR \Rightarrow V_{el} = \rho d \langle Q \rangle \Phi$$

$$V_{gas} = V_a - \rho \cdot \frac{d}{S} \cdot \langle Q \rangle \cdot S \cdot \Phi_{particles} = V_a - \rho \cdot d \cdot \langle Q \rangle \cdot \Phi_{particles}$$

$$RateCapability = \frac{\Phi}{V_{el}} = \frac{1}{\rho d \langle Q \rangle}$$

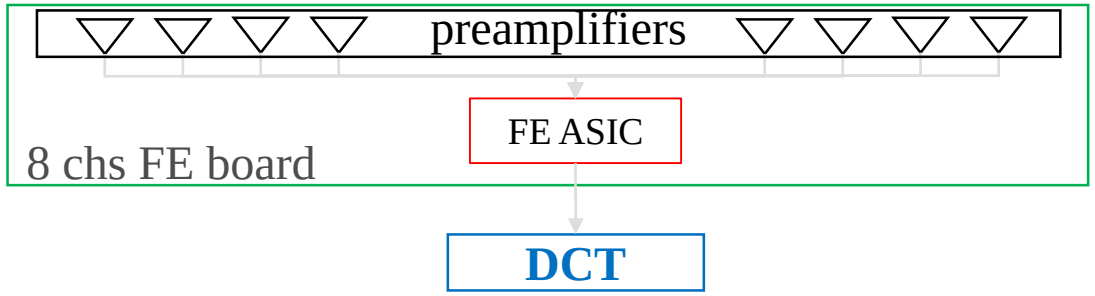
Reduce the average charge per count Q:
This method is the only one that permits to increase the rate capability while operating the detector at fixed current.
No further ageing test required

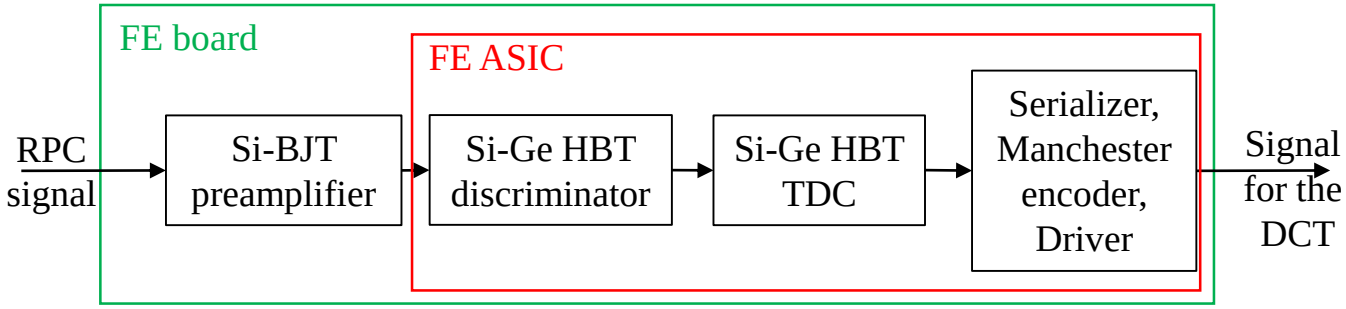
$\langle Q \rangle$ reduction requirements:

- Very sensitive FE electronics with an excellent signal to noise ratio
- High suppression of the noise induced inside the detector by the electronics and by external sources
- Very careful optimization of the chamber structure as a Faraday cage.

BI Front-End electronics

Mixed technology of Silicon BJT for the discrete component preamplifier and a full custom ASIC in IHP BiCMOS technology





1. Minimum Threshold of 0.3 mV
2. Detectable signal of *1-2 fC*

Pubblished on JINST **15** (2020) no.11, C11010

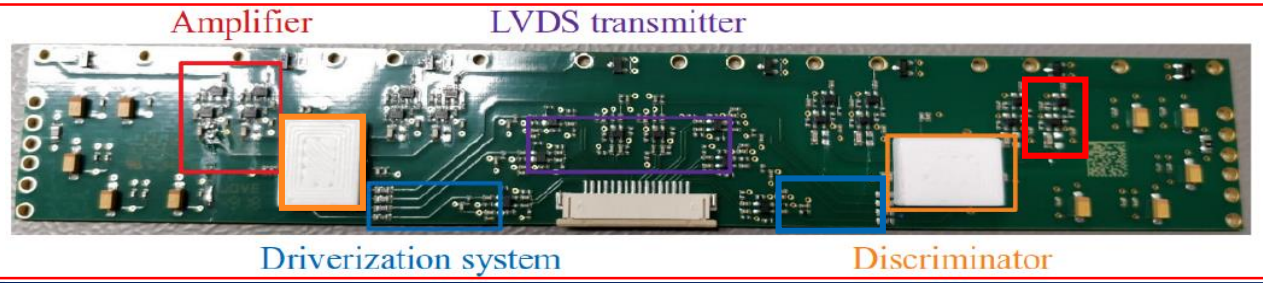
Reduction of factor 10 in the charge produced inside the gas gap

Total FE power consumption: 15mW/ch

Rate capability up to 10 kHz/cm²

Strategy behind the integration of the TDC directly within the FE ASIC:

- Less sensibility to the various sources of noise, implying better overall performance
- "Easier" to achieve the required time resolution (100ps) for the second coordinate measurement with 1cm space resolution
- Reduction in the complexity of the connections with an external system
- No complex cables calibration are required in order to achieve the desired space resolution (1 cm) for the second coordinate measurement



ATLAS phase-I RPC FE electronics (BIS78 project)
This is the FE board I developed for the pilot project of the BI. The BI electronics will inherit most of the architecture

BI Front-End electronics - ASIC Overview

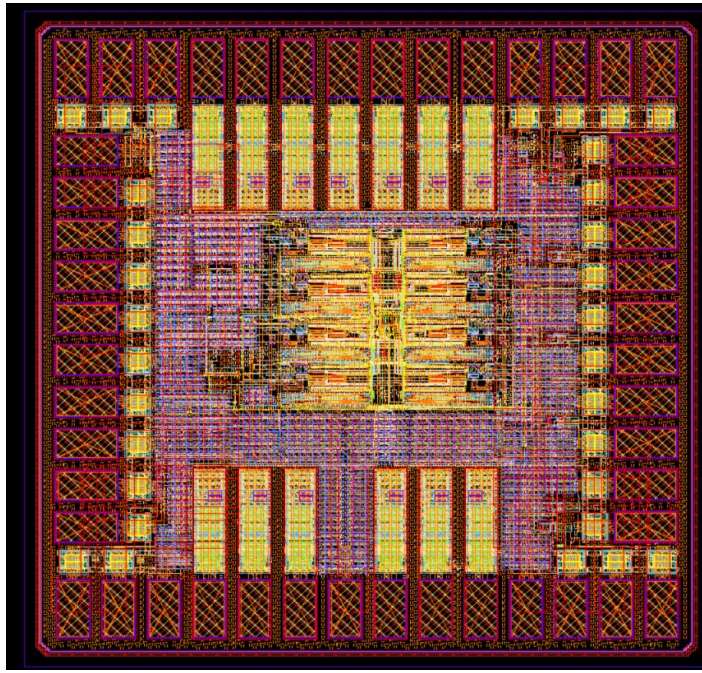
- **Discriminator**

  Upgrade and optimization of the BIS78 discriminator

- **TDC**
  - VCO; free running oscillator which defines the TDC time resolution driving the scaler
  - Scaler; 8-bits synchronous counter
  - FF & Registers; memories which save the status of the TDC scaler when the RPC(latch) signal is provided

- **Transmission logic, serializer and transmission protocol**

  The data communication to the DCT is performed with a serial line for each channel which transmits, in the given latency budget, all the informations to allow for the reconstruction of the event and a possible trigger candidate. The transmission is Manchester encoded

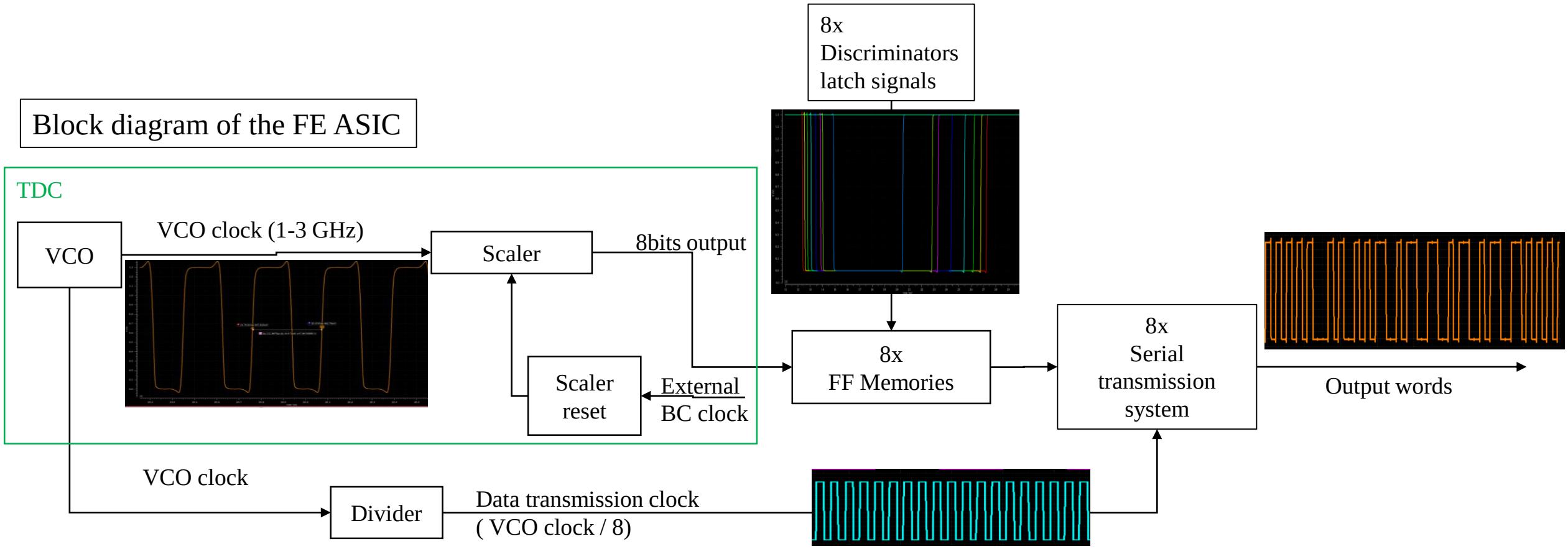


ASIC foundry runs:

- September 2020; pre-prototype containing the individual components and several single chain configurations
- March 2021; First prototype with the 8-channels configuration along with the final architecture and the transmission system
- July 2021; Same architecture of the previous foundry run with a slightly different technology
- September 2022; Second prototype with the full configuration and problems found fixed

BI Front-End electronics - ASIC Overview

Block diagram of the FE ASIC



BI Front-End electronics – Voltage Controlled Oscillator

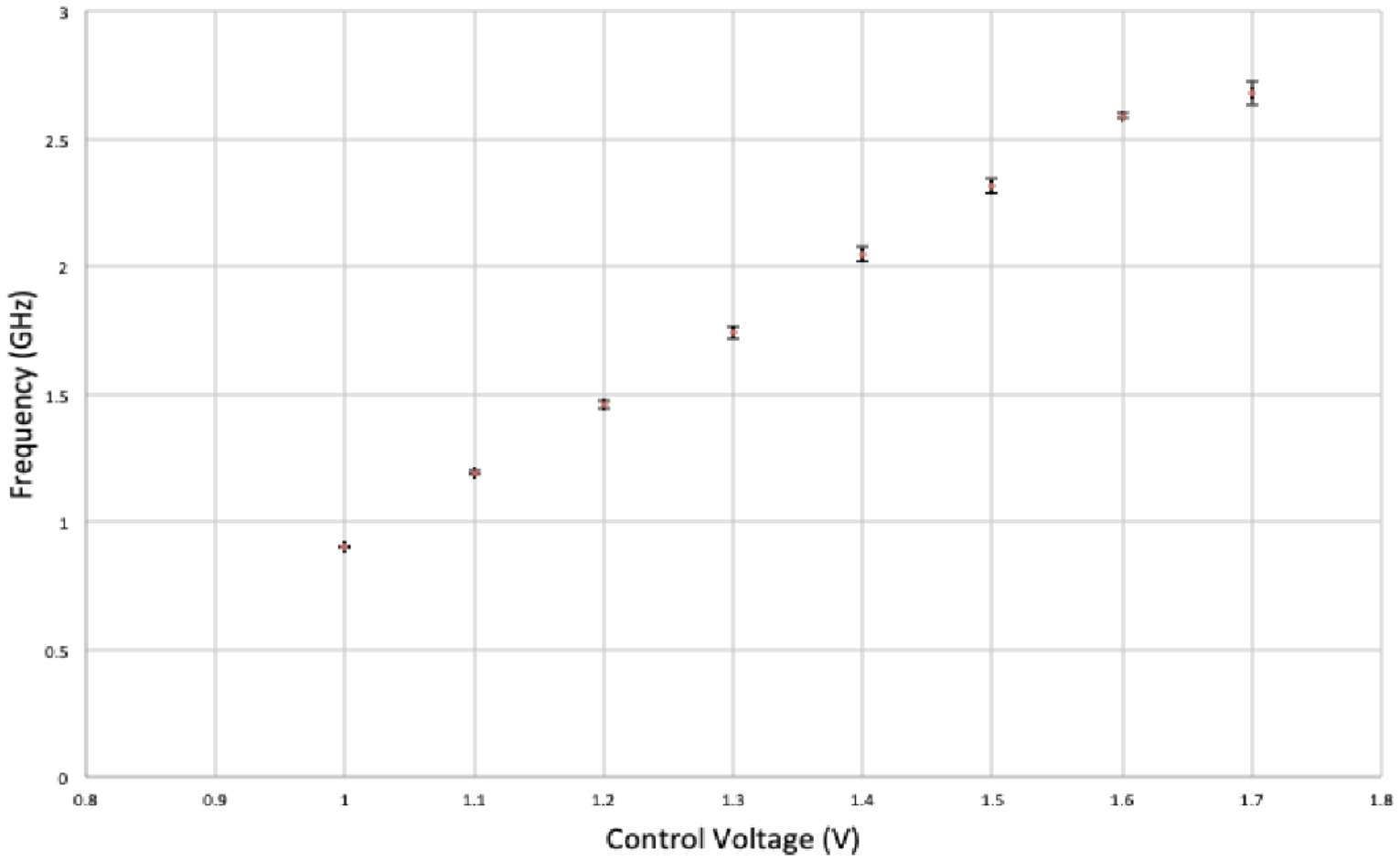
Study of the performance of the VCO 3 stages **with control circuits** as function of the voltage that defines its oscillation frequency (Vctrl)

(simulation results)

Period (ps)	Binning (ps)	Voltage supply (V) (Vctrl)
516	258	1
418	209	1.1
354	177	1.2
314	157	1.3
285	142	1.4
262	131	1.5

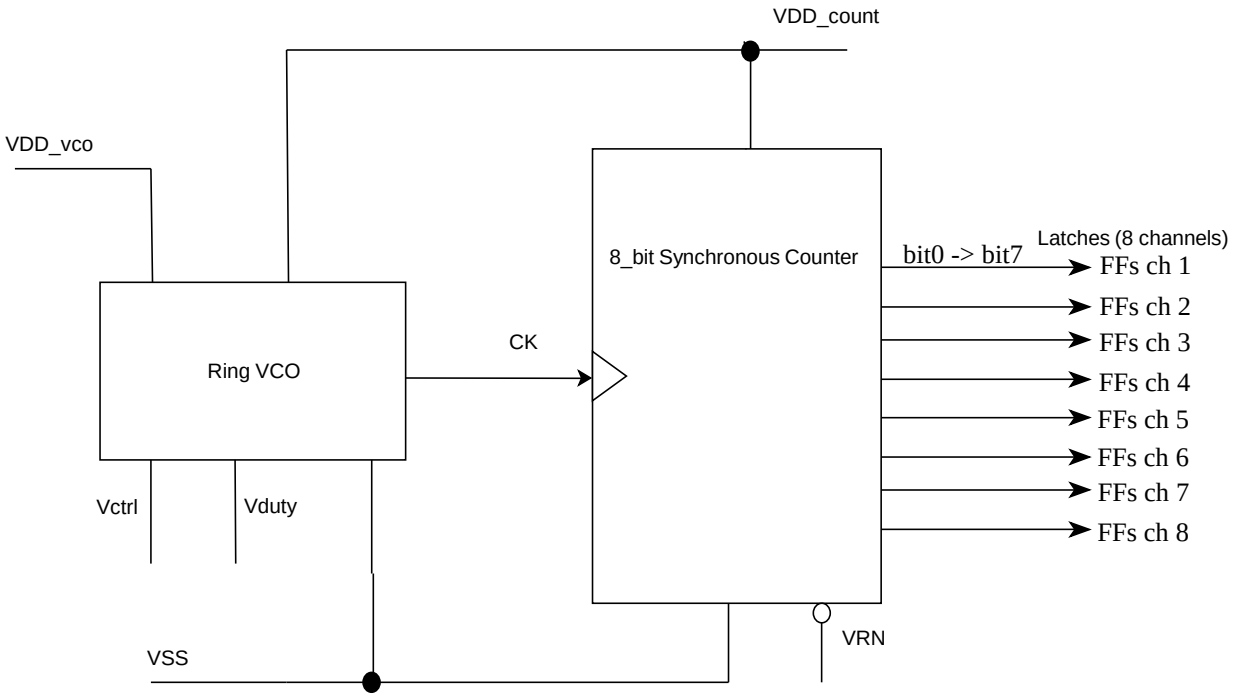
Typical values: VDD = 1.3 V ; Vctrl = 1.3	
VCO Frequency	3.2 GHz
Duty Cycle	Tunable
Power consumption	1-2 mW

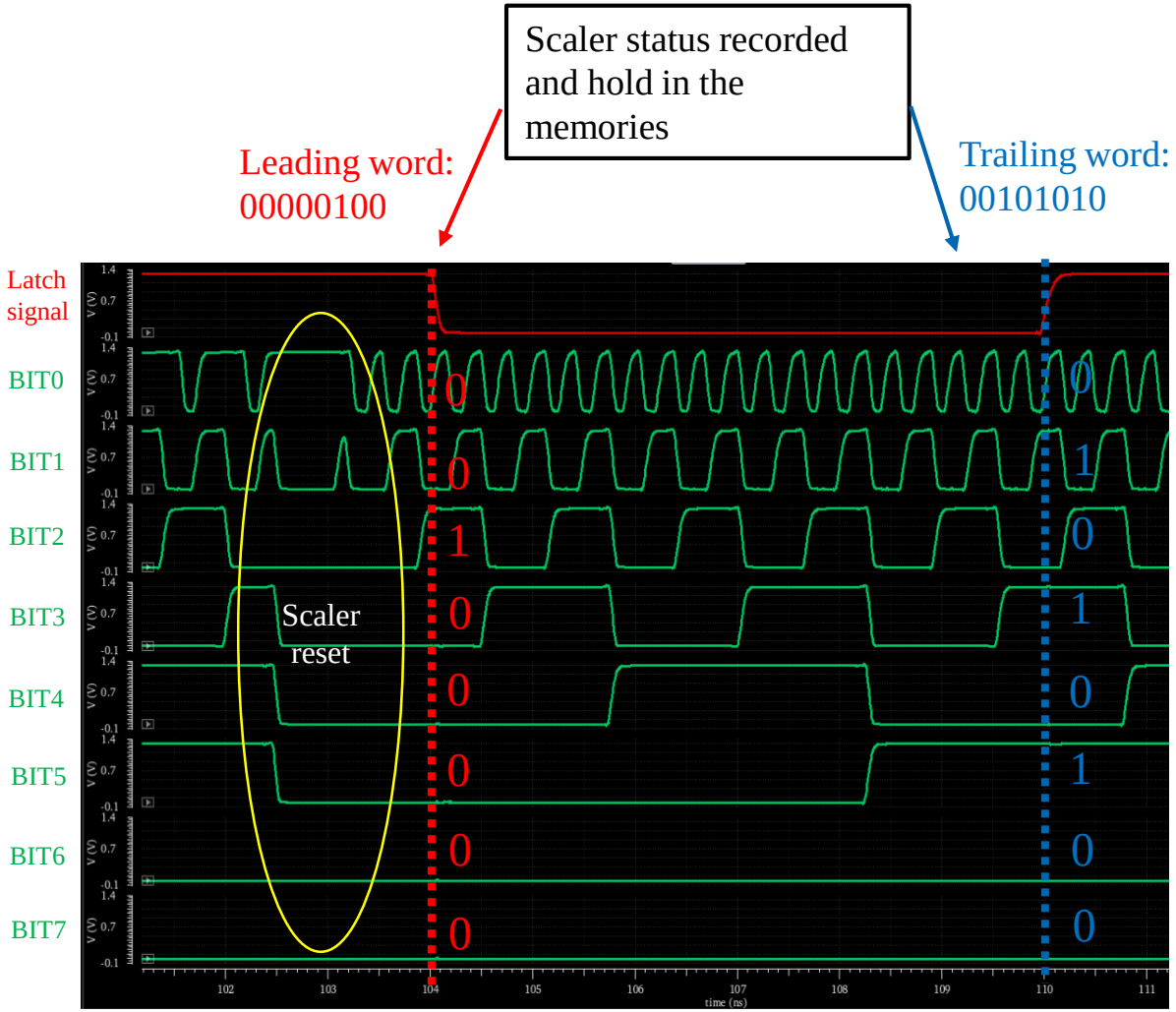
VCO with 3 stages calibration curve as function of Voltage supply (experimental results)



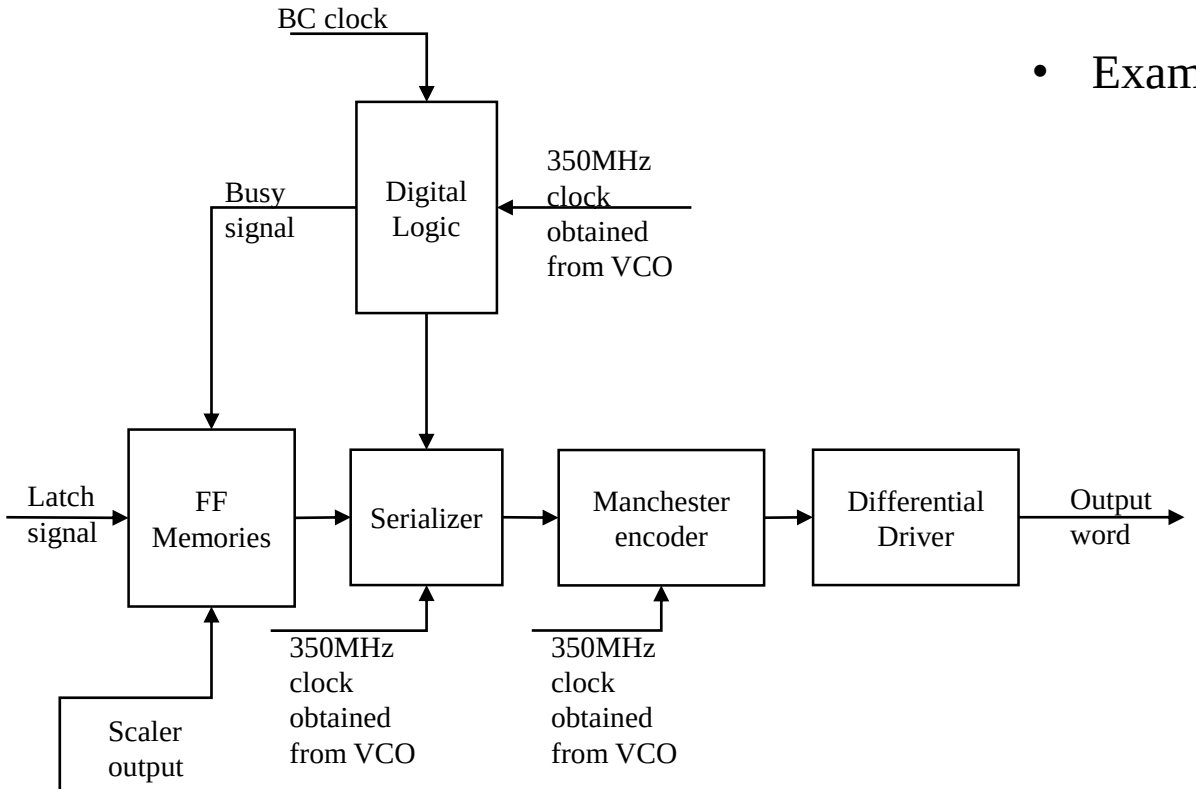
BI Front-End electronics - TDC

- **Time resolution: 150 - 50 ps rms**
- **TDC power consumption 5 mW**
- **VCO frequency range: 1 – 3 GHz**





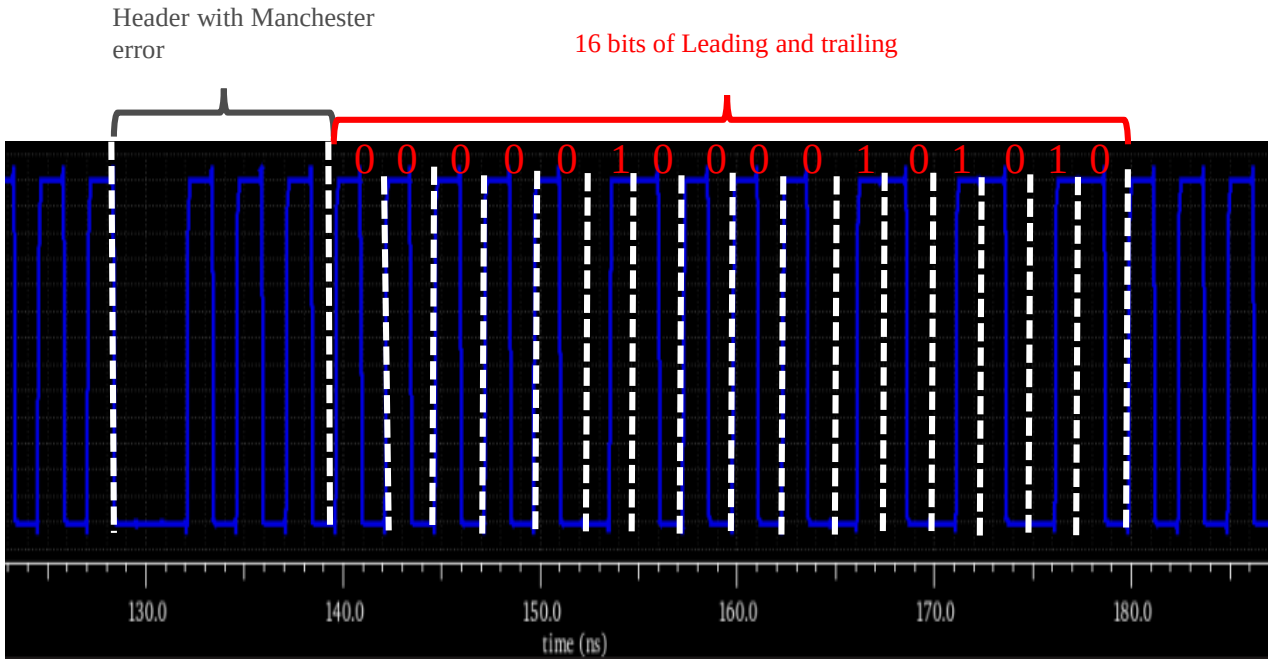
BI Front-End electronics - Serial transmission



Clock transmission in idle state | Header | Clock transmission in idle state

- Example of transmission: 101010-0010-Manchester encoded data-101010

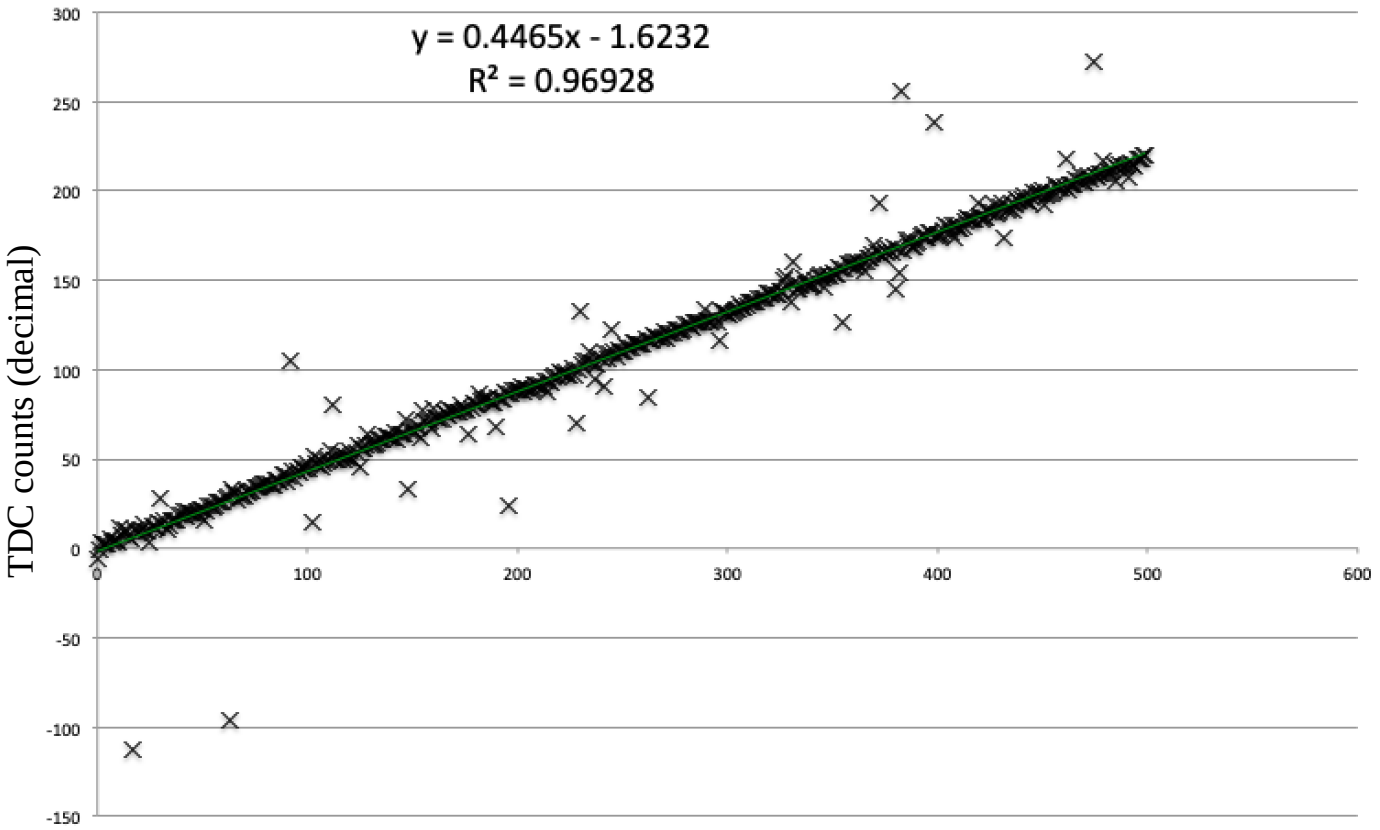
Manchester error



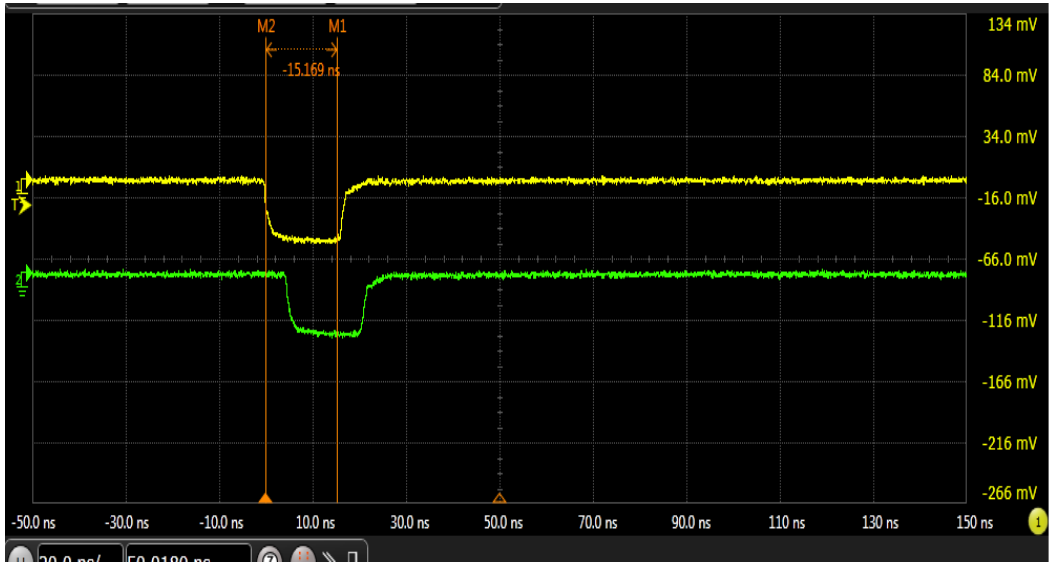
- The data will be encoded using the Manchester coding. For this prototype the transmission will consist of 16 bits of leading and trailing + 2 bits of BC counter and 2 bits of header (Manchester error; 3 semiperiod at 0 and 1 semiperiod at 1) to recognize the beginning of a data word in the receiver and to start the decoding.
- Each channel has its own independent serial transmission line

BI Front-End electronics - Functionality measurement

2 synchronyzed signals have been injected in 2 different channels. One is fixed and used as a timing reference while the delay of the second one wrt the first one is varied and the time difference between the two channels is measured.



Delay between injected signals (*100 ps)



Each delay step is 100ps and for each step 100 events are acquired.
Events out of the linear fit corrispond to a fraction <1%

slope = 0.4465 bin / (100ps)
1/slope = 224 ps/bin

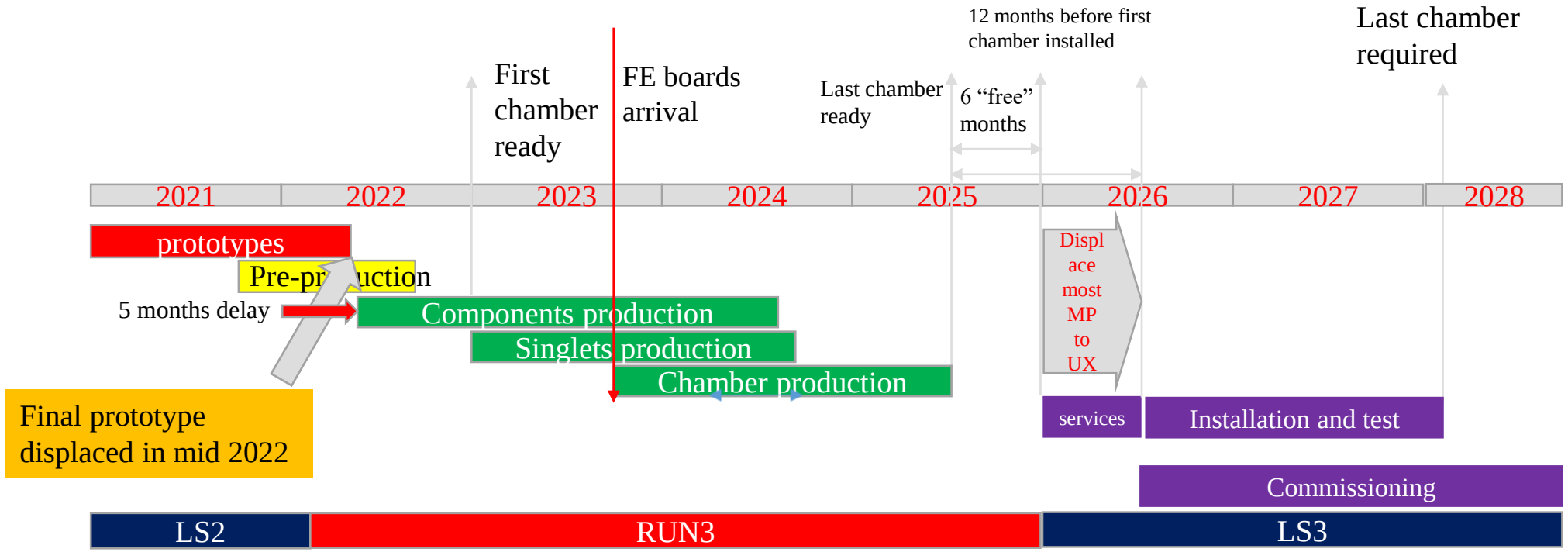
FE status & next to come

- The pre-prototype of September 2020 show that the individual components and the TDC+discriminator coupling in **all the different configurations work as designed**
- The prototypes of March and July 2021 work fine overall with 3 problems found: **Understood and solved**
- Second prototype submitted in September 2022 and expected for testing on March 2023
- FE electronics production expected to start in the second half of next year

Conclusion & overall project plan

The 2 BI project major challenges have been overcome

1. Rate capability improved; 1fC FE threshold and up to 10 KHz/cm^2 rate capability
2. Physical encumbrance; Detector full re-design completed



- Final prototype delayed by 5-6 months
- R3 extended by 1 year and LS3 by 6 months
- The schedule float is satisfactory at the moment

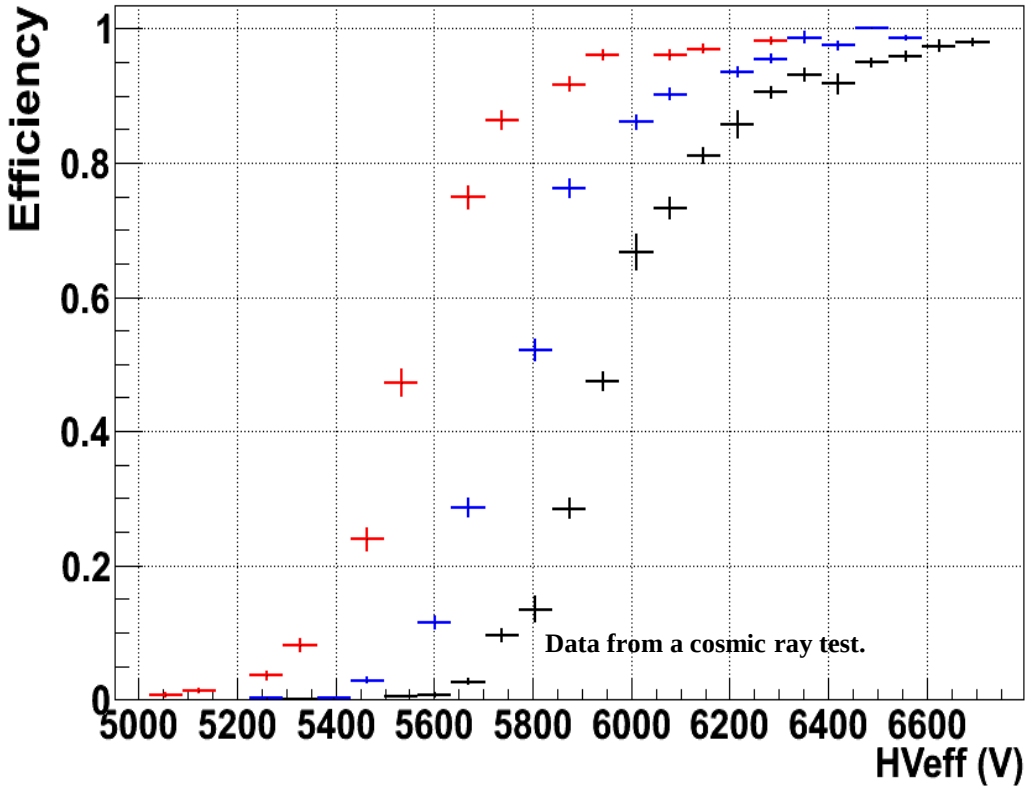
Thank you!!!

Back up

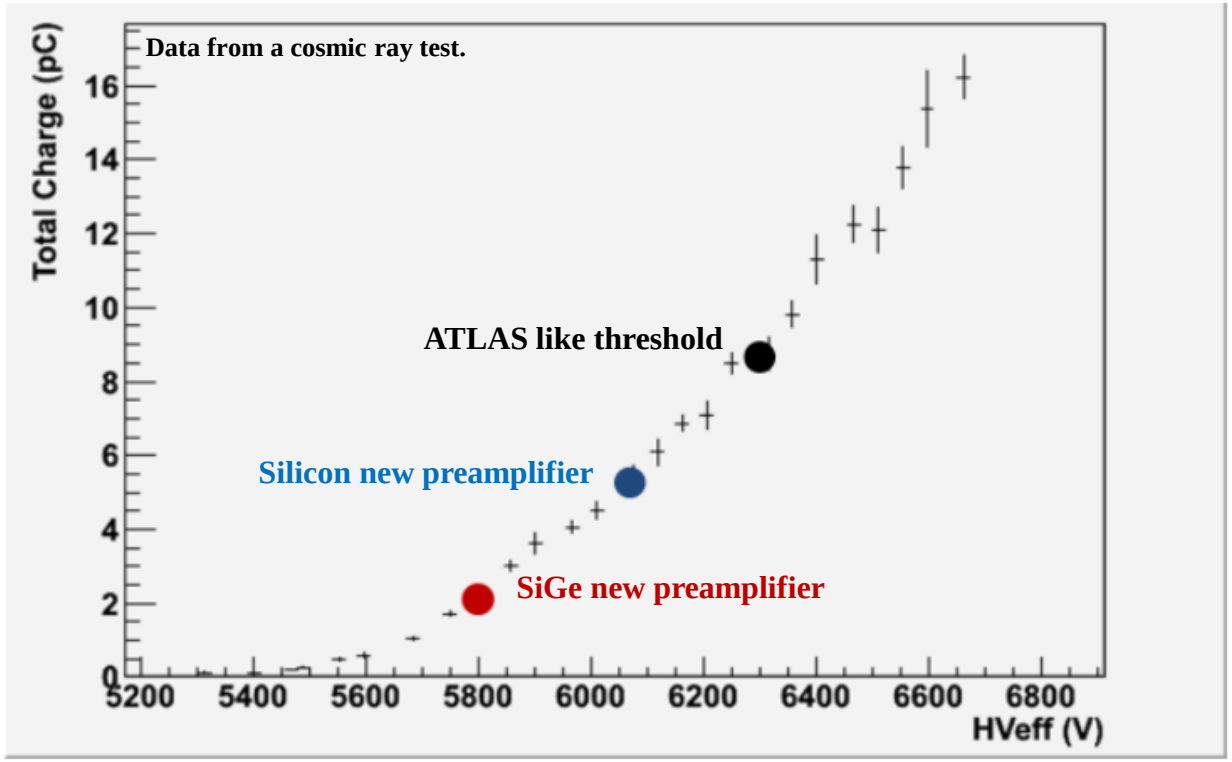
BI Front-End electronics on RPC

Using a more sensitive FE electronics allows to operate the detector at a lower gain. Lowering the gas gain means lower charge per count within the gas volume. The prompt charge injected in the FE is just a small fraction of the total charge.

A 1 mm gap RPC detector read out with a ATLAS like threshold (black), the new preamplifier in silicon technology (blue) and in SiGe technology (red)

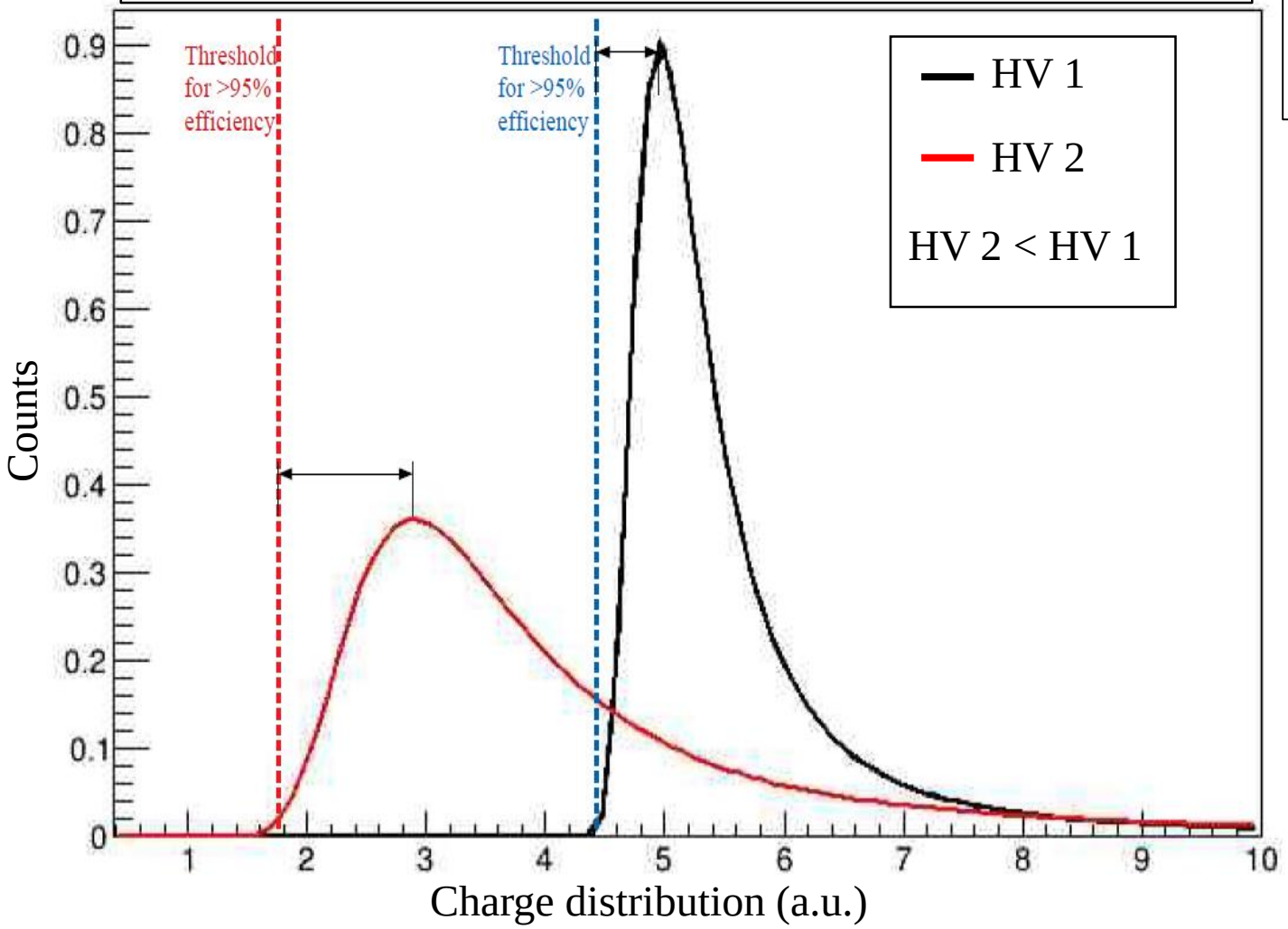


Total delivered charge per count in the gas volume. The working point with different front ends is reported .



BI Front-End electronics - threshold constraints

Sketch of the RPC charge distribution as function of HV

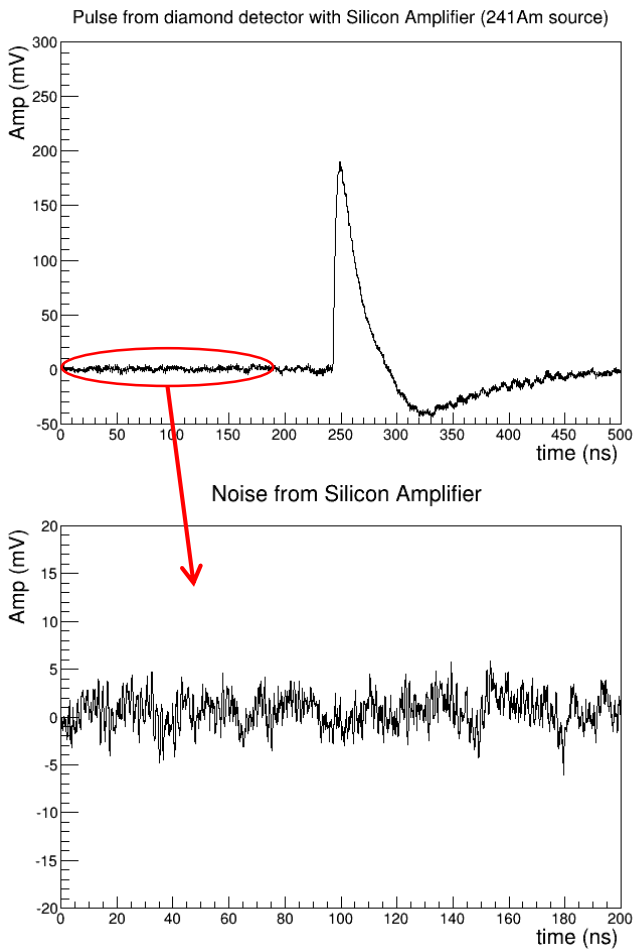


The approach chosen to increase the rate capability requires a reduction in the electric field

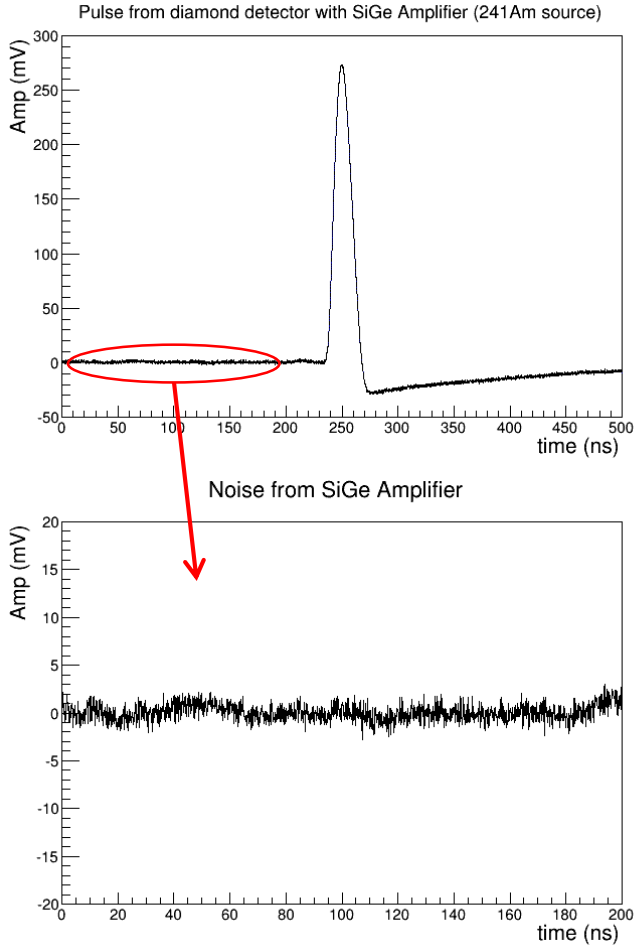
- Reduction of the average charge per count (mean value of the charge distribution)
- Charge distribution changes, spreading over a wider range

Signal and noise from SiGe Amplifier and Silicon Amplifier

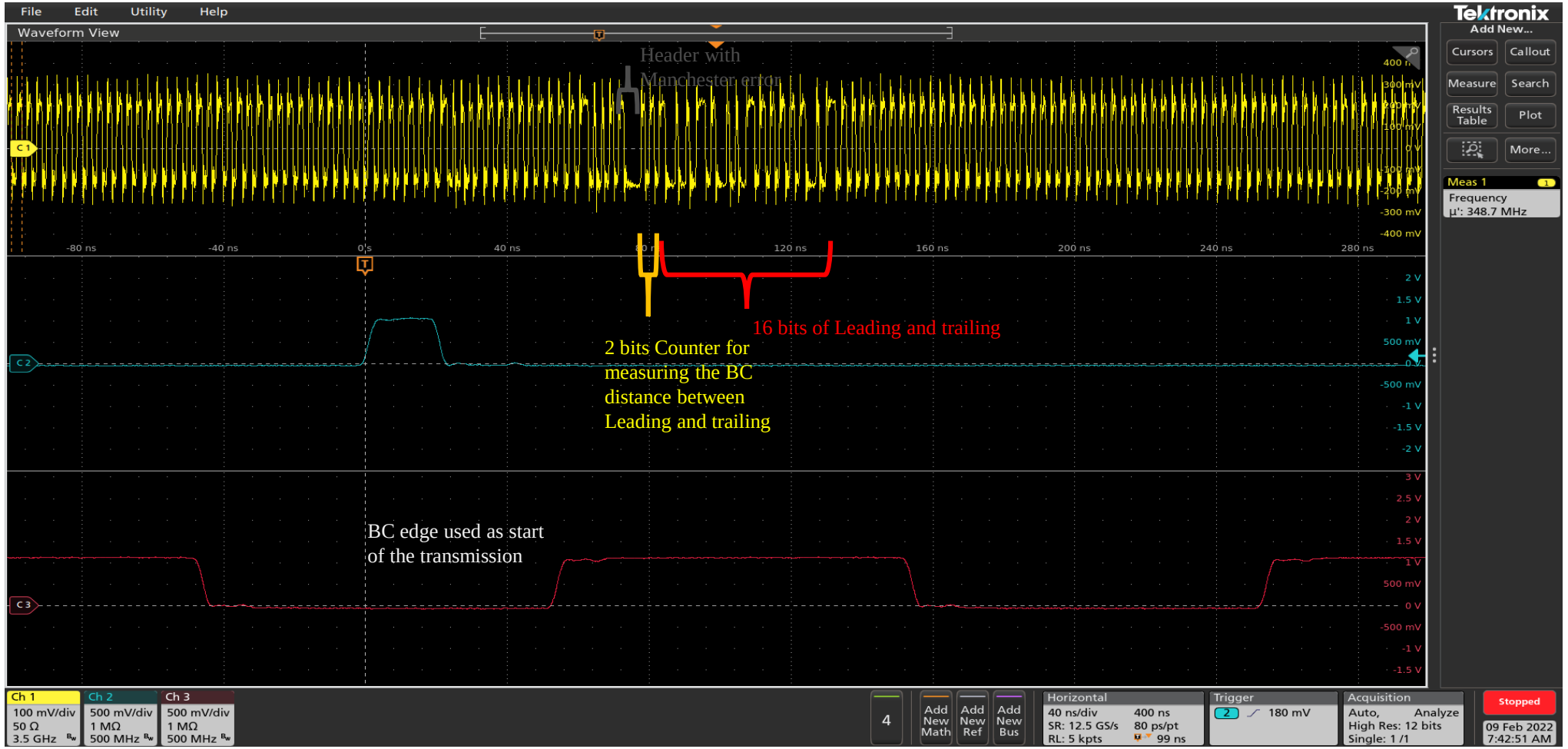
Silicon amplifier



SiGe amplifier



BI Front-End electronics - Serial transmission



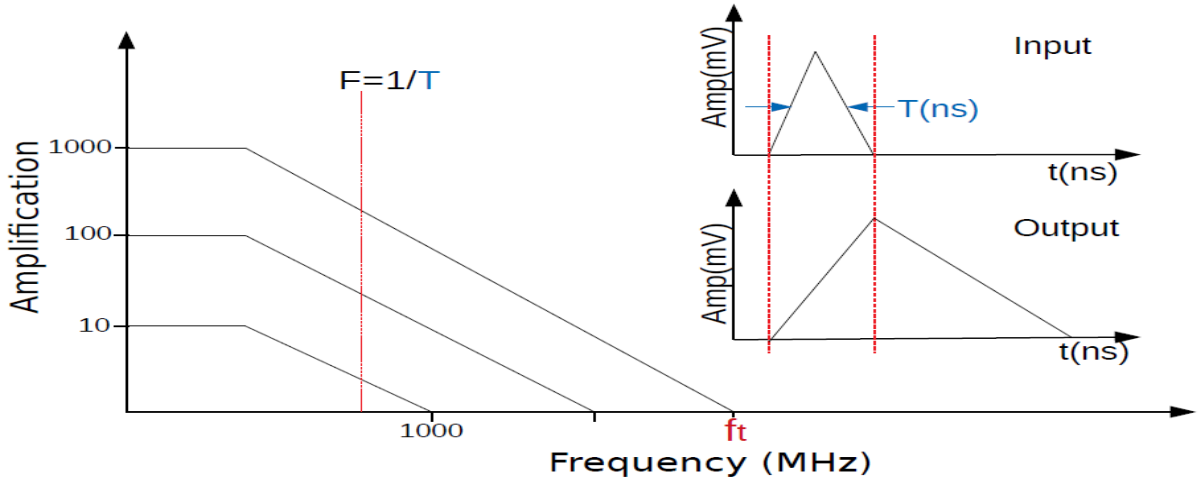
The data word transmitted for the given latch is reported in this plot. The serial encoded transmission is regulated receiving as inputs the status of the latched memories, the dataclock, the latch signal and the BC clock.

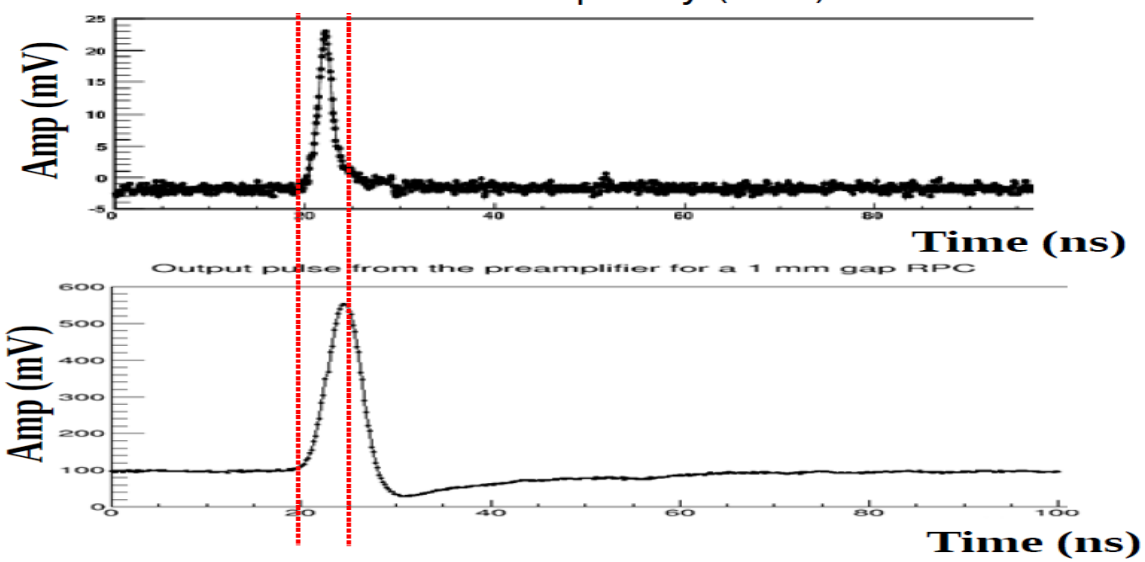
This shows how the words are correctly encoded and transmitted along with the header and the counter as expected

The transmission happens after the expected edge of the BC clock, the expected bits are transmitted manchester encoded and the trasmission last as expected according to the data clock provided by the VCO frequency

BI Front-End electronics – Preamplifier

The new premplifier developed for the RPCs is made in **Silicon Bipolar Junction Transistor** technology. It is based on the concept of a fast charge integration

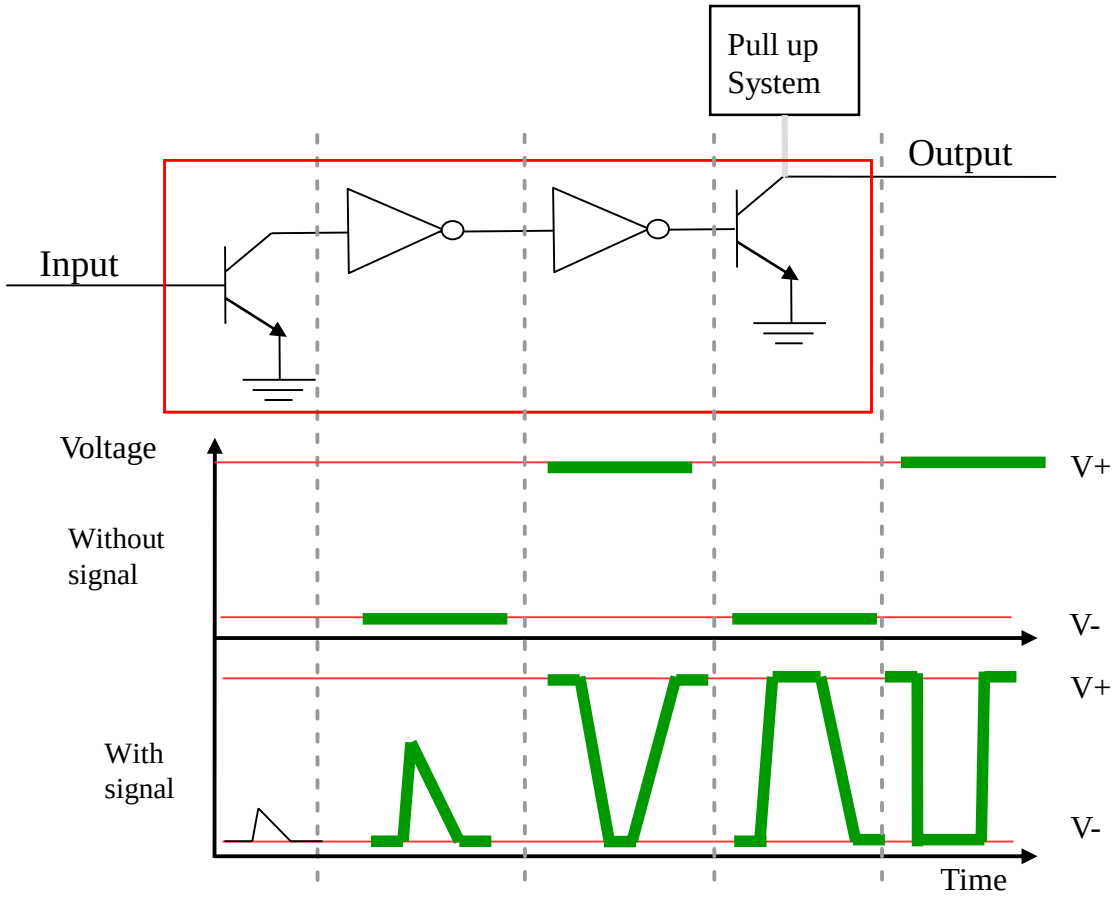




Preamplifier parameters	
Voltage supply	1-5 Volt
Sensitivity	2-4 mV/fC
Noise (up to 20pF input capacitance)	4000 e^- RMS
Input impedance	50-150 Ohm
BandWidth	10-100MHz
Power consumption	2-10mW/ch
Rise time $\delta(t)$ input	300-600 ps
Radiation hardness	1 Mrad, 10^{13} $n\ cm^{-2}$

BI Front-End electronics – Discriminator

The new full-custom discriminator circuit dedicated to the RPCs for high rate environment is developed by using **the Silicon-Germanium HJT technology.** The main idea behind this new discriminator is the limit amplifier. The output signal will have a FWHM proportional to the time the input signal stays above the threshold, performing a TOT measurement



The **SiGe heterojunction bipolar transistor (HBT)** suits perfectly the chosen architecture. The discriminator designed in this way is able to exploit the unique features of the Si-Ge technology

Discriminator parameters	
Technology	Si-Ge BiCMOS 130 nm
Voltage supply	1-2.5 Volt
Minimum Threhsold	0.3 μV
Minimum input pulse width for threshold linearity	0.5 ns
BandWidth	10-100MHz
Power consumption	10mW/ch
Output Rise time $\delta(t)$ input	300 ps
Input impedance	100 Ω
Double pulse separation	1 ns
Radiation hardness	10 kGy, 10^{13} $n\ cm^{-2}$