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CMS Phase 2 Upgrade of the RPC Link System - Review of the Link Board and Control Board firmware and System validation

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The electronics upgrade Phase 2 of the present RPC chambers is ongoing in the CMS RPC system. According to the project baseline, this system will be deployed and fully operational at the CMS for Run 3 to fully cope with the HL-LHC condition. Regarding this goal, the design and prototyping of the new Link System has started a few years ago, and now the final prototyping of this system is ready for final validation. For this reason, we decided to review the electronics architecture of the new Link Board and Control Board, the main building blocks of the Link System, and explain in more detail their firmware and state machine controller. We also describe the idea of the low latency multi-hit capturing in the Link Board and will show how every hit gets a timestamp at the high precision time to the digital converter unit. Moreover, we explain how every two Link Board, known as Slave Link Board, send their data to their adjacent Link Board, called Master Link Board, through the internal local bus on the front panel board by the GBT-FPGA data transmission protocol. In the same way, we will review the slow control command controller on each of the Link Board and Control Board. The system diagnostic, including the hit rate histogramming, RPC signal raw data logging, and the beam timing profile histogramming will be presented.

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