

Maxime Gouzevitch on Behalf of CMS Muon groups

IP2I, Lyon, France

- 1) FEB for iRPC upgrade for HL-LHC
- 2) FEB design
- 3) FEB certification, calibration and integration



1) FEB for iRPC upgrade for HL-LHC



iRPC project for HL-LHC phase



- 18*2 RE3/1 and 18*2 RE4/1 chambers.
- Redundancy with CSC chambers.
- Coverage of CSC dead regions fr the trigger.
- Excellent absolute timing resolution for L1 trigger: O(500 ps).
- Dedicated trigger for Heavy Stable Charged Particles.

iRPC project constraints

	Present system	iRPC
η coverage	0 – 1.9	1.8 – 2.4
Max expected rate (Safety factor SF = 3 included)	600 Hz/cm ²	2 kHz/cm ²
Gap size	2 mm	1.4 mm
Average charge / MIP	> 60 pC	~ 40 pC
Electronics threshold	150 fC	30-50 fC
TDC T resolution		20 ps



A dedicated iRPC electronics designed compared to RPC one:

- Higher rate capability
- Fast and high rate optical fiber readout
- Provide absolute time resolution < 100 ps for space resolution and absolute time resolution.
- Sensitivity to 3 times lower threshold.
- Low noise.
- Radiation tolerance.



2) FEB design





Technical specifications

Difference wrt to previous FEBs

 \cap

RPC FEB.

Output connectors (each: 16 LVDS out + 4 LVDS



Input connectors (each: 16 Signal-GND pair)



■ Connected to 1 side of a copper strip through shielded cables (endcap)/kapton flex (barrel).

- Custom CMS electronics (amplification & discrimination)
- Time association (BX) done at level of Link System.
- FEB \rightarrow twisted pair cable (LVDS signal) \rightarrow Link system iRPC FEB:
 - Connected to both ends of a PCB strip through an internal return line (inside PCB): 2D signal readout
 - PETIROC ASIC: preamplifier + discriminator (custom OMEGA).
 - Time measurement with a TDC FPGA on board.
 - FEB \rightarrow Optical fiber \rightarrow BackEnd



History of the FEB

First proto

2017 proof of principle for <u>CMS-MUON-TDR-016</u>

2 PetiROC2A + FPGA Cyclone II + ETHERNET directly on strip PCB (50 cm)



M. Gouzevitch	: CMS	iRPC FEE	development	and v
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Feb V0 2018 <u>First FEB</u> (Conf. note)

1 PetiROC2A + MEZZANINE with FPGA Cyclone II + ETHERNET





Feb V1 2019 FEB without mezzanine

2 PetiROC2B + FPGA Cyclone V + ETHERNET



Feb V2 2021 Non-rad hard for iRPC Demo

6 PETIROC2C + 3 FPGA Cyclone V + Optical GBT



Feb V3 \rightarrow 2023 Rad hard final

6 PETIROC2C + 3 FPGA PolarFire + Optical GBT





FEBv2 details

- > 2 FEBs / Chamber \rightarrow 144 (+16 spares) FEBs in total
- ➤ 3 Erni connectors with 32 channels each.
- ➤ 6 ASIC PetiROC2C (PR2C):
 - Specially designed by OMEGA group for CMS RPC project based on Petiroc2A
- > 3 FPGAs (96 + 6 TDC channels)
 - FEBv2: CYCLONE V (non rad-hard)
 - FEBv3: POLARFIRE (rad-hard)
- ➤ CERN ASICS: GBTx + GBT-SCA + VTRx
 - for the communication ald slow control
- Separated 2V and 4V power zone for Analog and Digital components. Latchup protection (Overcurrent detection).





FEBv2 logical scheme





PetiROC ASIC

PETIROC2A designed for PET

- High frequency preamp
- Thr > 60 fC
- Time resolution < 100 ps
- Limitations: low rate expected



https://dx.doi.org/10.1109/NSSMIC.2018.8824464

PETIROC2A for RPC :

- Retriggering and inter-channels cross-talk
- Thr > 100 fC
- Time resolution < 200 ps

PETIROC2B modif for iRPC :

- Reduce preamp. frequency
- Thr $\sim 100 \text{ fC}$
- 10-20 ns / ASIC dead time introduced to remove retriggering
 - \rightarrow 2-3% efficiency loss / chamber

PETIROC2C re-designed for iRPC :

- Removed useless components from PR2A.
- Thr < 50 fC
- 40 ns auto-reset / channel te remove retriggering.
- 864 (+ 96 spares) required,
 900 available,
 1000 under production.



3) Certification, calibration and integration



FEB certification steps in IP2I, Lyon

Based on the **FC7 card (Tracker certification card)** system and controlled by **Python software** tools.

- Perform a Quality Check Process to validate :
 - Each electronic block of the FEB independently (SCA, GBTx, Power Supplies, tests points)
 - The data integrity of the system
 - The operation of the FEB firmware designed in the FPGA(s)
 - The operations of the TDC(s) and ASIC's
- Simulation and validation of real operation with injection board



CMS

FEB pedestal alignement method



Threshold applied well above noise level

M. Gouzevitch: CMS iRPC FEB development and validation

CMS

FEB calibration

DAC T vs Charge Measurement setup considerations





Calibration factor = 4.6 ± 0.5 fC/DAC T

THR: Specification $50 \text{ fC} \Leftrightarrow 11 \text{ DAC T}$ Used in test beams $32 \text{ fC} \Leftrightarrow 7 \text{ DAC T}$



TDC time resolution



Pure TDC time resolution was measured using 2 channels test and a reference.

- <u>TID passed</u> (γ's) -- Facility ENEA Casaccia Calliope ⁶⁰Co : Requested: 20 Gy Certified:
 - FPGA Cyclone V (50 Gy):
 - Petiroc (160 Gy);
 - Power supply zone (100 Gy)





2) <u>TNID passed</u> (neutrons) - Facility FNG Frascati, with support from RADNEXT March 2022

Requested: 2.5e12 neq1MeV/cm²: Certified: 2.5e12 neq1MeV/cm²:

3) <u>Neutron flux passed</u> -

Requested: 50.000 neq1MeV/cm²/s Certified: Up to 10 requested flux

4) <u>SEU</u> (charged hadrons) - Foreseen in CHARM, CERN in Oct. 2022

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Exemple of iradiation map



FEB power consumption

Total consumption: 2V*6.3A+4V*2.3A = 22 W



Hottest elements:

- linear regulators Ohmic effect
- Optical communication
- FPGA logic

Cooling system

- Thermal pads + copper plate
- 2) Cooling pipe
- 3) Cool water: 15 C

Max temperature < 50 C

Play also the role of grounding plane



CONCLUSIONS

- Non-rad hard FEBv2 with Cyclone V FPGA is designed and certified.
- Time and threshold calibration finalised.
- Feb integrated into the Chamber
- The rad tolerance of the FEB seems to be higher than expected. Tests for SEU are ongoing.
- Rad hard FEBv3 with PolarFire FPGA is ready for prototyping.



IN MEMORIAM

Claude Girerd left us 26/08/2022 after a long illness.

- One of the most brilliant French electronics engineers in HEP.
- <u>2006 Crystal Medal of the CNRS for</u> <u>FEB for OPERA experiment.</u>
- Technical coordinator of iRPC electronics project from 2019 to 2021. Lead FEBv2 design and certification.

CLAUDE GIRERD L'EXPÉRIMENTATION AVANT TOUT



des systèmes p responsabilités

dui le passionn appliquées (Ins appliqué à la re Il participe nota projet d'imager au Laboratoire systèmes instr la micro-électr avant de reveni au sein de l'IPN confier la respo la mise en œuv de l'expérience souterrain de E consiste à obse au Cern, à 730 les Alpes. Le br de nature et de neut devenir ur

« PARTICIPER EXPÉRIENCE, L'INSTRUMEN EFFECTUÉES :

L'architecture (

BACKUP





Validation en radiation gamma



Caliope a ENEA Casaccia a côté de Rome





FEB certification steps

FEB Test Bench - In Lyon (IN2P3/IP2I)

Based on the **FC7 acquisition** system and controlled by **Python software** tools.

- Perform a Quality Check Process to validate :
- Each electronic block of the FEB independantly (SCA, GBTx, Power Supplies, tests points)
- The data integrity of the system
- The operation of the FEB firmware designed in the FPGA(s)
- The operations of the TDC(s) and Asics(s)
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Test bench in IP2I Lyon



LINUX





FEBv2 logical scheme



M. Gouzevitch: CMS iRPC FEB development and validation



Expected Fluence and Dose at HL-LHC









Expected fluence and dose (RE34/1 FEBs)

- at R=303 cm for RE3/1 is ~4.3 (5.8) x10¹¹ n/cm², and
- at R=304 cm for RE4/1 it is about 6.2 (8.2) x10¹¹ n/cm²,
- at R=303 cm for RE3/1 is ~10 (13.6) Gy
- at R=304 cm for RE4/1 it is about 18 (24) Gy
- where R=303 (304)cm are the expected FEB positions
- Expected fluence and dose (Balcony)
 - The total irradiation fluence 800 x 10⁹ cm⁻²
 - Maximum integrated dose is about 10 Gy





Behzad Boghrati, Radiation Hardness of Electronics for Phase-2 Upgrade of RPC Muon System, RPC Workshop, 31 Aug. – 1 Sep

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