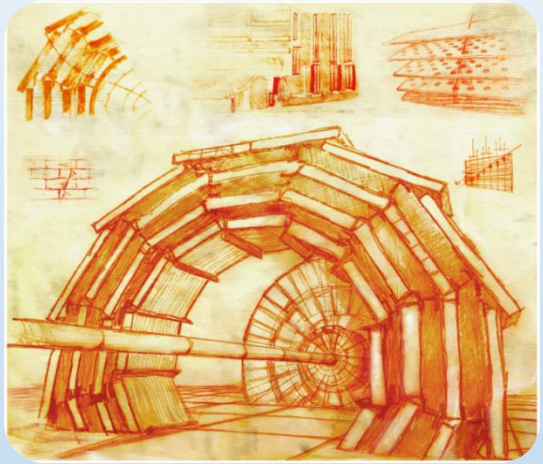
96-channel Time-to-Digital converter (TDC) for the CMS Phase 2 Upgrade of the RPC Link System



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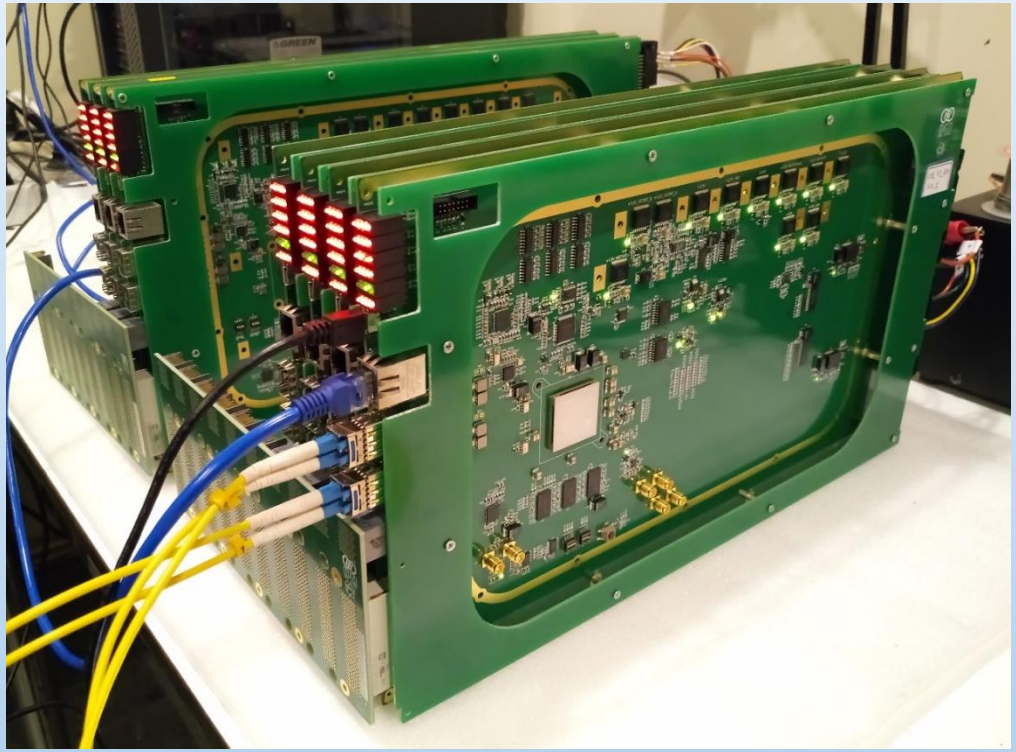
on behalf of CMS Muon Group

RPC 2022

XVI Workshop on Resistive Plate Chambers and Related Detectors

Outlook

- ✓ Overview on the RPC Phase-2 Upgrade Projects
- ✓ RPC Link System upgrade motivation
- ✓ New Link System features
- ✓ RPC Signal and Data Processing
- ✓ Time-Stamping on RPC hits
- ✓ Time-to-Digital Converter Transfer Function
- ✓ Result and Validation
- ✓ Conclusion

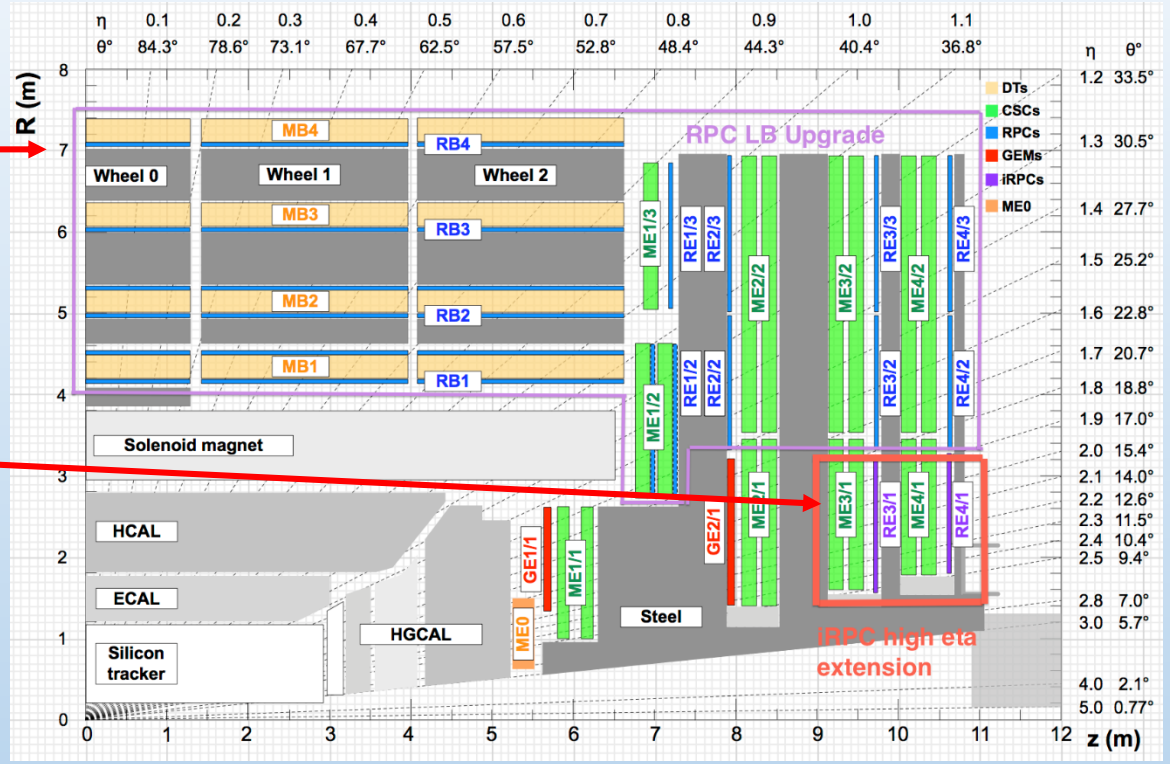


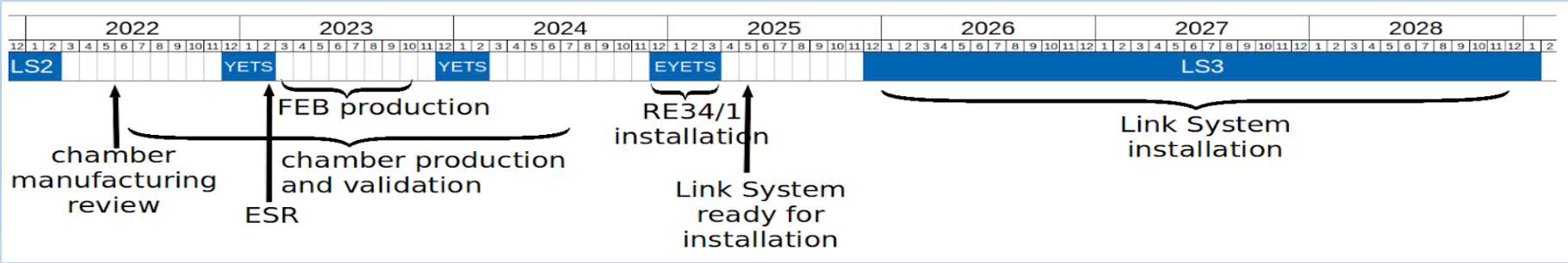
RPC Phase-2 Upgrade Project for HL-LHC

RPC upgrade Project scope:

1. **New electronics for the legacy detectors:**
   - Replace all off-chamber electronics, Backend Electronics (BE)
   - To improve timing resolution for existing RPC (|h | < 1.9).
   - Installation and commissioning in LS3 (2026-2027)

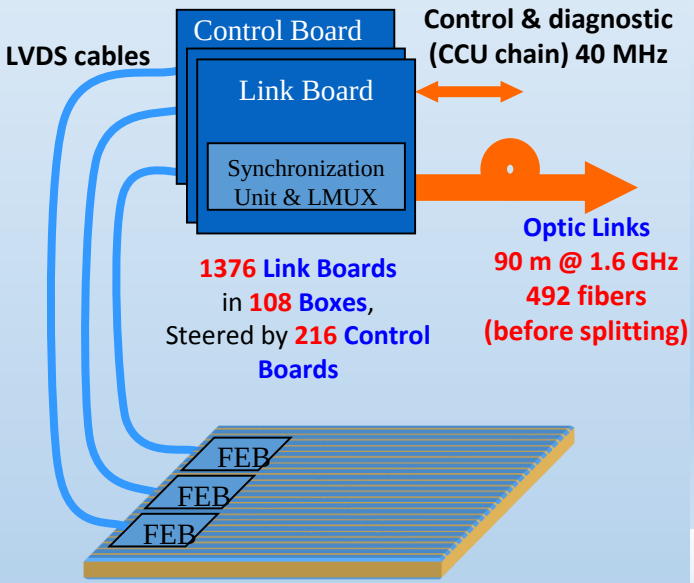
2. **New detectors:**
   - To Extend the RPC coverage up to |η | = 2.4, and
   - Increase redundancy in high eta region in stations 3 and 4.
   - Installation in YETS 2024-25.





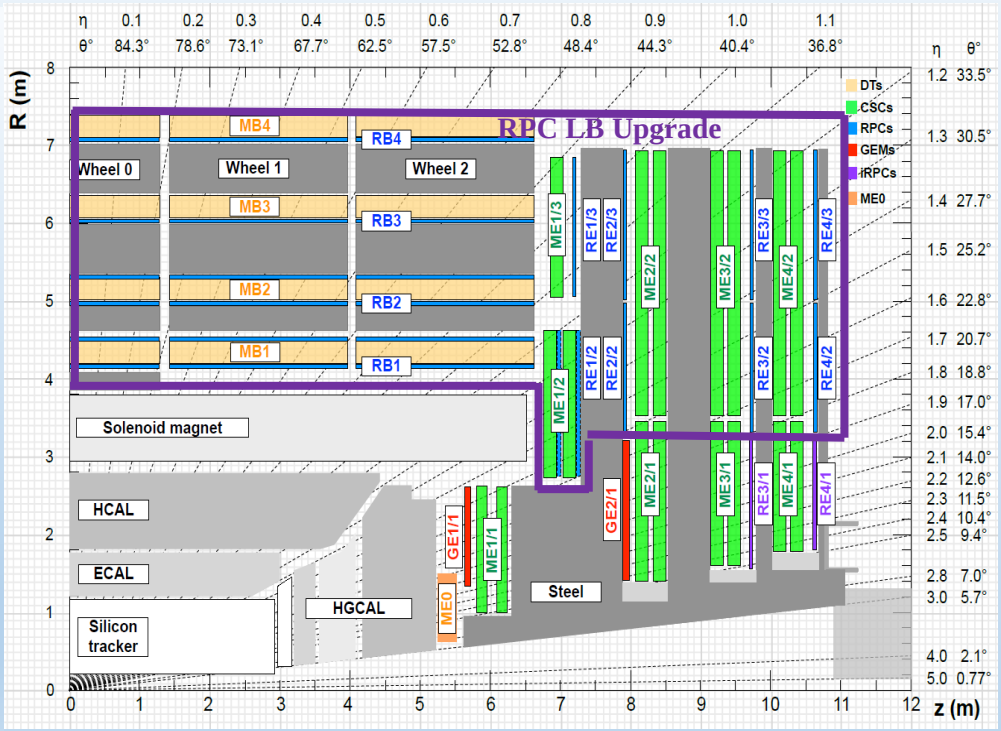
Present RPC Link System - Upgrade Motivation

Present RPC Link System



Upgrade Motivation

- RPC signals synchronization, timing resolution is 25ns
- Data transmission speed is about 1.6 Gbps
- Control, diagnostic and monitoring of the Link system has been designed based on CCU ring (combination of copper cable and fiber optic), very susceptible to electromagnetic interference



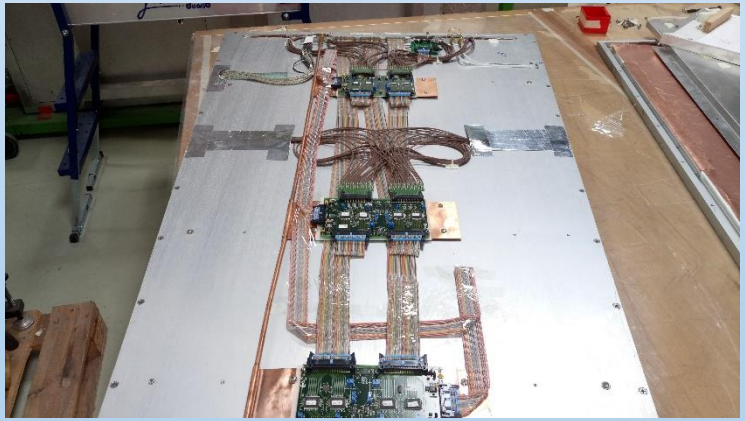
- CCU ring is not very fast, the bandwidth (40 MHz) share between 12 control boards
- Most radiation hard electronic components are obsoleted
- Electronic aging, presently the Link system at the end of LS2 is already 13 years old

Present RPC System Ingredients

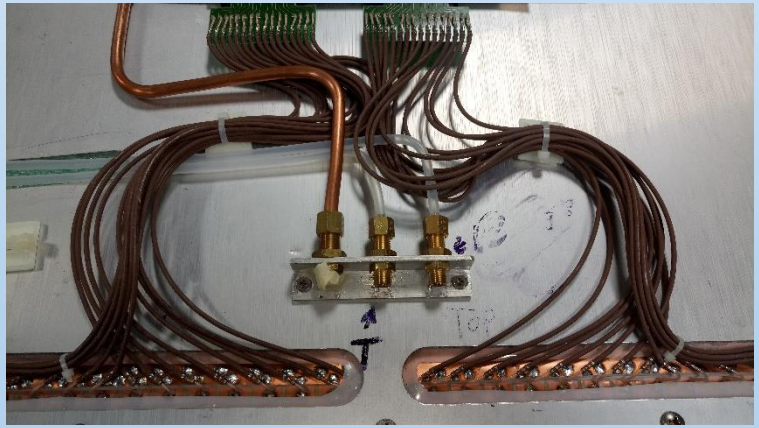
RPC Endcap Chamber

Front-end Board

Link Board



On-detector Electronics



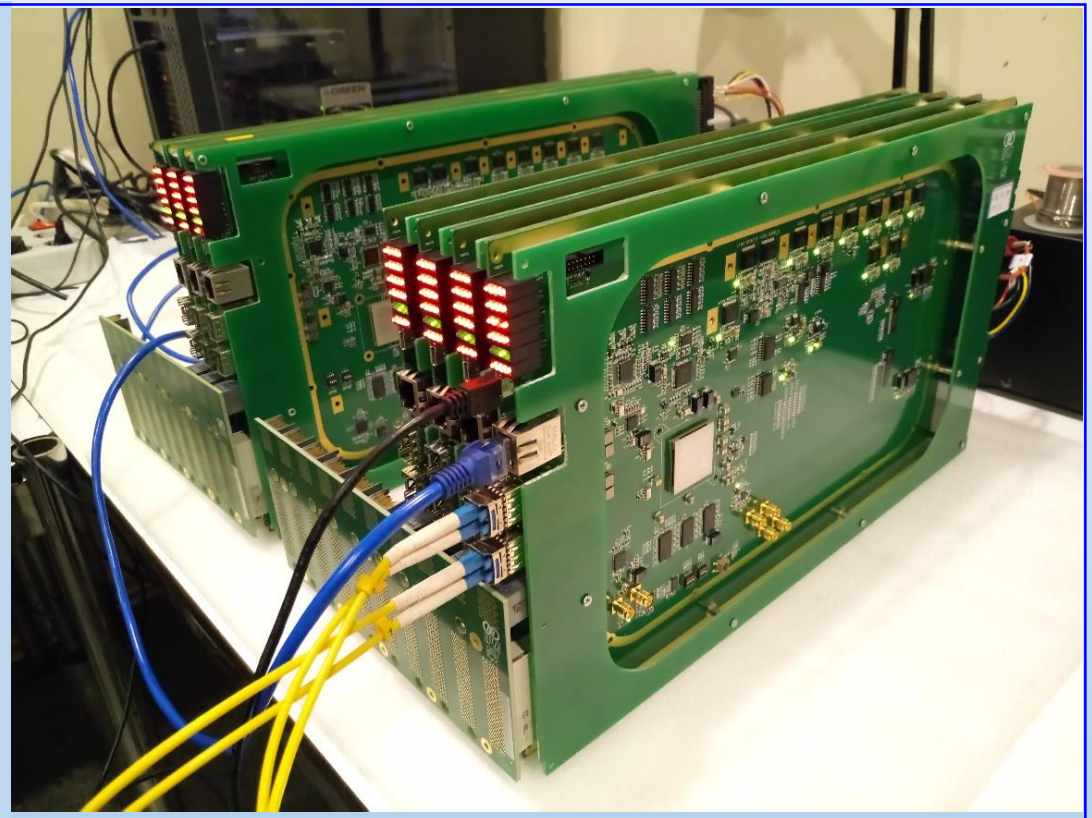
RPC Strips, Coaxial cables, Cooling and Gas Pipe

Link System

Link System for Phase-2 Upgrade

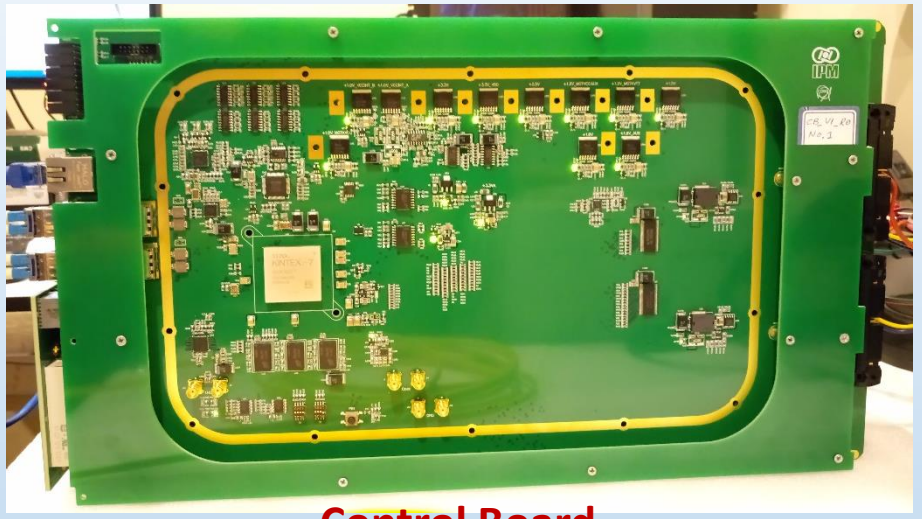
New Link system Features :

1. FPGAs are KINTEX-7, XC7K160T – Industrial Version
2. Muon hit time, TDC timing Resolution : 1.56ns
3. Master Link board output data rate : < 10.24 Gbps
4. Control Board communication with slow controller at < 10.24 Gbps
5. Embedded internal buffer (DDR3) : 4 GByte
6. Radiation Mitigation: TMR + Internal Scrubbing
   - Scrub Rate of entire FPGA (Real time SEU detection and Correction) : 13ms (31,770 times faster than the rate of SEU at the Balcony)
   - SEU at the Balcony : Every 413000 ms
7. Safety Systems:
   - Over & Under Voltage Protection
   - FPGA Over Temperature Protection
   - Transient Voltage Suppressor
   - ESD Protection (15 kV)



Link System for Phase-2 Upgrade

- **Control Board:**
  - The main bridge between Slow Controller and Link Boards
  - Optical Links to receive TTC, Fast, and Slow commands. GBT-FPGA link driver.
  - TTC clock and Fast BGo commands, BC0
  - TTC Clock Phase shift adjustment
  - FEB Parameter Configuration and Verification.
  - Control and monitoring the Link Boards Histograms, Data Logs and Diagnostics through front panel bus.

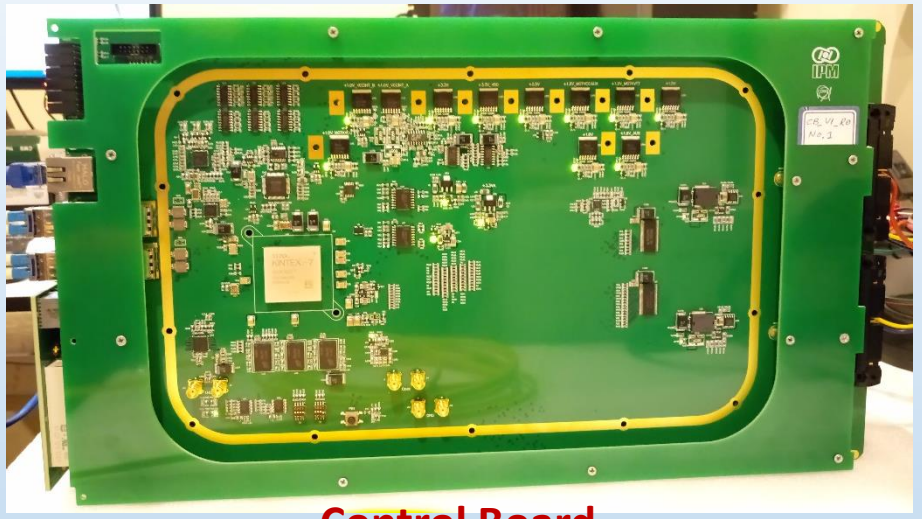


Control Board

Link Board

Link System for Phase-2 Upgrade

- **Link Board Main Functions:**
  - 96 Input Channels. 15 kV ESD protected.
  - 24 output Channels to trigger the FEB to check the FEBs, Flat cables, and all interface connectors.
  - Detector Diagnostic and monitoring:
    - Full/Close window Histograms
    - RPC Data logging
    - Timing Histogram
  - Muon Hit time information with a TDC resolution of 1.5 ns.
  - Collects 42 hits per Bunch Crossing without buffer overflow and data loss.
  - Transmit 21 hits per Bunch Crossing to the L1T through 10 G optical Link.
  - Voltage, Current, temperature, and Radiation Protection features.



Control Board

Link Board

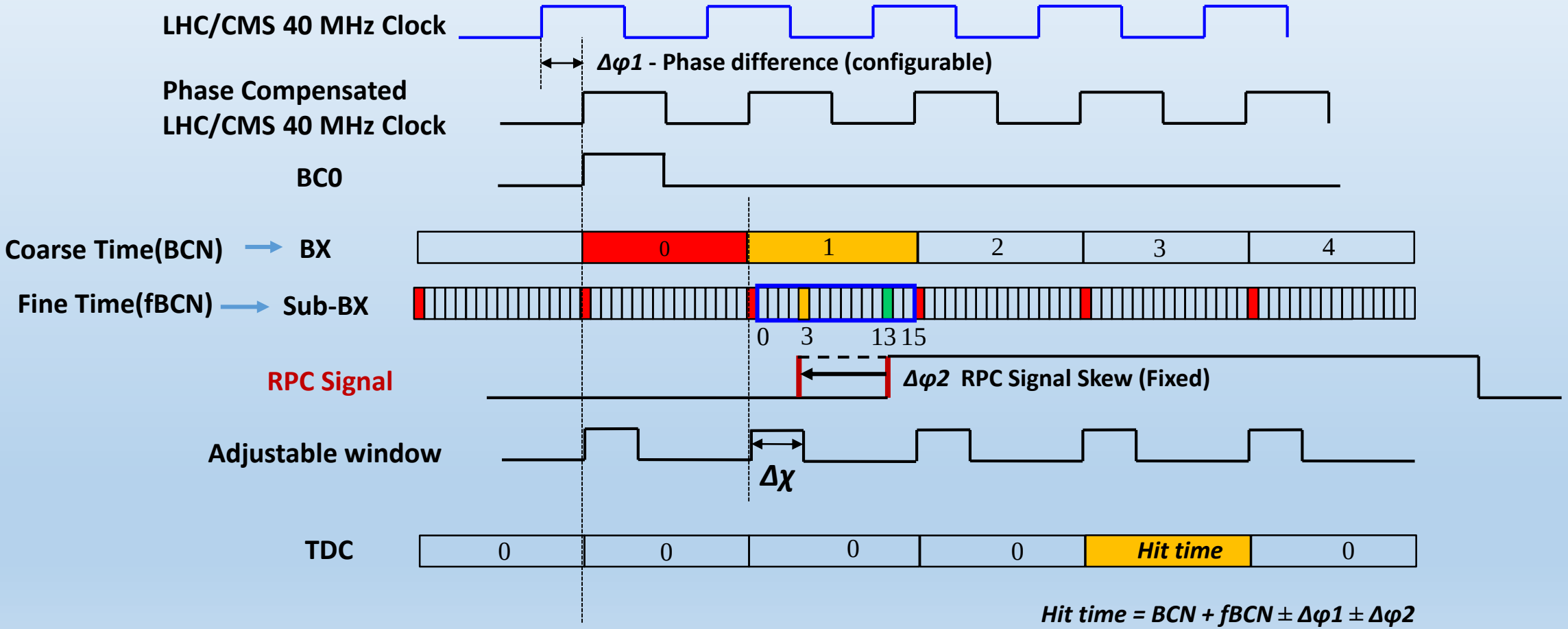
RPC Signal and Data Processing

1. **Signal Conditioning;** Single LVDS signal (pair of wires/pins) for each RPC channel (strip). RPC hit is a pulse of 100ns.
   - Each LB receives 96 RPC channels i.e. full Endcap RPC (3 eta rolls),
   - or one roll of barrel RPC.
2. **Impedance Matching;** According to the LVDS standard, the line should be terminated on the receiver side by ~100 Ω resistance inside the LVDS line receiver chips.
3. **Time-Stamping;** the signals are asynchronous, and the rising edge of the pulse brings information about the RPC hits timing (the signals are not synchronous to any clock). Time-Stamping unit measure the arrival time of rising edge of the pulses with respect to the corresponding bunch crossing.
4. **Latency Compensation;** Both of RPC signal and received TTC clock has delayed with respect to the main bunch crossing and they should be fixed at first. RPC signal delay and TTC clock phase shift compensator.
5. **Data collection and transmitter;** Information of 42 fired strips at each bunch crossing are selected and buffered by the data collector inside of the Link Board FPGA. In one bunch crossing information of 7 hits from one Link Board will be send to the Master Link Board. In Master Link board, the data of two adjacent Link boards are collected and merged with its own data. At Final, information of 21 hits of current bunch crossing will send to the next layer of the trigger.

RPC Signal and Data processing – Time-Stamping

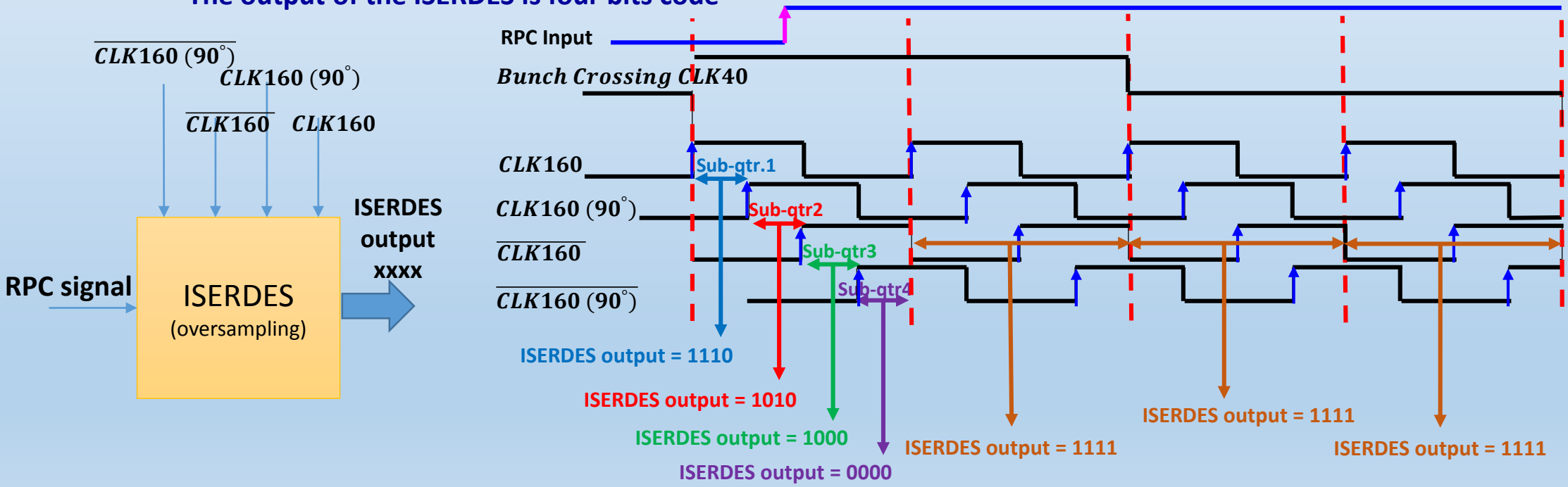
- **RPC signals time Stamp**

  The first step of the RPC signal processing is the measurement of RPC signal arrival time and assignment of this data to the phase compensated LHC/CMS clock (40 MHz) .

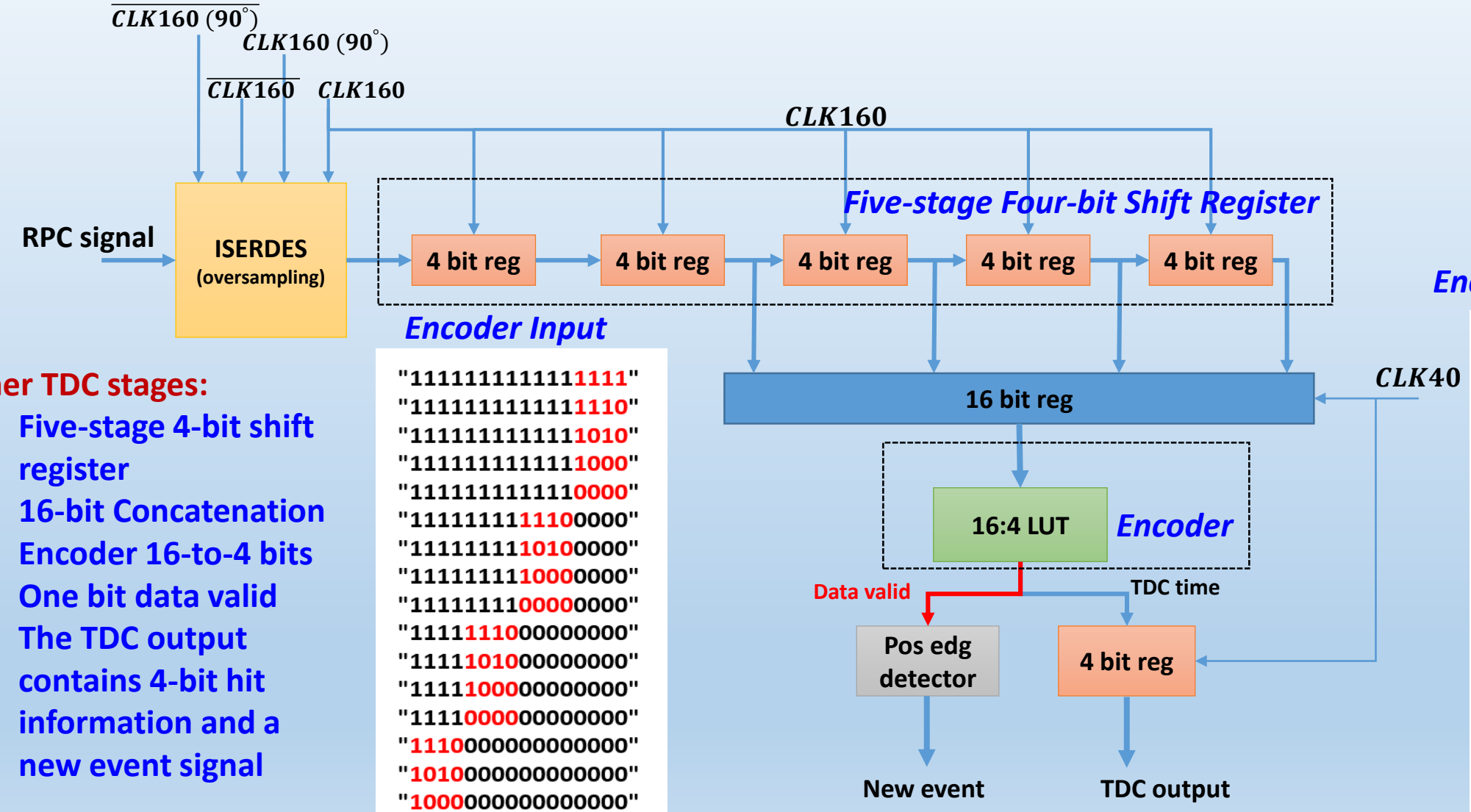


RPC data processing – Time-Stamping

- **RPC signals time-Stamping on RPC hits**
  - Time-to-Digital Converter (TDC)
  - In TDC the first stage is the Input Serial/De-serial (ISERDES) DIGITIZAER unit.
  - It needs four Clocks, four times higher than the reference clock (Bunch Crossing). Take four samples on every quarter of the reference Clock
  - ISERDES is a hardware built-in component inside the FPGA
  - The main function of ISERDES is to serialize the RPC input signal at the specific sampling rate
  - The output of the ISERDES is four bits code



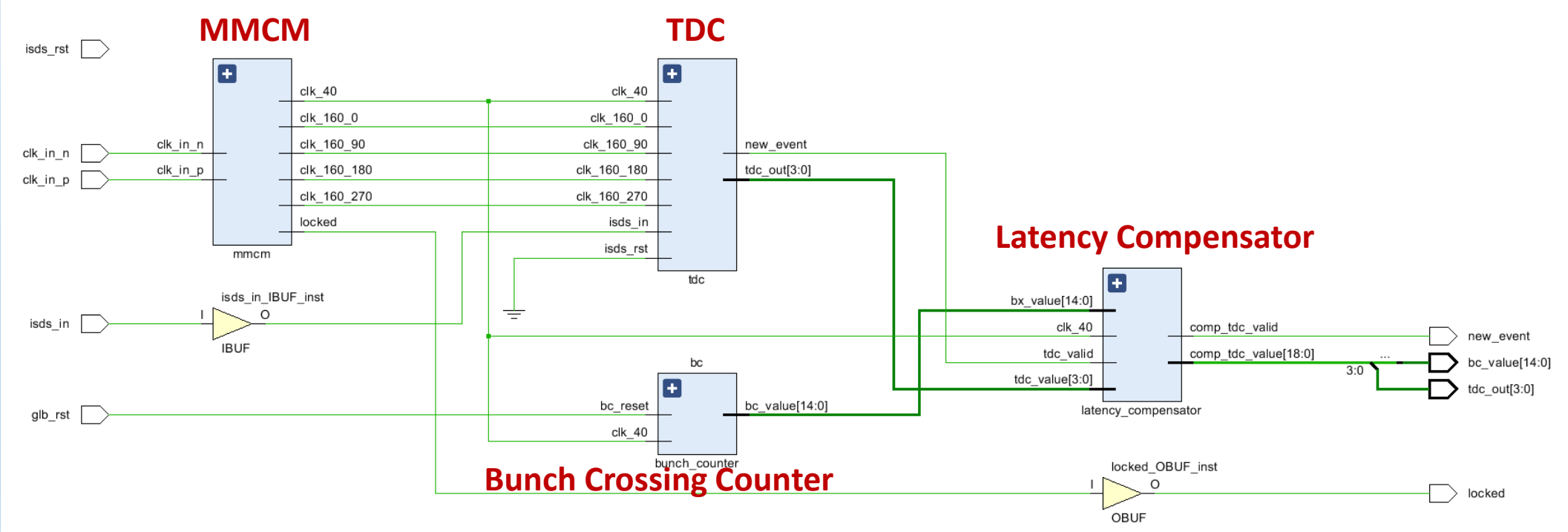
RPC data processing – Time-Stamping



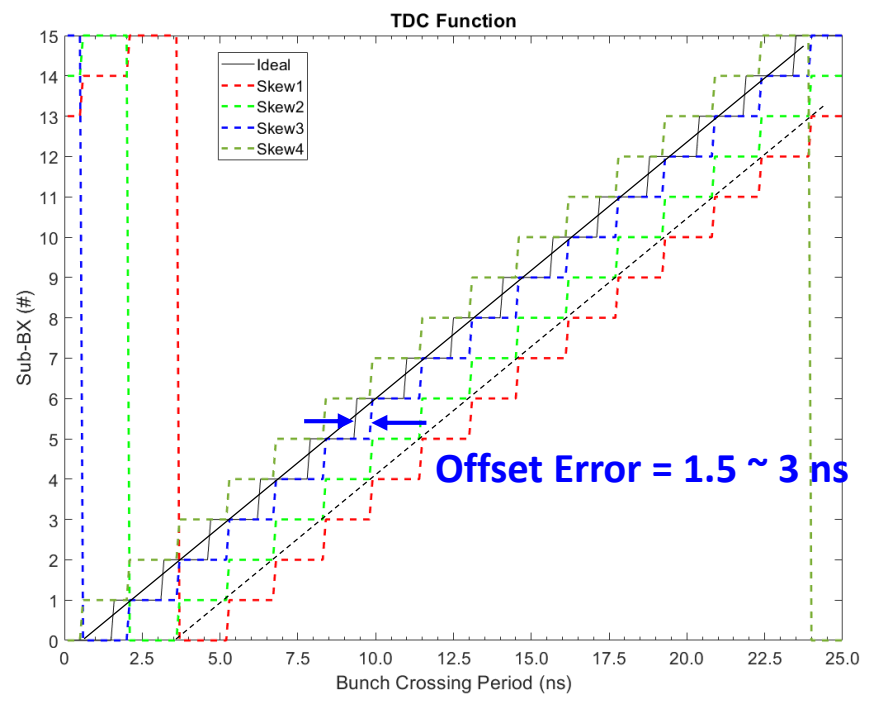
- **Other TDC stages:**
  1. Five-stage 4-bit shift register
  2. 16-bit Concatenation
  3. Encoder 16-to-4 bits
  4. One bit data valid
  5. The TDC output contains 4-bit hit information and a new event signal

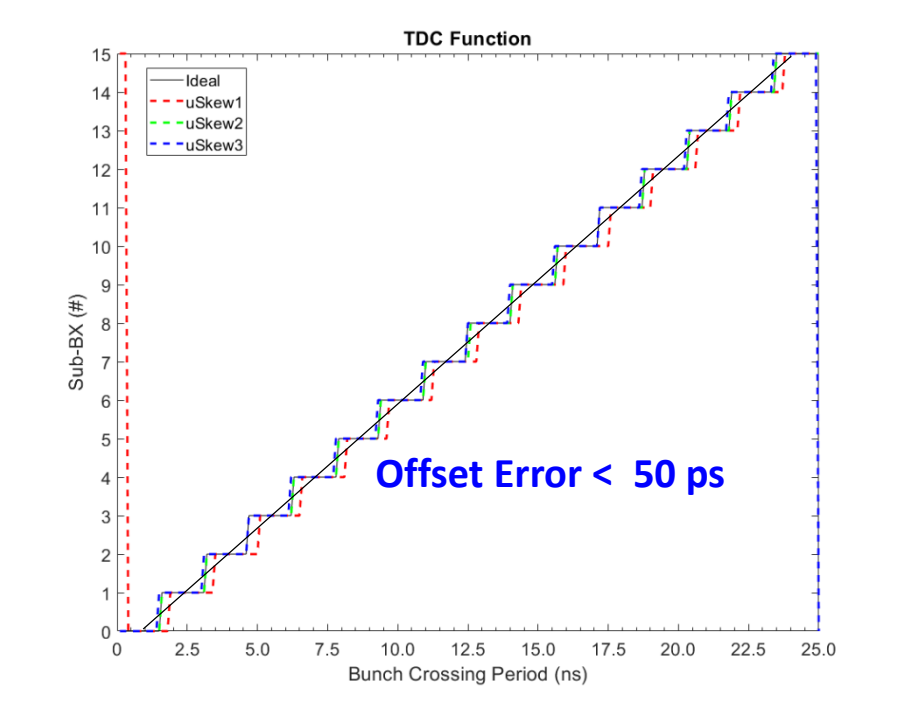
Time-Stamping – FPGA Implementation

- **Time-Stamping stages in FPGA:**
  1. MMCM generate four-phase shifted clocks at frequency of 160 MHz
  2. Time-to-Digital Converter, fine-time measurement.
  3. Bunch Crossing Counter is implemented by a 15-bit Counter, coarse time measurement.
  4. TTC Clock Latency and RPC signal propagation delay are compensated by the Latency Compensation unit.



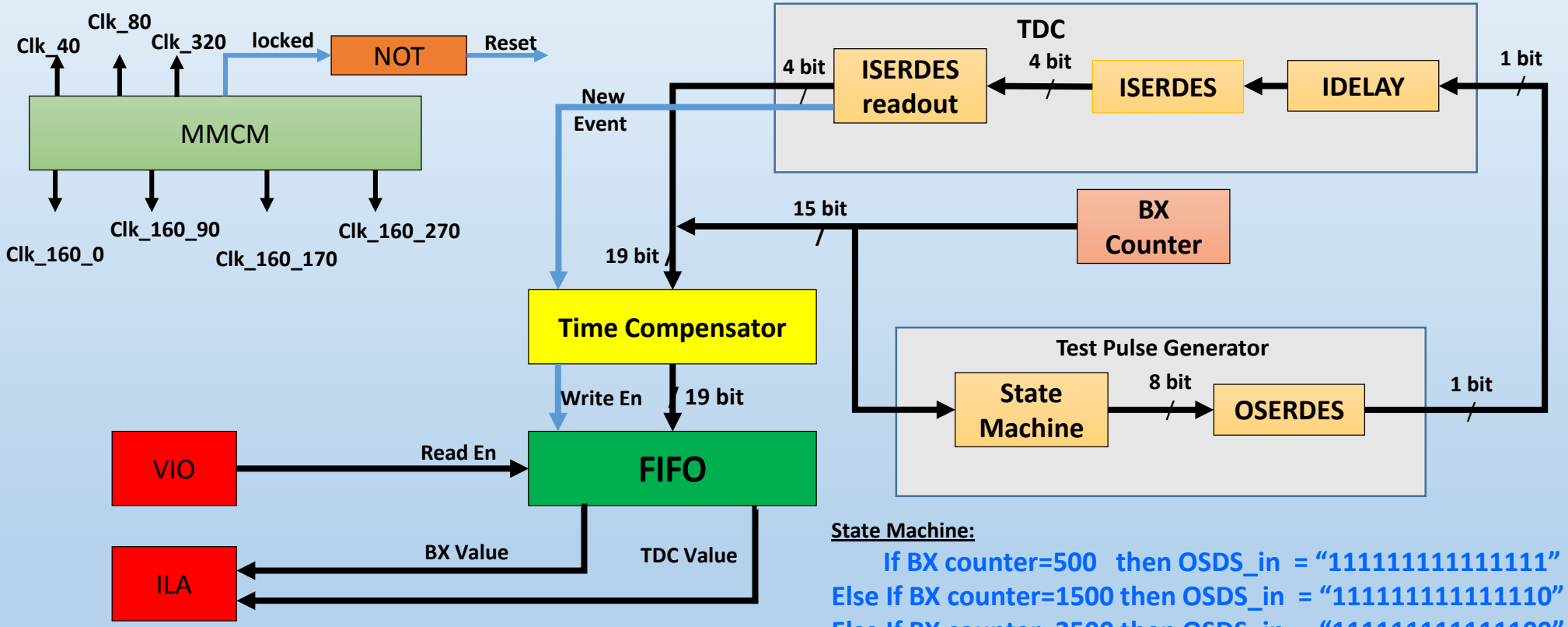
Time-Stamping – TDC Transfer Function





- TDC resolution is 1.56 ns. The gain error is zero but offset error is not.
- TTC clocks and RPC hit signals has delays w.r.t the origin of LHC clock. This cause a fixed offset error on the TDC transfer function.
- In Link Board, the TDC data is compensated with two parameters; 1) Macro steps : **1.56 ns**, and 2) Micro steps: **48 ps**. Figure left, Macro step offset error compensation, and Figure right, Macro + Micro steps offset error compensation.

Time-Stamping – Validation

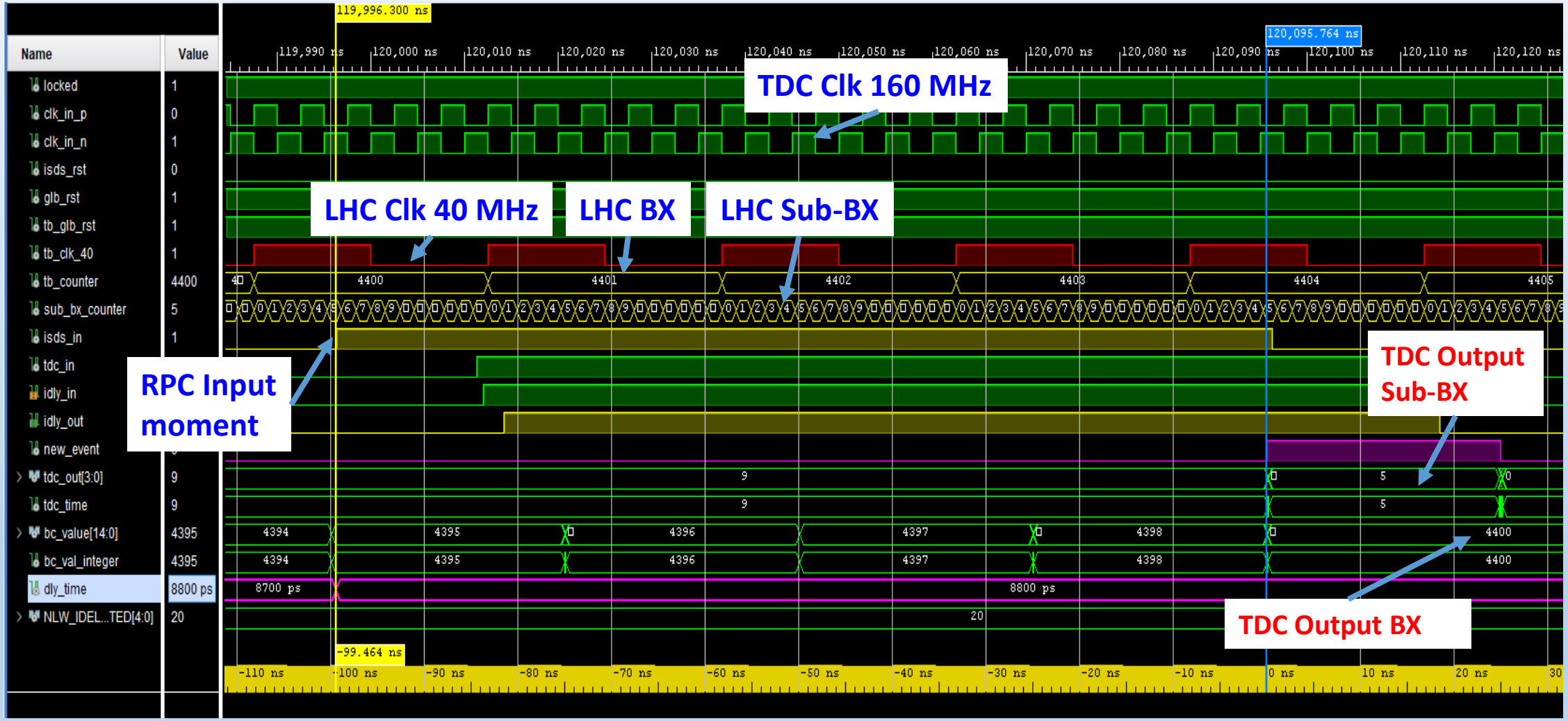


State Machine:

If BX counter=500 then OSDS_in = "111111111111111"
Else If BX counter=1500 then OSDS_in = "111111111111110"
Else If BX counter=2500 then OSDS_in = "111111111111100"

.
.
.

Time-Stamping – Validation

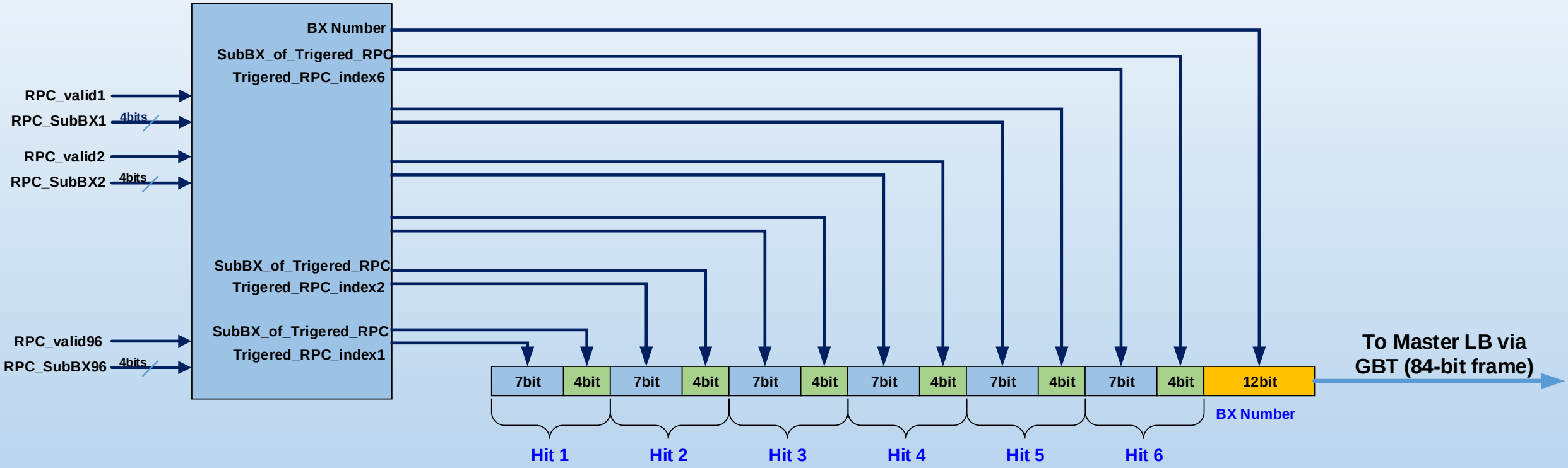


Conclusion

- The phase-2 upgrade of the RPC Link System was reviewed. Five fundamental steps are needed for RPC signal and Data Processing. Signal impedance matching, Signal standard conversion from LVDS to single-ended, TDC for time-stamping, zero latency data collection, and data transmission.
- The TDC unit measures the rising edge moment of the RPC input signal to bunch crossing. The main elements of the TDC are the ISERDES, five-stage four-bit shift registers, 16-bit concatenation, data encoder 16 to 4-bit, and a new event detector.
- This unit is designed based on the hardware-built-in ISERDES. The sampling time of the input RPC signal is 1/16 of a bunch crossing period. The time resolution of the TDC is 1.52 ns.
- The linear transfer function of the TDC shows the necessity of latency compensation. Therefore, this unit is included to the TDC.
- Test and validation of the TDC has been done successfully.

Backup Slides

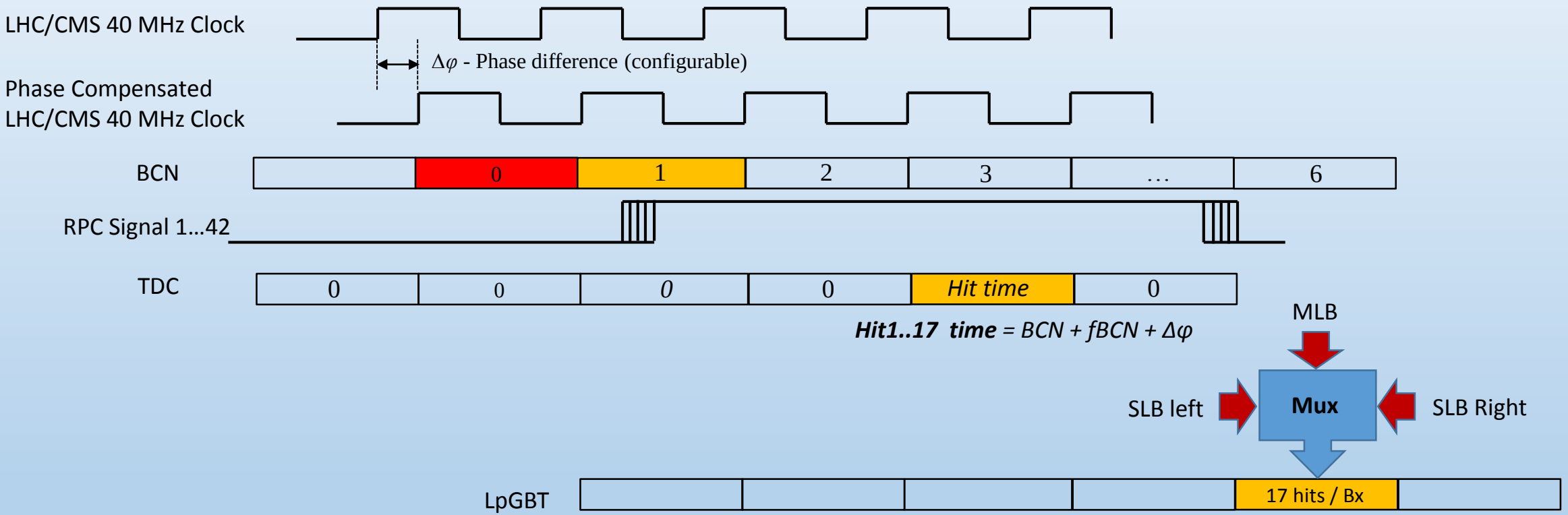
RPC data processing - Data Collector and Transmission



Total Number of bits = (6 x 11) + 12 = 78

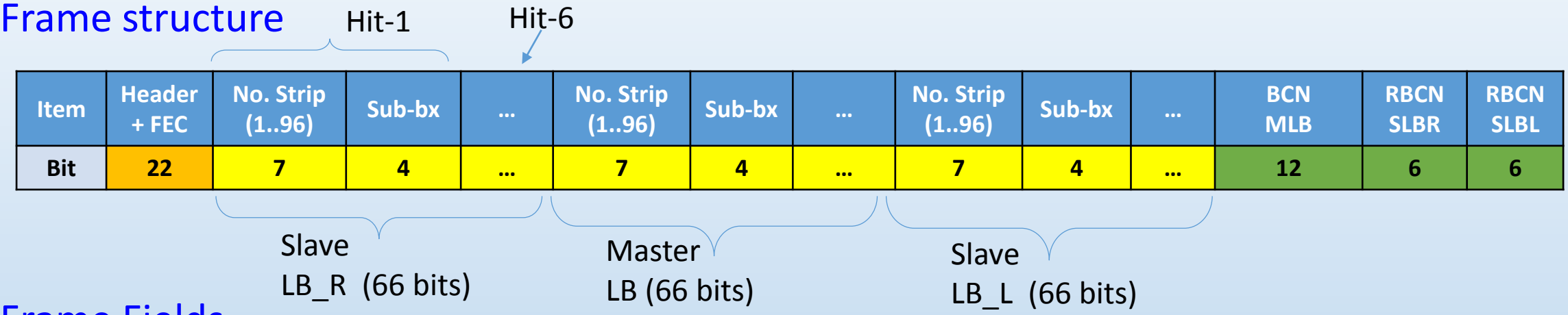
- Data of UP to **6 fired strips (activated channels)** are transmitted per BX clock cycle.
- Bursts with up to **42 activated channels** can be transmitted without data loss.
- In Burst cases, channel data are transmitted with a delay.

RPC data processing - Data Multiplexing and Transmission



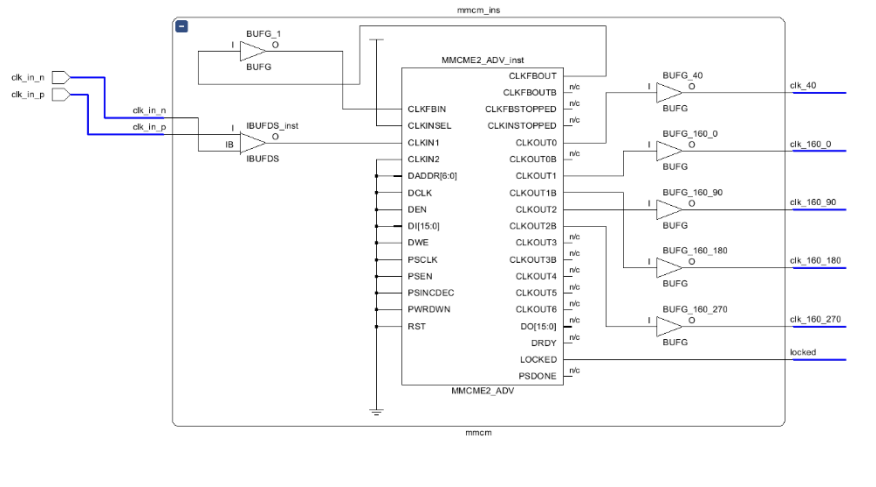
RPC Link System - MLB Frame structure

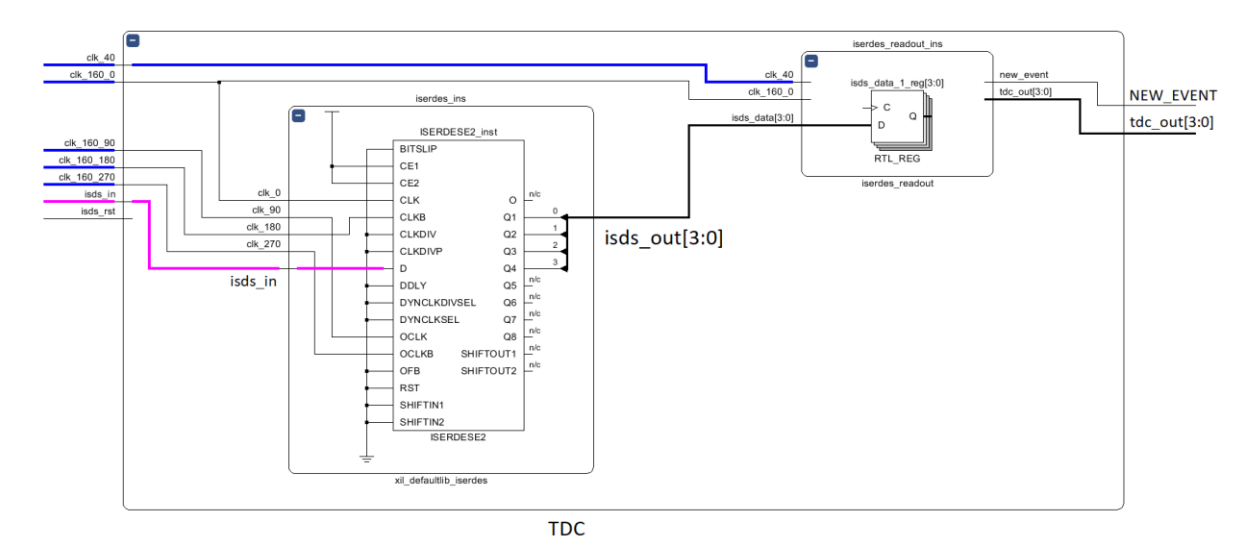
- Frame structure

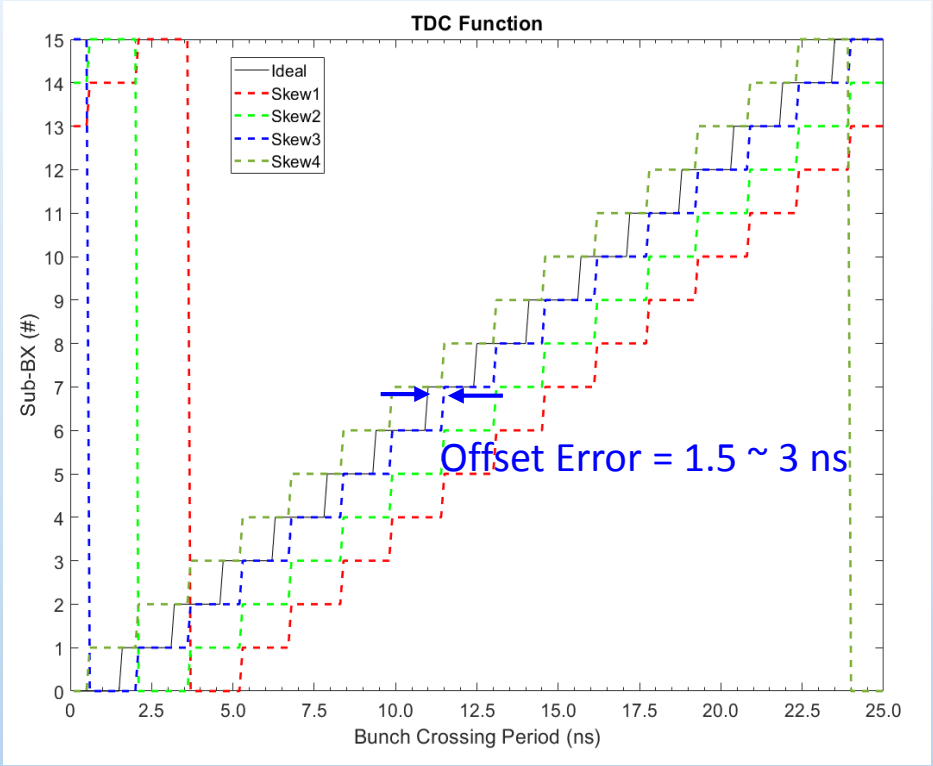


- Frame Fields
  - **Header** (2 bits) + **FEC** (20 bits)
  - **Hit information**
    - **Number of fired strip** which could be between strip no. 1 to strip no. 96. Size of this field is 7 bits.
    - **The Sub-BX** or fractional part of the hit time of a fired strip. The size of this field is 4 bits.
  - The number of the Bunch Crossing keeps in the **BNC field**.
  - Master LB Bunch Crossing is put in the **BCN MLB**.
  - Slave LB Right/Left Bunch Crossing number, **RBCN SLBR/SLBL**, are mentioned by their difference to the Master LB Bunch Crossing.
  - Frame size = 256 bits
  - Total Number of data bits = (3 x 66) + 12 + 6 + 6 = 222 bits

Time-Stamping – TDC Transfer Function







Time-Stamping – TDC Transfer Function