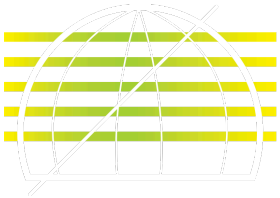

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96-channel Time-to-Digital converter (TDC) for the CMS Phase 2 Upgrade of the RPC Link System

Thursday, 29 September 2022 11:20 (20 minutes)

We describe a 96-channel Time-to-Digital converter (TDC) and its intended state-machines, implemented in field-programmable Gate Array (FPGA) for the CMS Phase 2 upgrade of the RPC Link System. It is realized as a 6U card, called Link Board and will be used at the High Luminosity LHC (HL-LHC). The TDC system operates at an RPC intrinsic time resolution of 1.56 ns, a minimum input pulse width of 3.12 ns, and a minimum separation of 3.12 ns between input pulses. The complete edge-detection and time-stamping process take up to four LHC bunch crossings. The time response of the TDC is four times shorter than the width of RPC output pulses. It guarantees that a pulse processing of each bunch crossing could be done real-time per each bunch crossing.

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