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CMS iRPC Backend and Front-End Electronics joint test

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CMS has started Phase 2 upgrade to prepare for the High-Luminosity LHC (HL-LHC). The improved Resistive Plate Chambers (iRPC) will be installed in the challenging forward region with new Front-End Electronics (FEE) to read each strip from both ends. The Backend Electronics (BE) provides fast/slow control for the FEB and performs trigger primitives, data acquisition, and readout. A joint test system was set up to verify the BE functionalities. The slow control based on IPbus was developed to realize functions like powering up and TDC correction for the FEE and configuration for the BE. Besides, the system efficiency was measured and cross-checked with the Lyon FC7 system to ensure the BE works normally.

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