CAEN Electronic Instrumentation

Tools for Discovery

Future perspective of Digital DAQ

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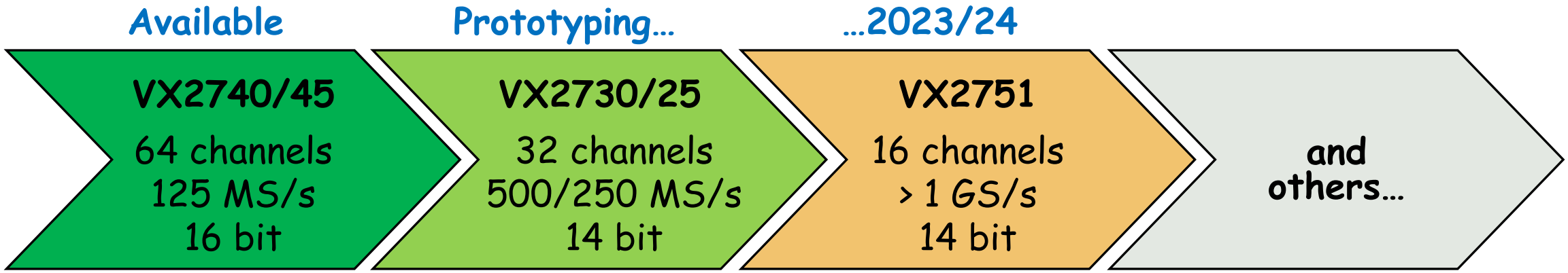
Introduction

Digital Detector Readout: TimeStamp, Amplitude (Energy) and Pulse Shape.

Two different approaches:

- **Stand-alone preamps + Waveform Digitizers with Digital Pulse Processing (DPP)**
  - Continuous A/D conversion and Signal Processing (no dead-time)
  - High throughput data transfer
  - Open FPGA for custom algorithms
- **Front-End ASICs + FPGA for Acquisition Logic and Readout Interfaces (Back-end)**
  - Tailored FE ASICs
  - Easy integration and scalability
  - Low cost/channel, Low power, Small dimensions

Digitizer 2.0 Roadmap



2740/2745 Digitizers

64 channel, 125 MS/s, 16 bit waveform digitizer

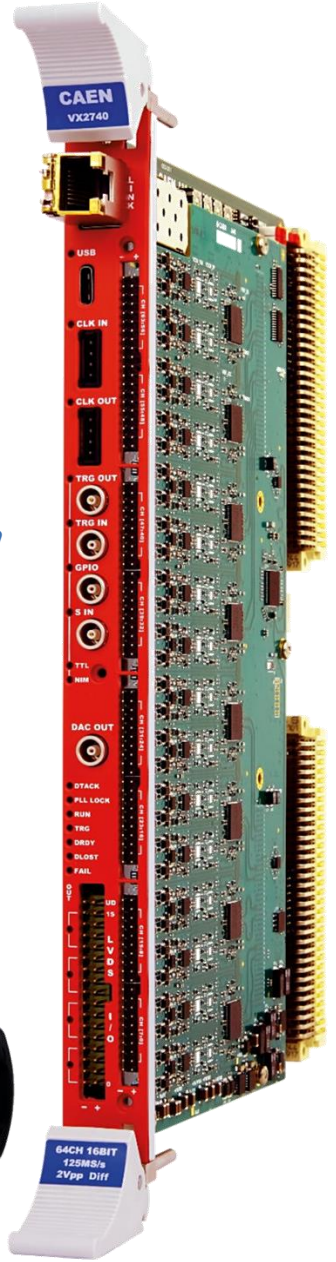
- Single Ended of Differential inputs (2 mm header connectors)
- **Dynamic Range**:
  - V2740 → 2 Vpp fixed
  - V2745 → 40 mV ÷ 4 Vpp (Gain from 0 to 40 dB in steps of 0.5 dB)
- Individual DC offset adjust over the full dynamic range
- Multiple **readout** interfaces: 1/10 GbE, USB 3.1, Optical Link
- **Open FPGA** to provide flexibility in the pulse processing algorithm
- **DPP** functionalities: PHA, QDC, PSD, CFD, Zero Suppression
- Embedded Linux **ARM**
- Form factors: VME64X, VME64 and Desktop

Good fit for:

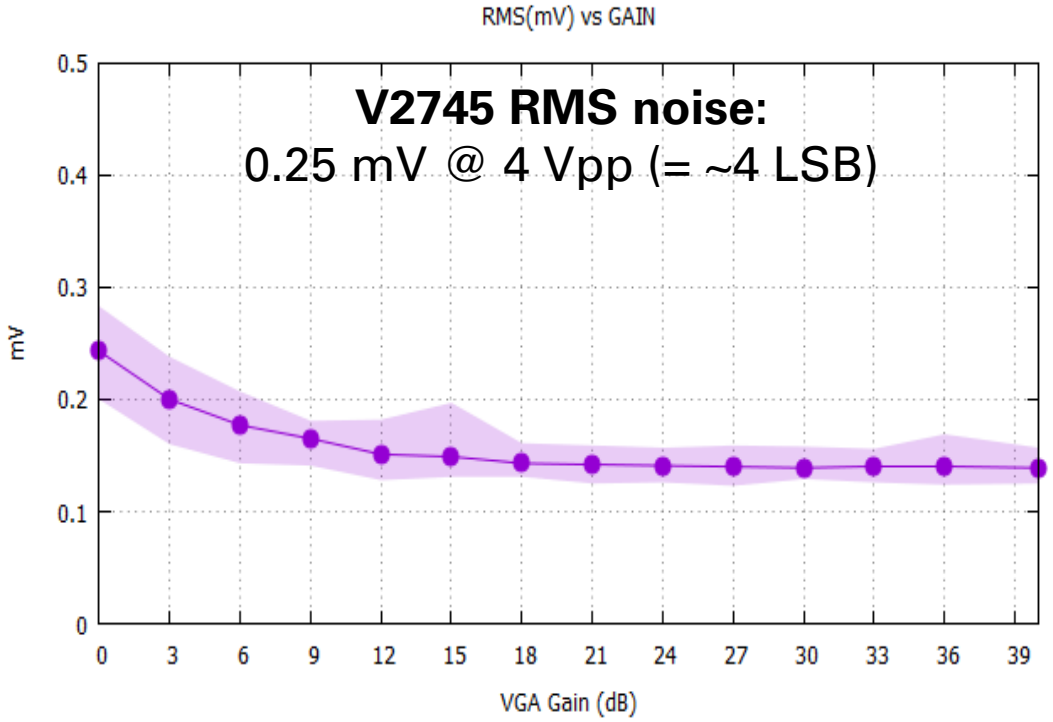
- *neutrino and dark matter experiments*
- *high channel density spectroscopy with Silicon and HPGe detectors*

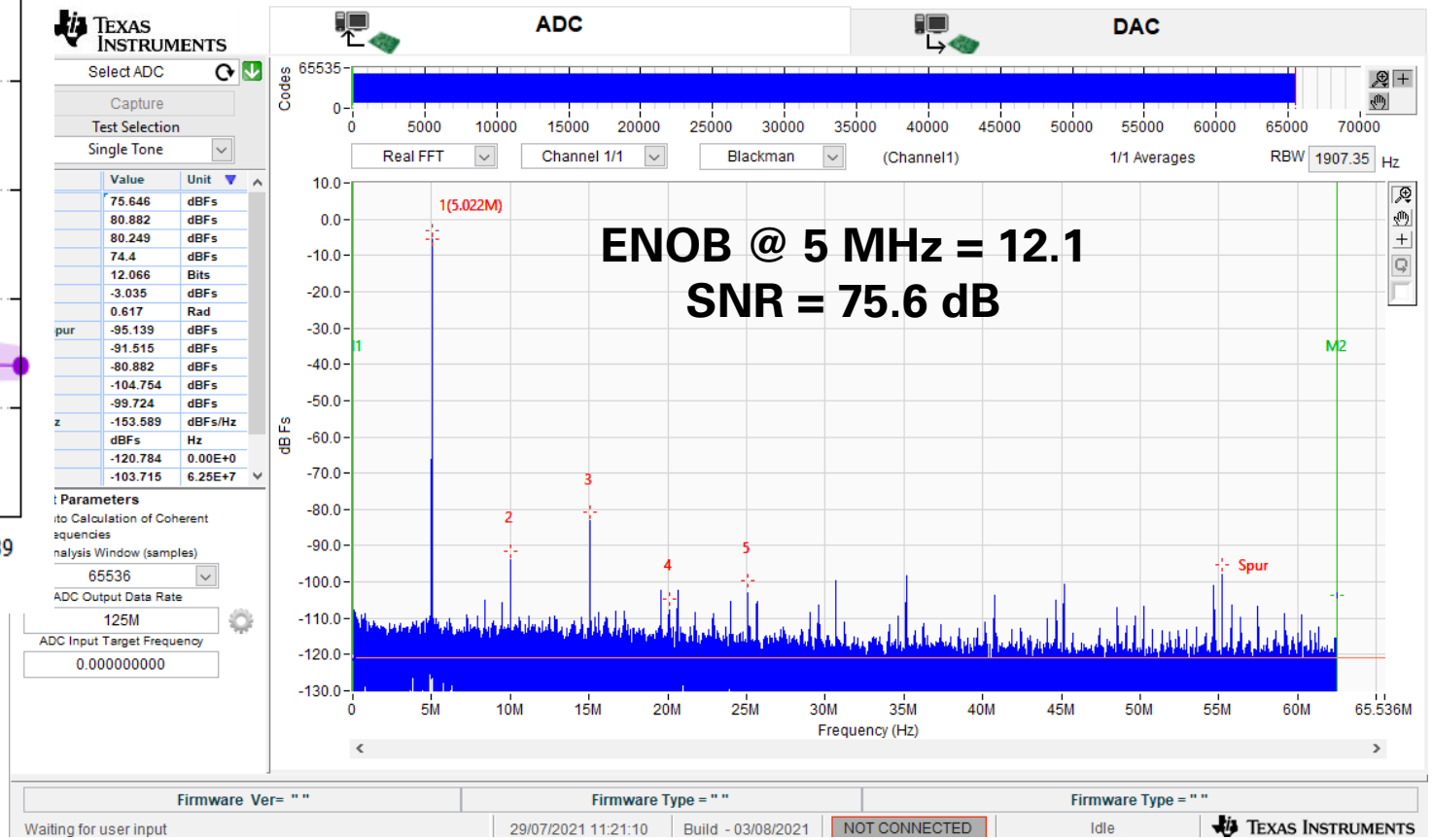
Currently used by:

- *Numen (SSD, SiC, $LaBr_3$)*
- *Dark Side (Argon TPC)*
- *Tristan (multi pixel SDD)*
- *… and others…*



Noise test

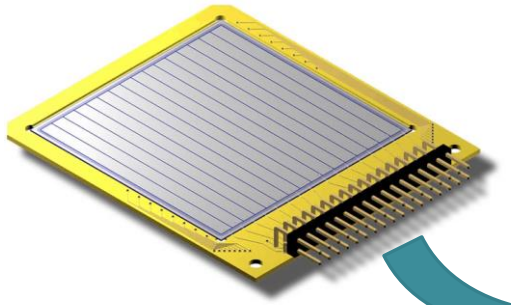




SSD readout @ Numen (LNS)

A1429
64 ch Charge Sensitive Preamplifier

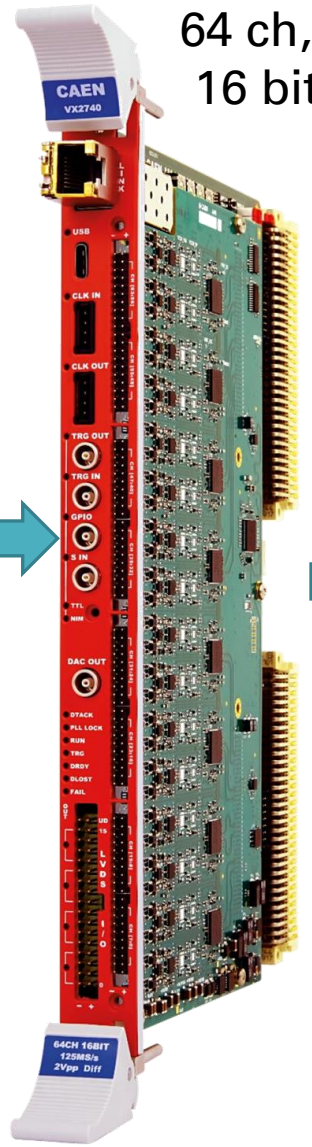
4 Vpp differential signals
1.27 mm Ribbon Cable



ERCD
MicroCoaxial Cable

A372F
Cable Adapter

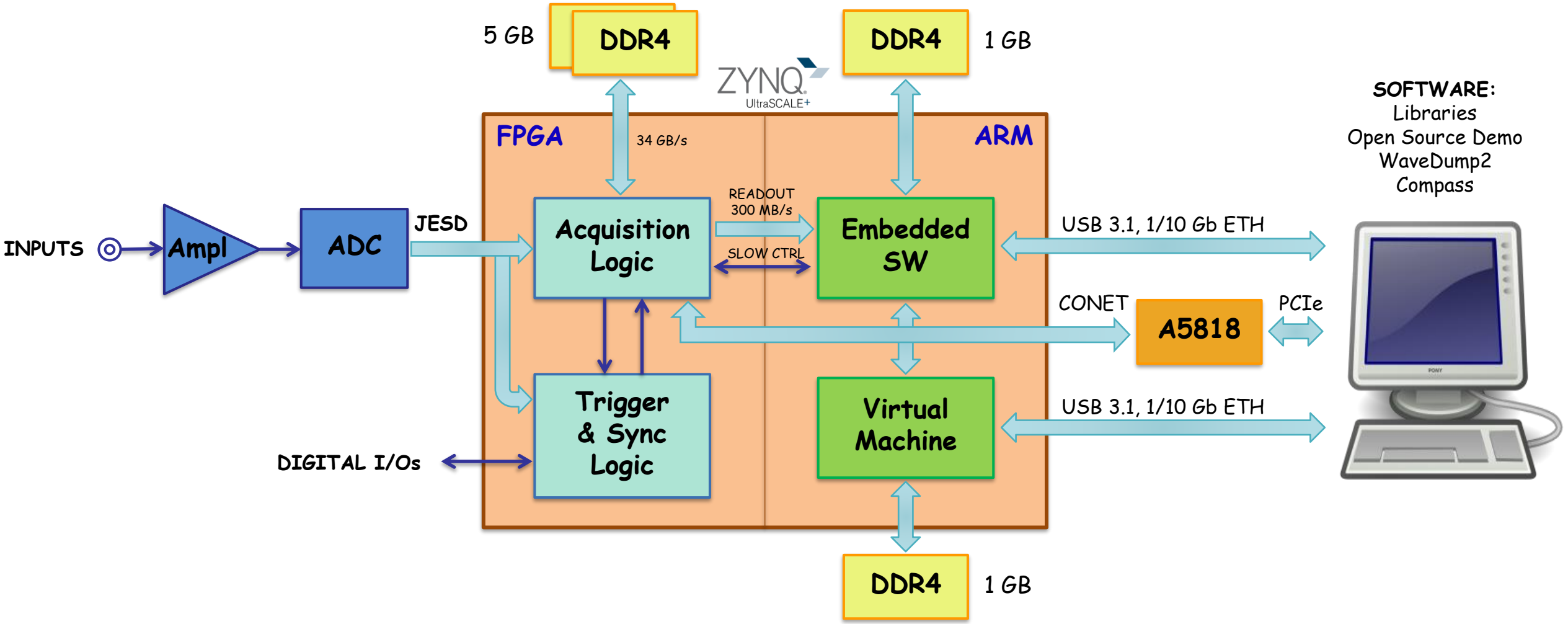
VX2745
64 ch, 125 MS/s
16 bit Digitizer



DPP
PHA

List Mode
Streaming
Readout

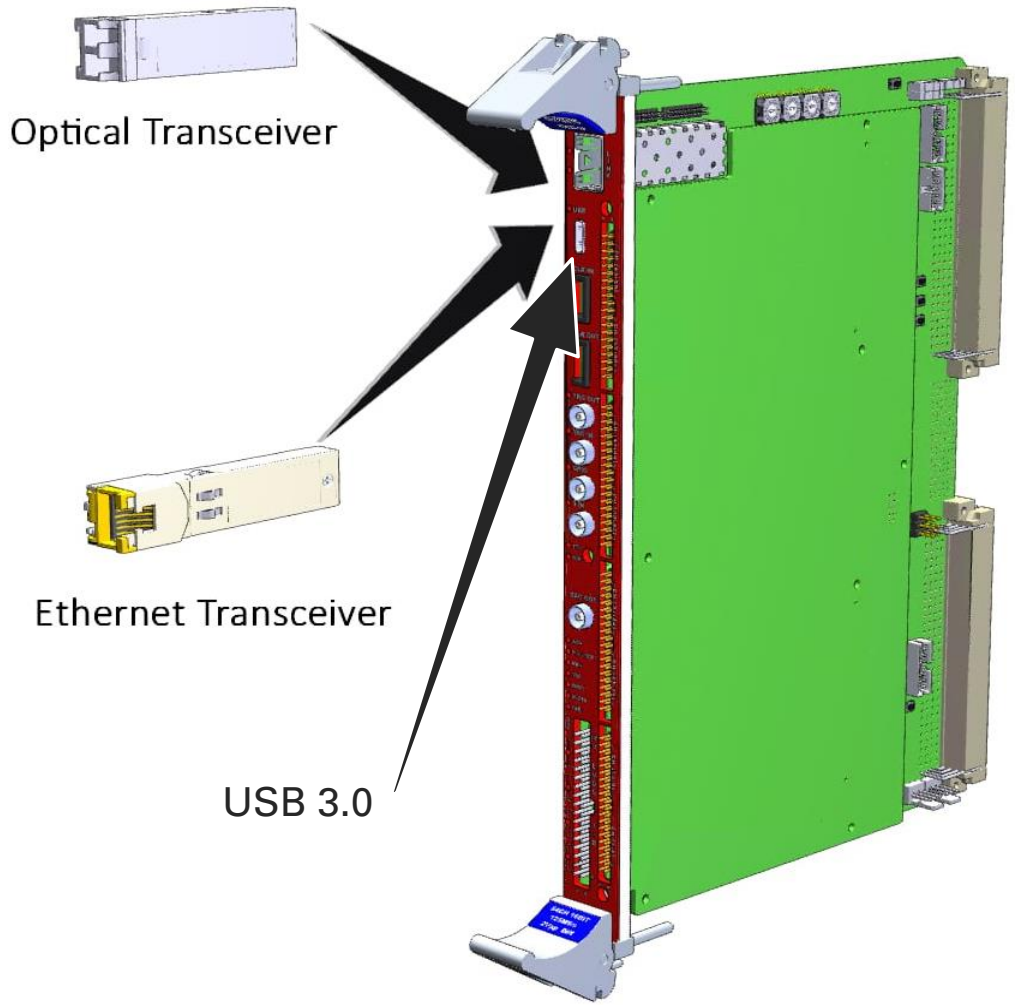
The Digitizer architecture



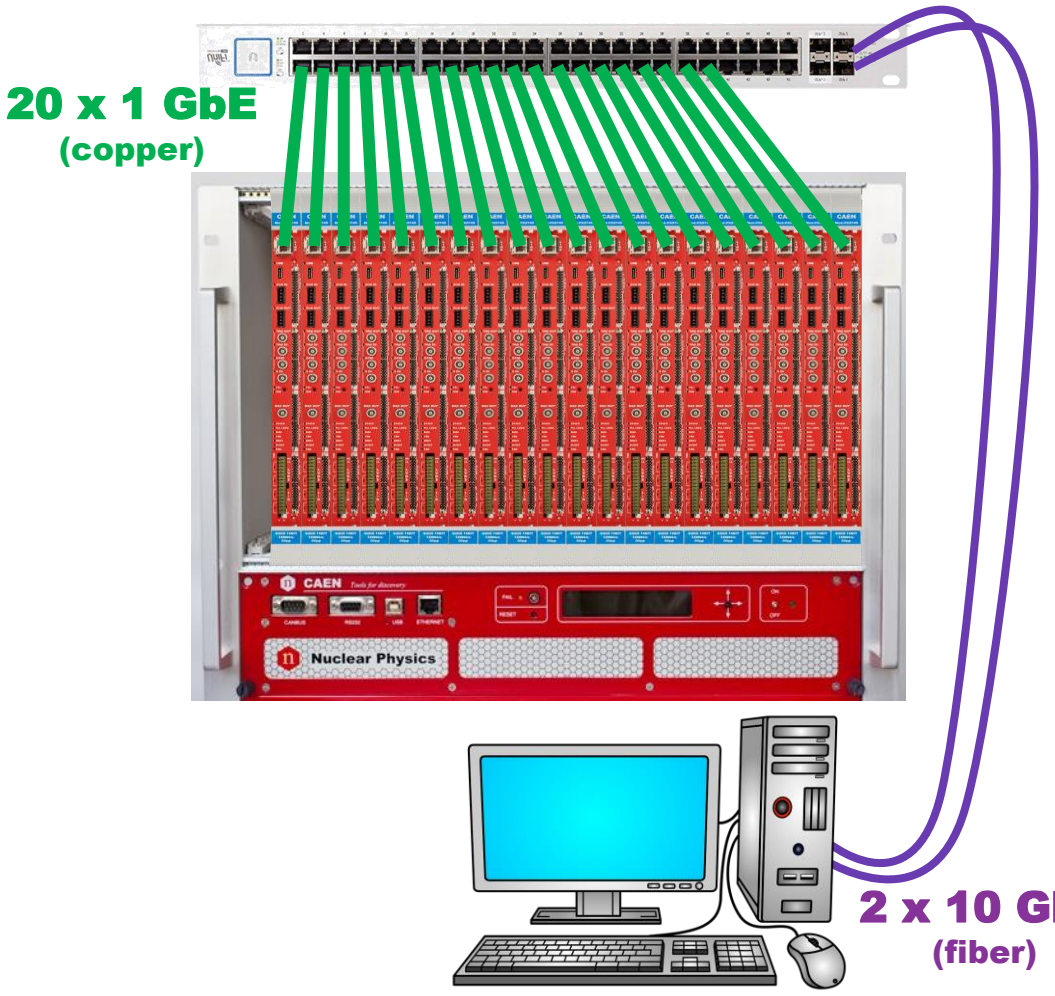
Readout interfaces

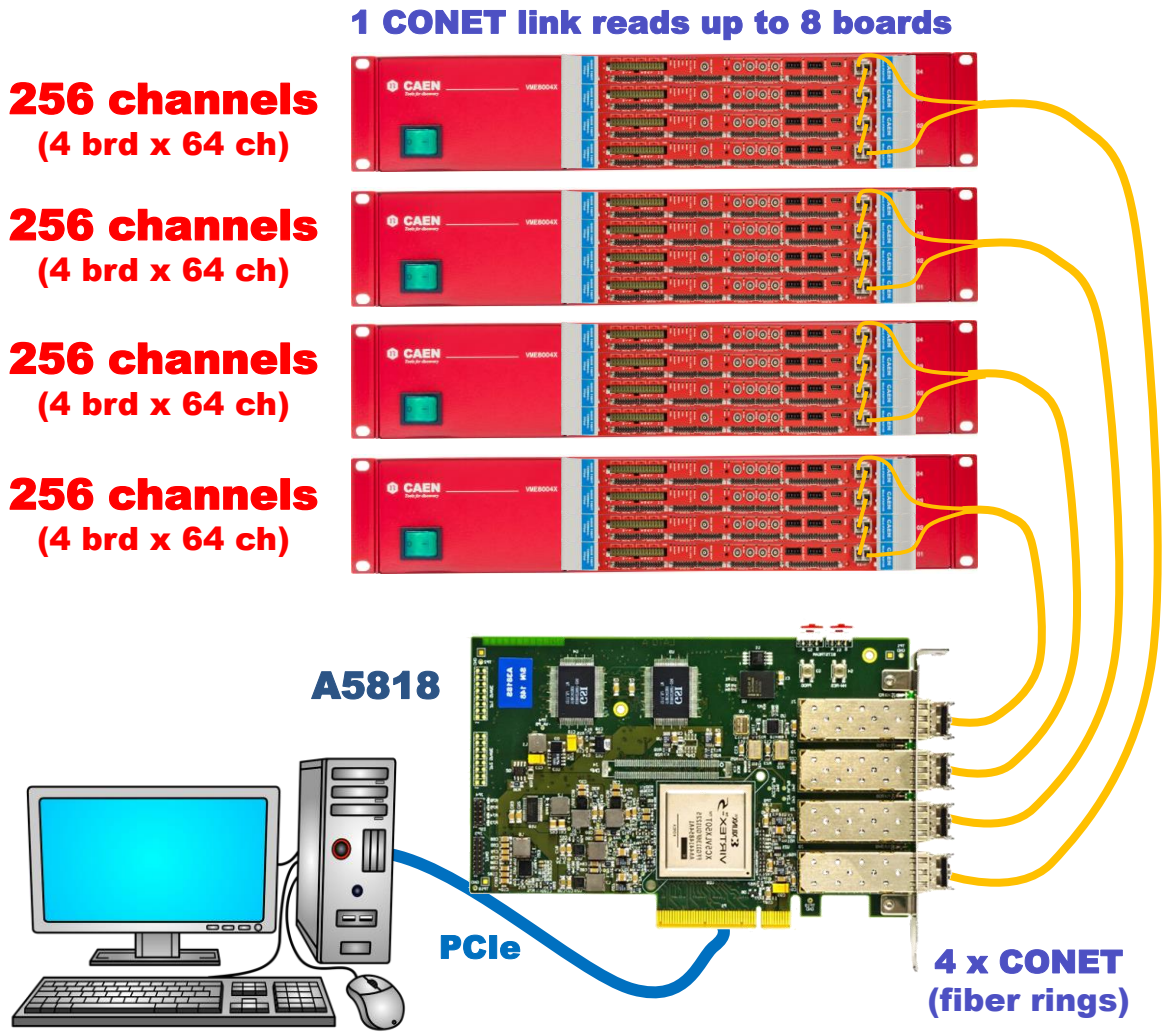
No Backplane Protocols

- 10 Gb Ethernet: Bandwidth = ~280 MB/s
- 1 Gb Ethernet: Bandwidth = ~100 MB/s
- USB 3.0: Bandwidth = ~280 MB/s
- PCIe: via optical links, daisy chainable.
  Aggregate Bandwidth = ~320 MB/s
- VME: legacy from the past… being dismissed (only used for power supply)



Multiboard Readout – Ethernet vs. CONET2





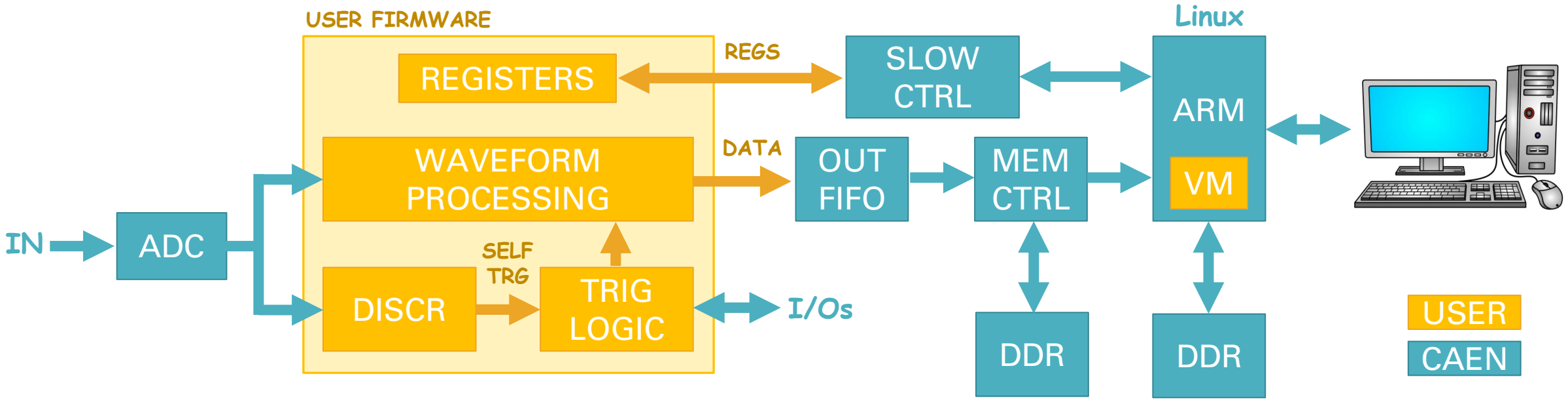
Open FPGA

We provide infrastructure: ADC data flow, data buffering and transfer, slow control

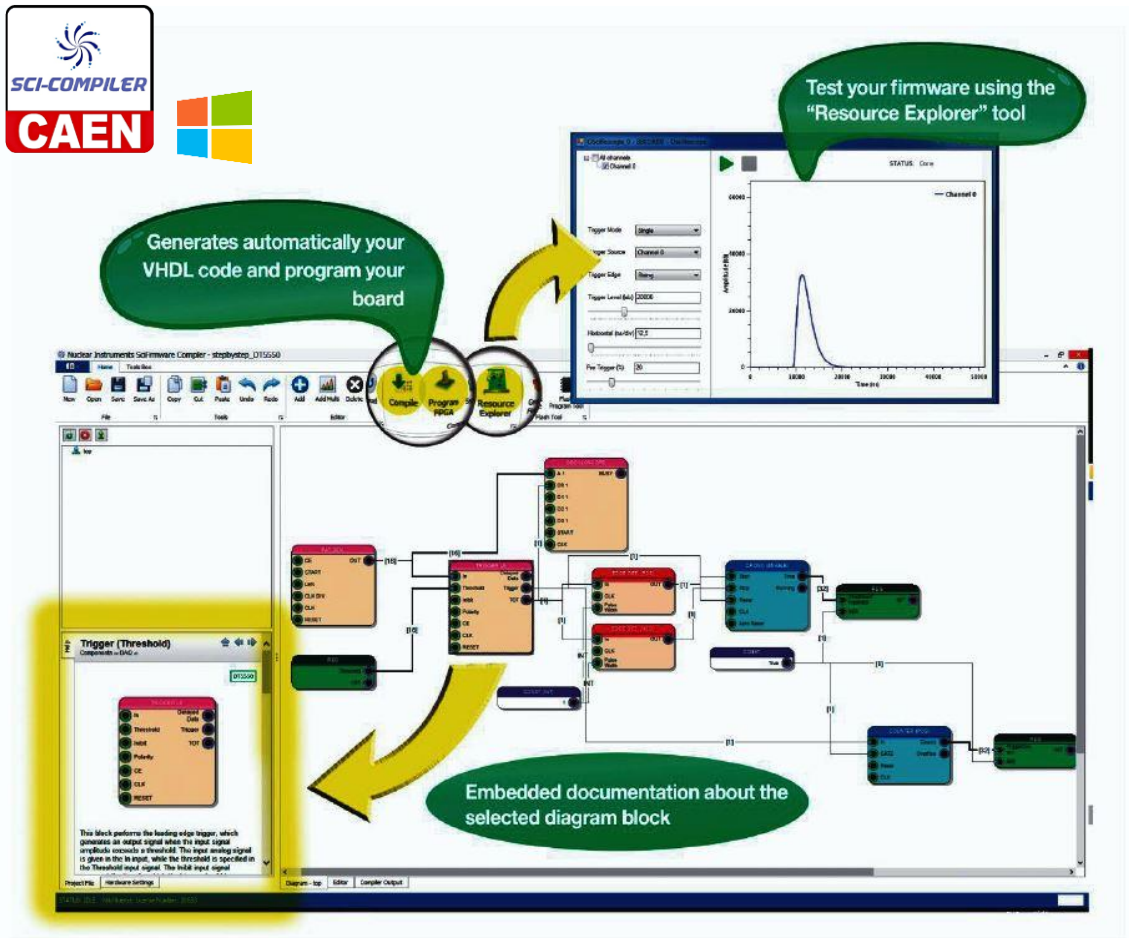
You implement your algorithms for data processing, parameter extraction and trigger logic

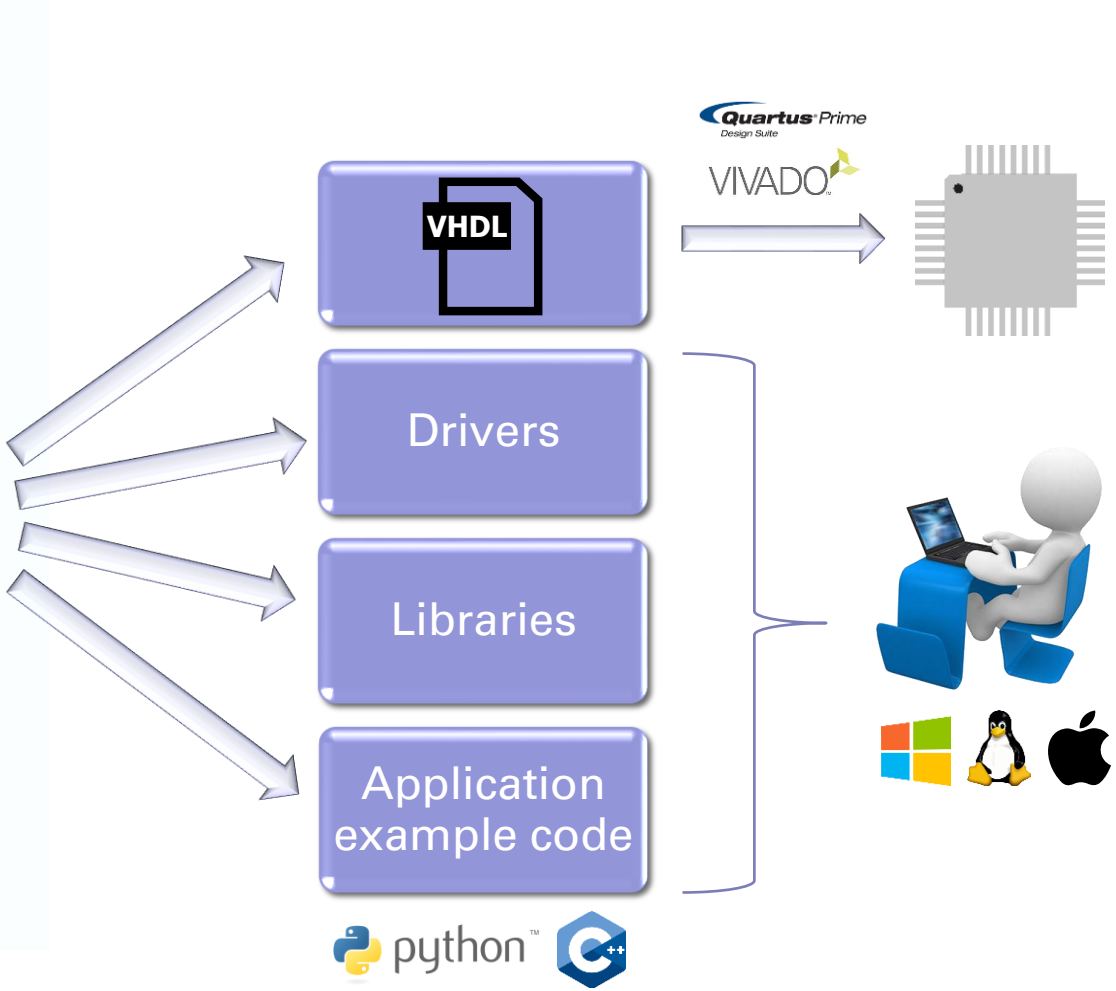
Sci-Compiler: graphical FPGA programming tool with precompiled modules (logic, filters, …)

FDK: FW development kit with VHDL templates, simulation models, signal inspection, etc.



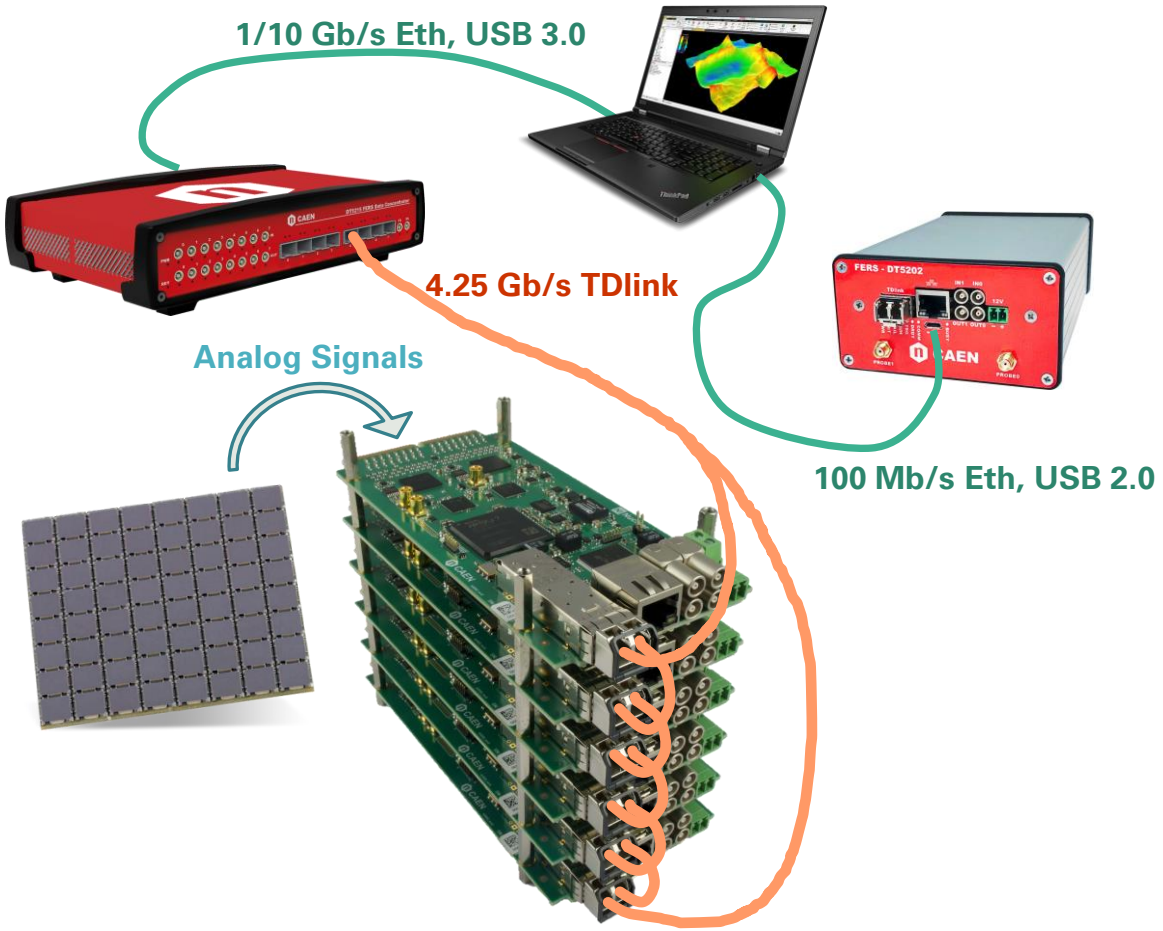
Open FPGA : alternative for transitional R&D





FERS-5200

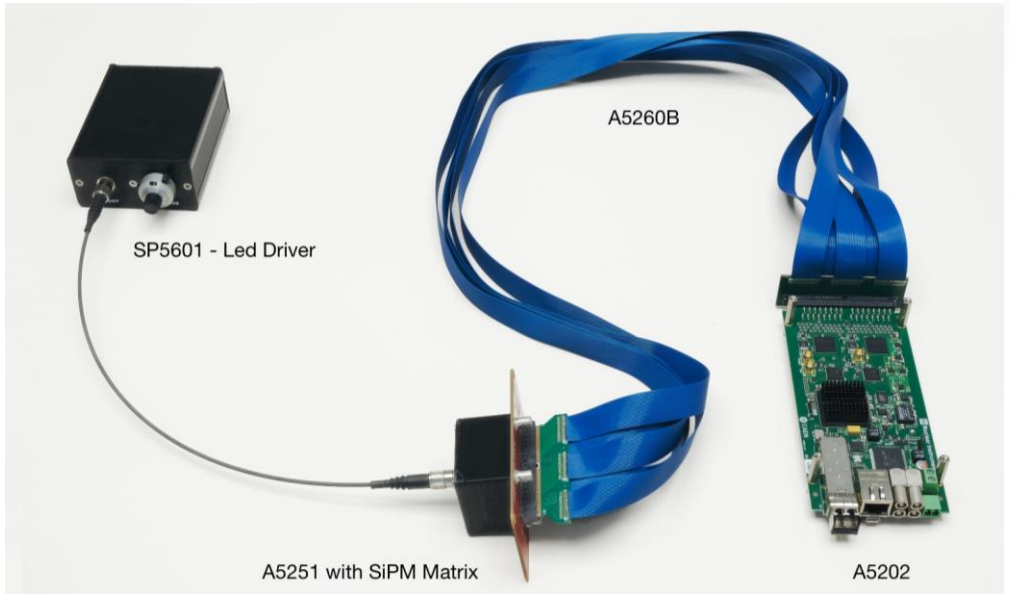
- **FERS:** Front End ASIC + A/D + Scalable Readout Infrastructure
- Easy **integration** of new ASICs => Compact solutions, tailored to the application
- **Scalability:** from single stand alone version for evaluation, to 10k/100k channels with same electronics
- **TDL:** daisy chainable optical link protocol with **data+sync**
- **Readout Tree:**
  1 FERS unit = 64/128 ch
  1 link = 16 FERS units
  1 Concentrator = 8 links = 128 FERS = 8k/16k channels
  Multiple Concentrators for unlimited readout…

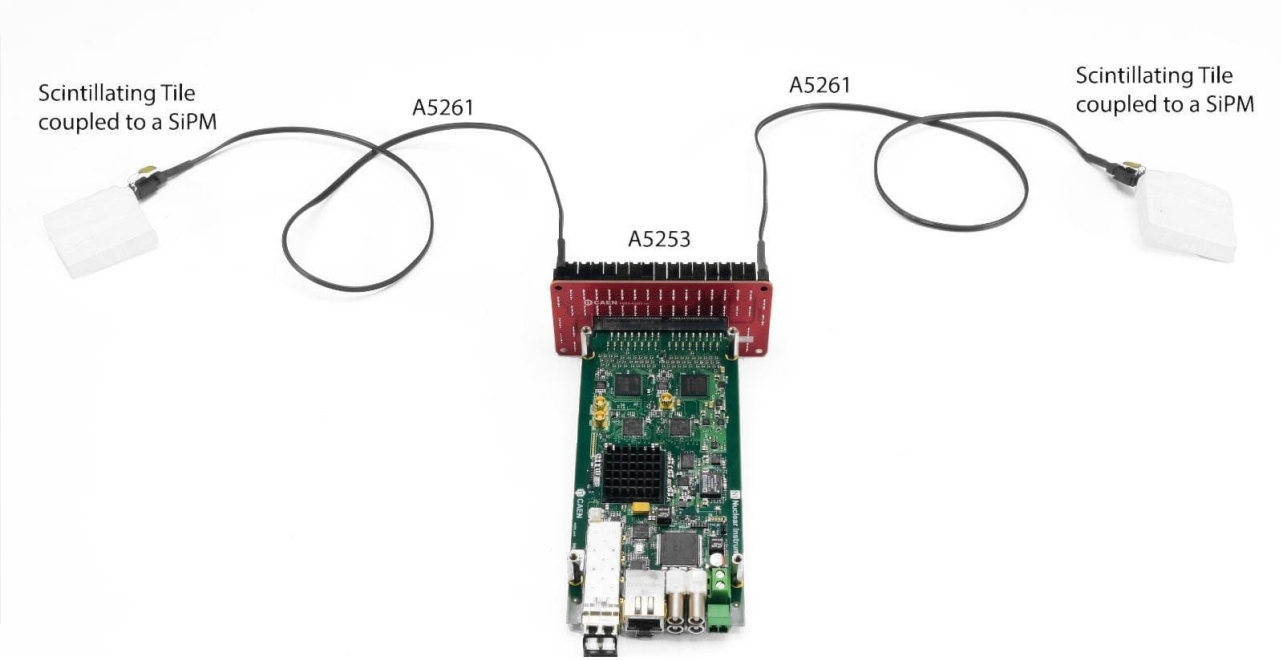


Connectors and Cables

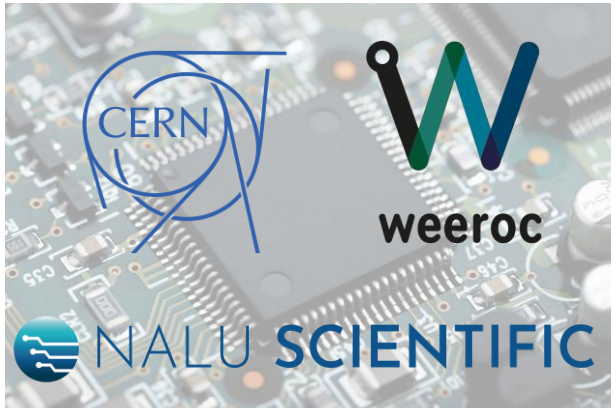
- **Micro-coaxial extension cable** for detector remoting
- Detached electronics simplifies the connection to **cold detectors**
- **Edge connector**: optimal fit for feed-through **flanges**
- Different types of interchangeable end connectors + custom made easily
- Easy fitting of **geometrical constraints**

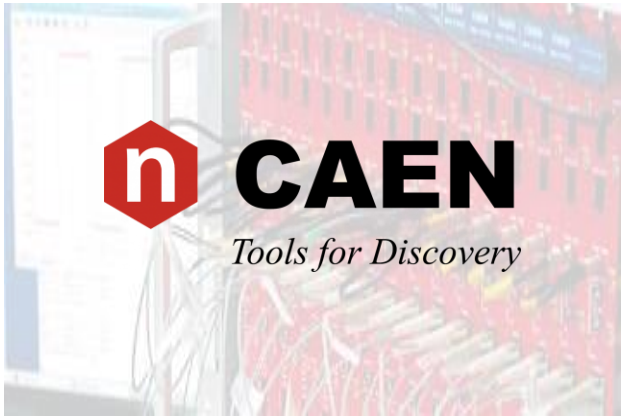
- 2.54 mm strip
- Hamamatsu footprint
- SensL footprint
- single SiPM footprint
- LEMO with discriminator





Synergies





Off-the-shelf front-end ASIC for scientific instrumentation.

Readout of **SiPMs**, **Si strips**, **GEMs**, PIN diodes, microMegas, MA-PMTs, ... for spectroscopy, PSD, timing applications.

Custom solutions for HEP experiments, with expertise in **rad-hard** design

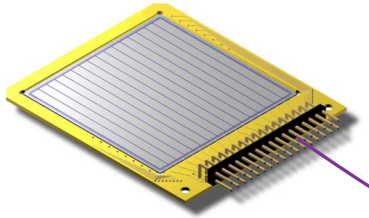
Design of high-end readout electronics and power supply for HEP and NP

We distribute Weeroc worldwide and Nalu Scientific in the U.S. for the scientific community.

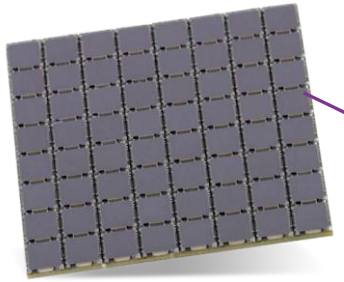
Integration expertise – **FERS-5200** and others

FERS-5200 flexibility

A **compact** and **flexible architecture** supports a wide range of potential applications:

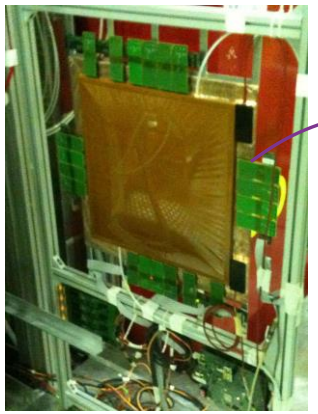


Silicon Strip Detectors



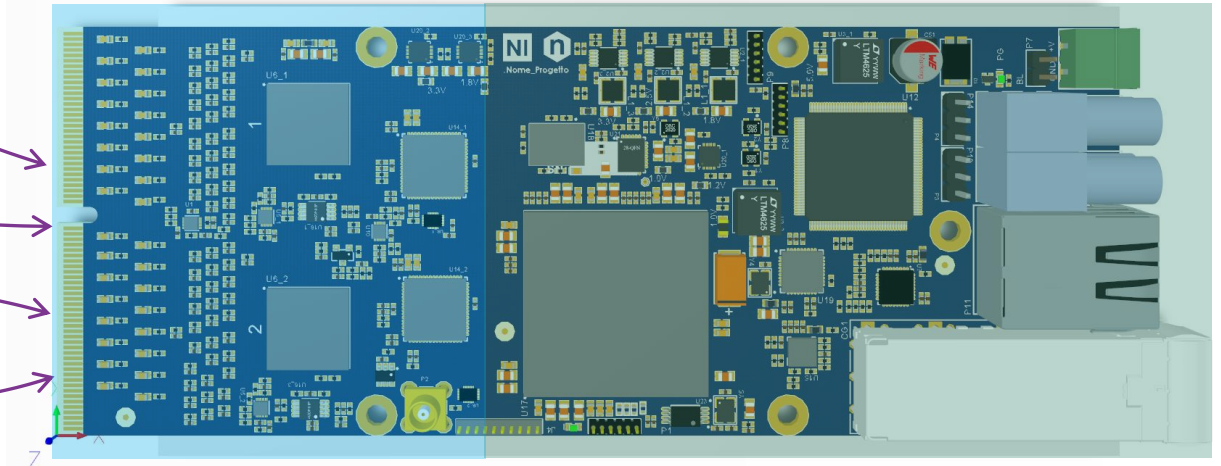
SiPM

Multi- wire chambers



Micromegas, GEMs

Same infrastructure, different Front-Ends by quick integration of different ASICs

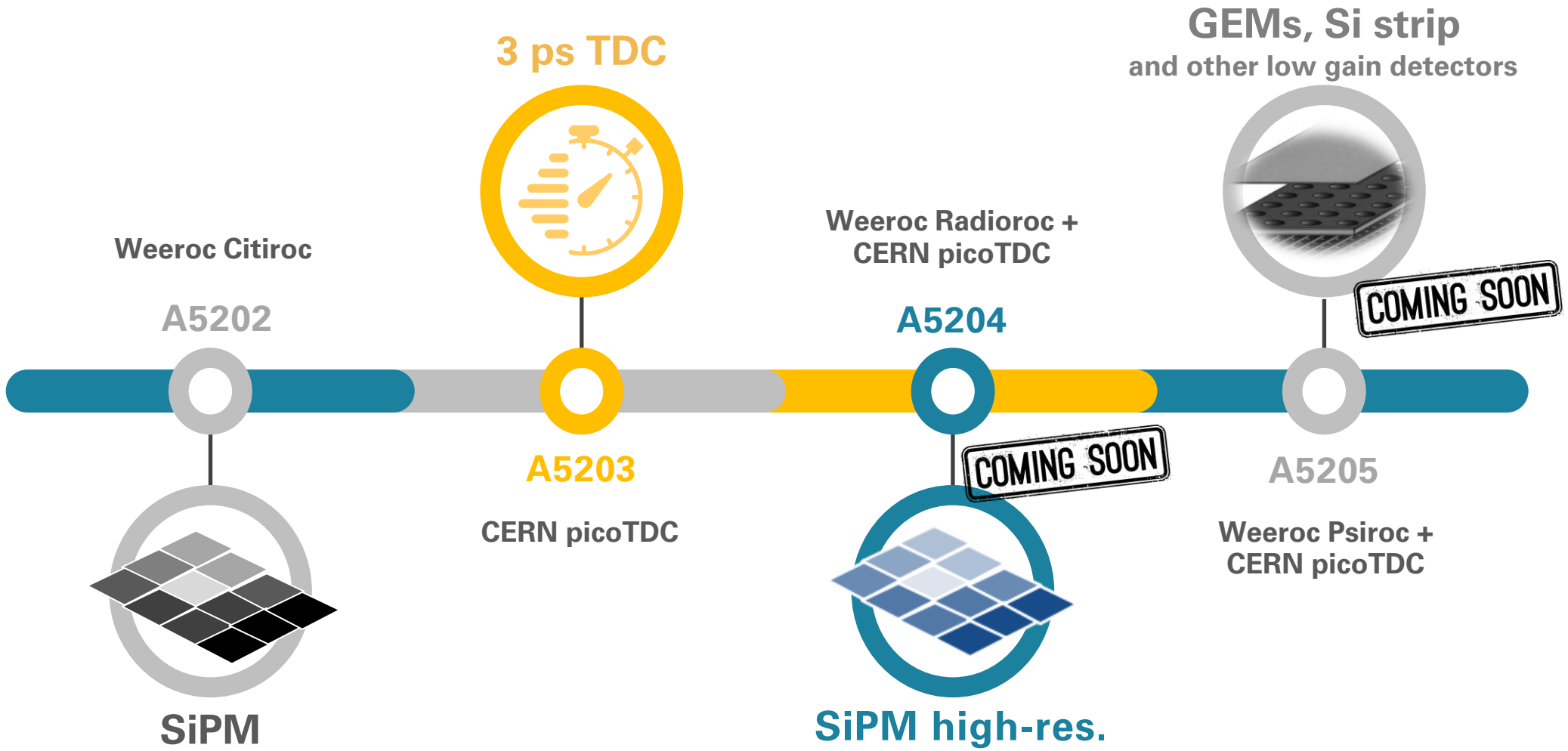


DETECTOR SPECIFIC **COMMON INFRASTRUCTURE**

- Weeroc CITIROC - SiPMs
- CERN picoTDC – ps timing
- Weeroc RADIOROC – SiPMs
- Weeroc PSIROC – SDD, GEM

In the pipeline

FERS Roadmap

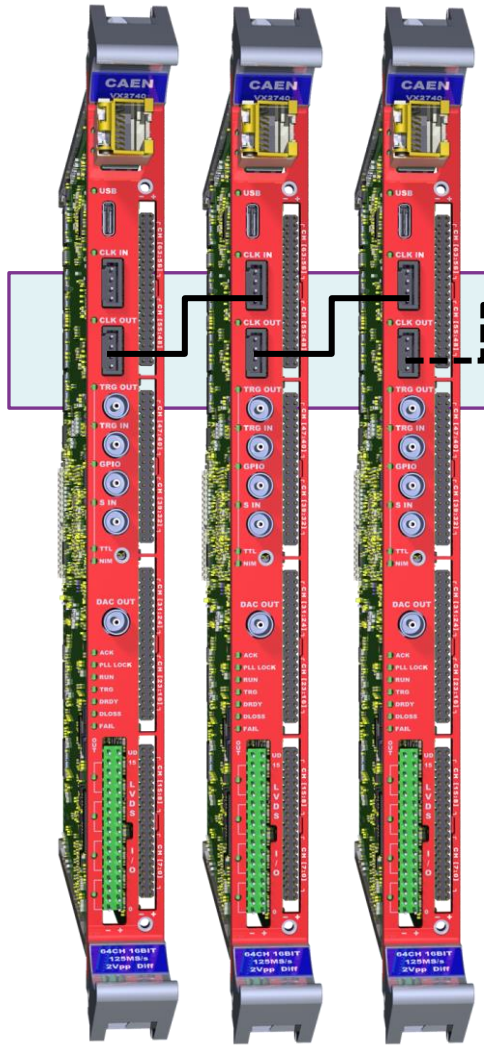


Thank you for your attention

Any question/curiosity?

Backup slides

Digitizers Synchronization



Synchronization of a CAEN Digitizer multiboard system

Clock and Sync distributed over a single cable –

Alternatively over the **VME backplane** user-defined pins

Synchronization with external systems

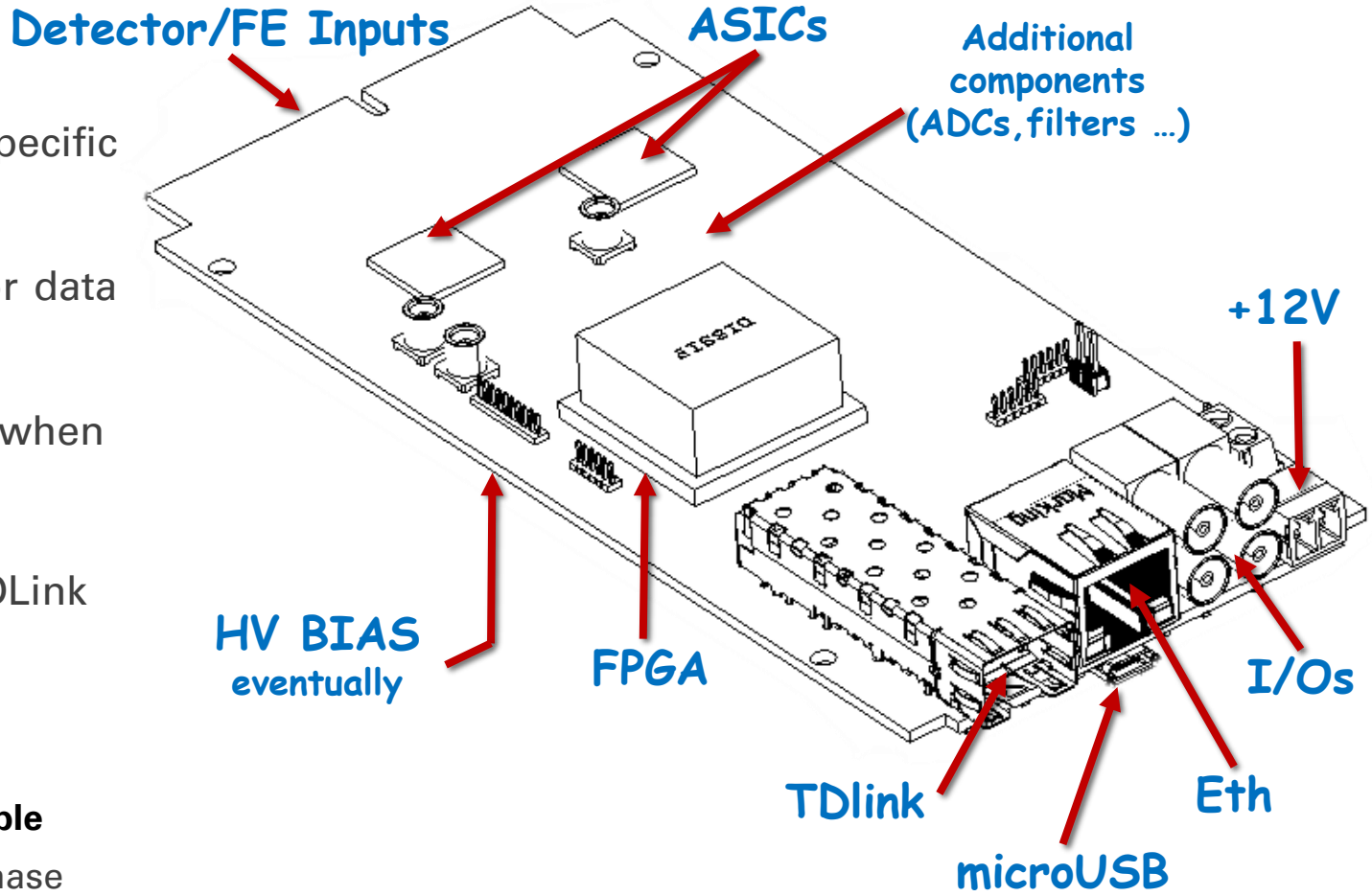
Additional LVDS I/Os for **trigger sharing, busy, veto** and **global timestamp**

FERS unit – how it is done

- Compact PCB - 17 x 8 cm
- Readout through **ASICs** tailored for specific applications
- FPGA implements the “processing center” for data coming from ASICs
- Embedded **High Voltage** for detector biasing, when requested by the application
- Different readout protocols: USB, Ethernet, TDLink

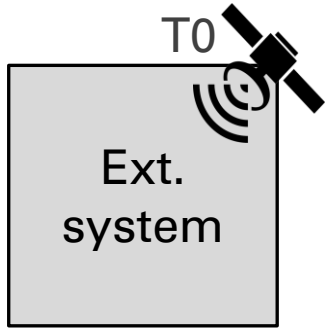
Desktop version available

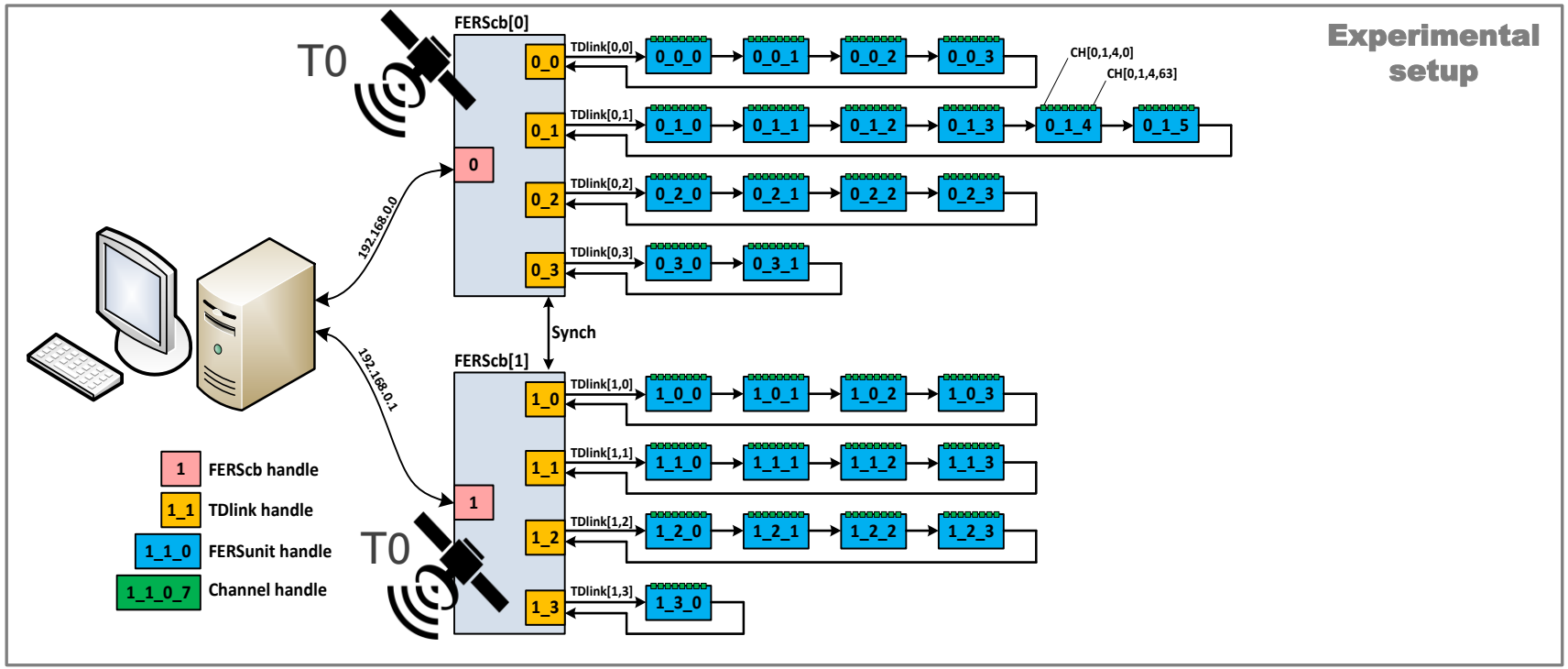
Ideal for prototyping phase



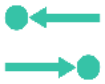
TD Link protocol

- **Proprietary protocol TDlink**: 4.25 Gb/s **over fiber** providing *Readout*, *Slow Control*, *Sync* and *Clock* at once
- Allows **alignment of the timestamps with external systems** too – for example GPS





SCI-Compiler: 100+ virtual blocks for physics



I/O INTERFACE

Control Digital and Analog Input/Output of the hardware devices

LOGIC GATE

Coincidence logic, boolean functions, Gate and Delay, counters, timers, scaler, frequency meters, array of bit manipulation

OSCILLOSCOPE

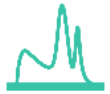
Probe signals of each acquiring channel, even in the middle of the processing chain.

IMAGING

Online image processing capabilities.

TRAPEZOIDAL FILTER

Trapezoidal filter allows to achieve the optimum resolution on HpGE and PMT detectors



ONLINE SPECTRUM

Energy/Time Spectrum can be calculated onboard.

TDC AND TIMESTAMPING

Timestamp events with 0.5 ns resolution and calculate ToT. Digital CFD increase 10x the timing resolution on analog signals

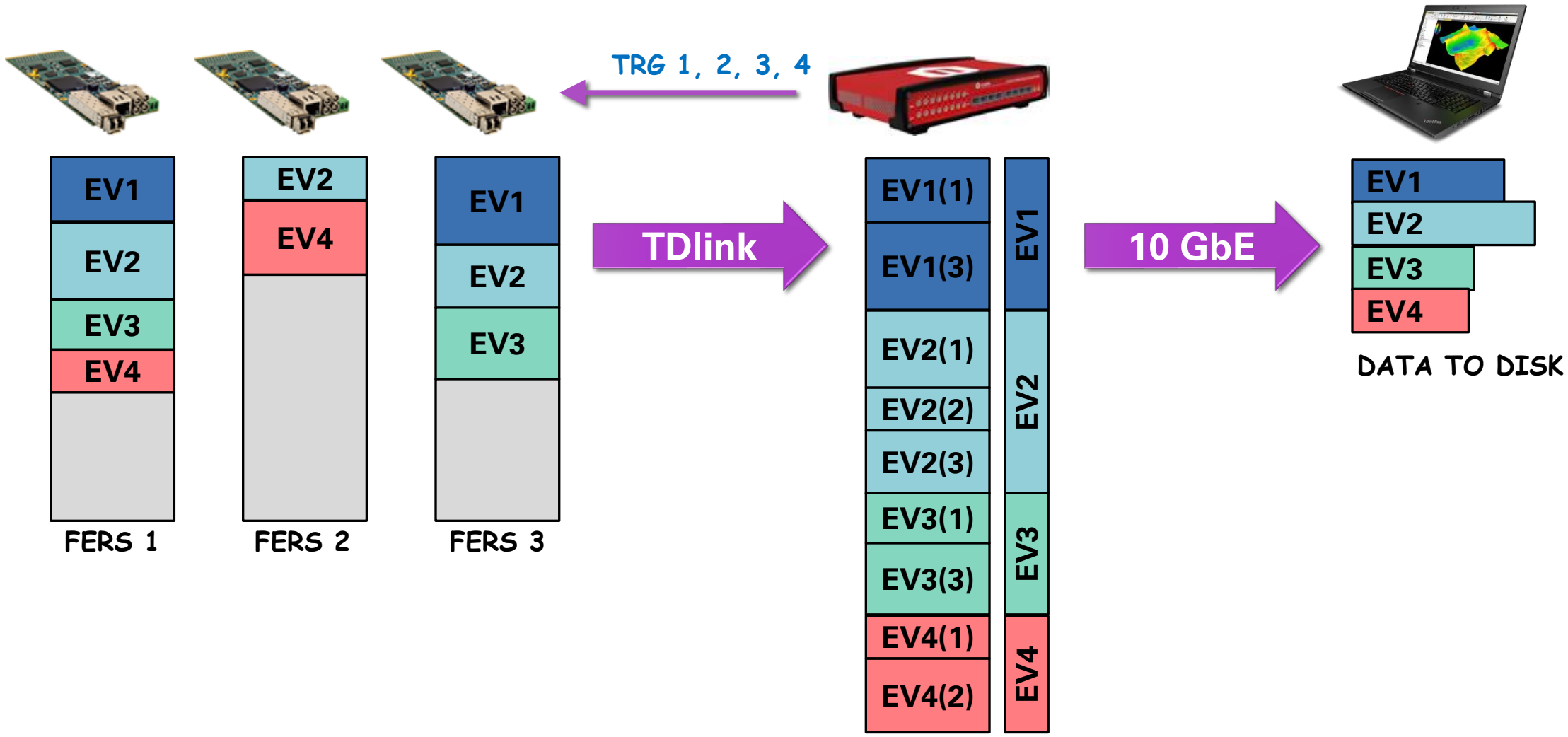
PSD

Pulse Shape Discrimination algorithm to allows for particle identification.

ANALOG SHAPER

High pass and Low pass real-time filter can be combined to emulate a traditional analog shaping chain.

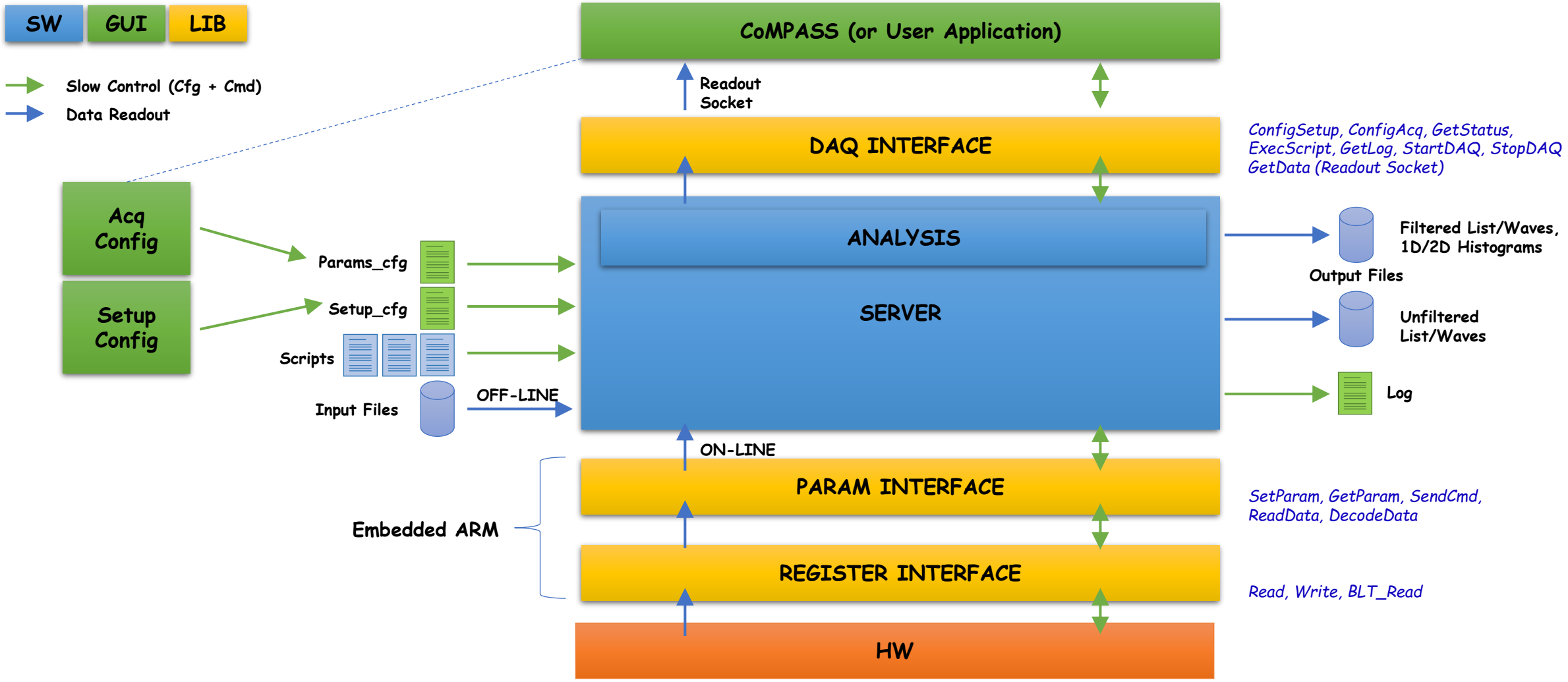
In-built sparse event readout



A5202: readout modes

- **Common Trigger Mode**
  - **FERS units**: generate a trigger request (typically OR of channel discriminators)
  - **Data Concentrators**: receive and combine requests from all units and generate the **Global Trigger**
  - **Event Building** and data reduction takes place in the ARM processor of the Data Concentrator
- **Trigger-less Mode (independent channel acquisition)**
  - **FERS units**: each channel pushes data asynchronously, typically at different rates
  - No trigger and data correlation in HW. Events reconstruction in DAQ.
- ARM processor running **Linux** and local DDR memory available in Data Concentrator
- High throughput data transfer to host computers via 10 GbE or USB 3.0
- Users can run custom routines for data handling in the embedded ARM

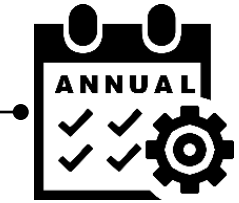
Software



SCI-Compiler: more than a software

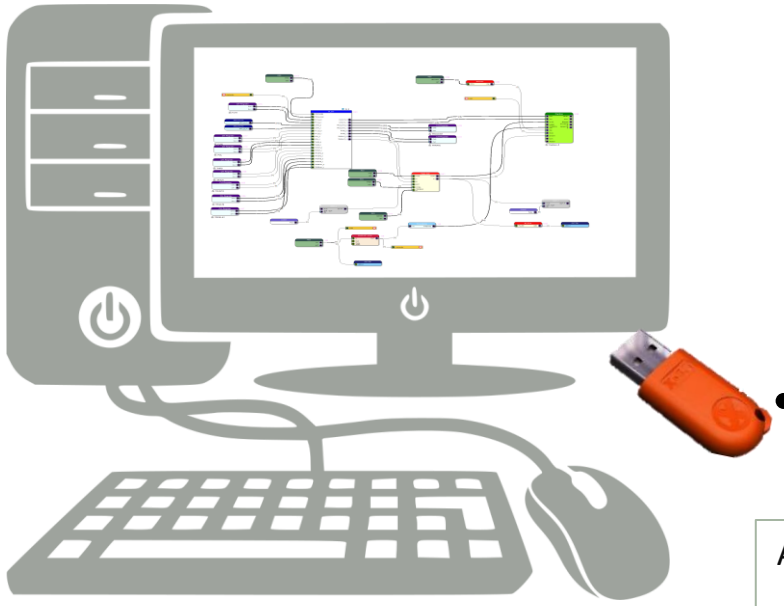
Remote customization service allows to generate the firmware code exploiting the computing power on CAEN server, with **no need of any local FPGA compiler**

Stay **up-to-date** with the newest SCI-Compiler features by subscribing the **yearly upgrade service**



Remote Customization Service

Using a single SCI-Compiler license, it is possible to compile and deploy firmware for **multiple compatible boards** that have been activated through a **runtime license***. A different runtime license is needed for each board.



A **single SCI-Compiler license** can run on a PC relying on a dedicated USB Dongle

*Firmware generated by SCI-Compiler runs for 30-minutes only if no runtime license is installed onboard

Digitizer options

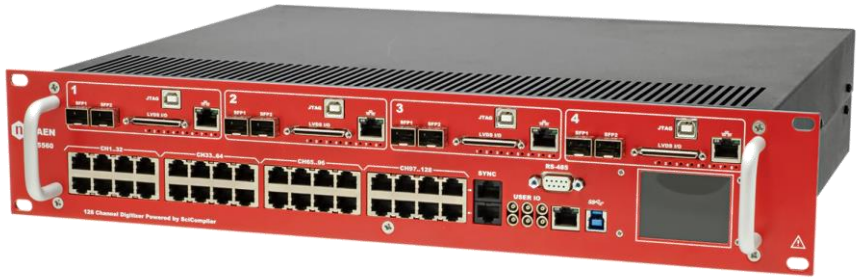
MS/s / #ch	62.5	100/125	250	500	1000	up to 5000
<8		DT	DT		DT	
8		V	V / DT	DT	V	DT(1)
16			V	V		V(1) / DT(1)
32	DT		coming…	coming…		V(1)
64	V	V / DT / R				
128		DT / R				

(1) SCA models => Max wave length = 1024 pts, Trg dead time = ~100 µs

V = VME

DT = Desktop

R = Rackable



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Acquisition Modes

	62.5	100/125	250	500	1000	> 1000	Description
Scope	●	●	●	●	●	●	Oscilloscope mode, all channels triggered simultaneously
PHA	●	●	●	●	●	●	Spectroscopy with Charge Preamps and PMTs
PSD	●	●	●	●	●	●	Neutron/Gamma/Alpha discriminations with Scintillators
TDC	●	●	●	●	●	●	Digital CFD or LED, Resolution < 1 ns (<100 ps with 500/1000 MS/s)
QDC	●	●	●	●	●	●	Self-gated charge integrator
ZLE/DAW	●	●	●	●	●	●	Waveform fragments (zero suppression, adaptive acquisition window)
Open FPGA	●	●	●	●	●	●	User defined Algorithms and Output Data Content

● Ready ● Coming soon ● Not Available