Electronics Development for High Energy Physics

RENAFAE Workshop 2022

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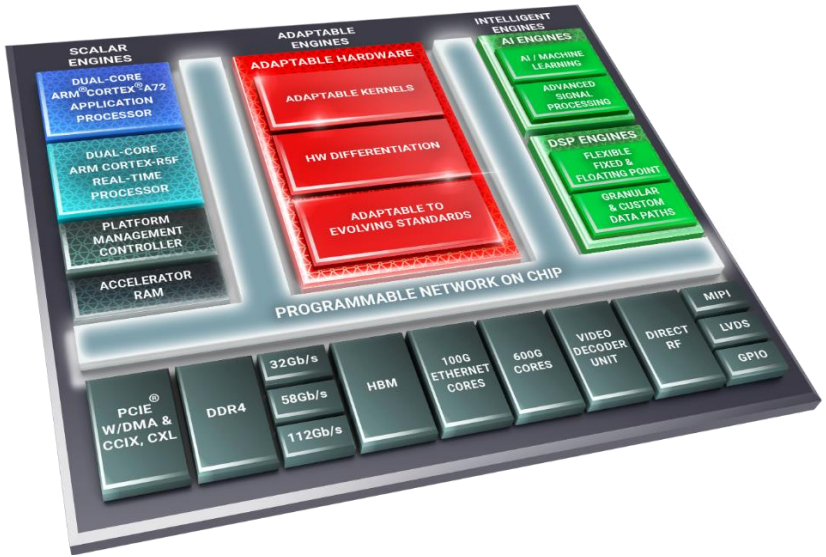
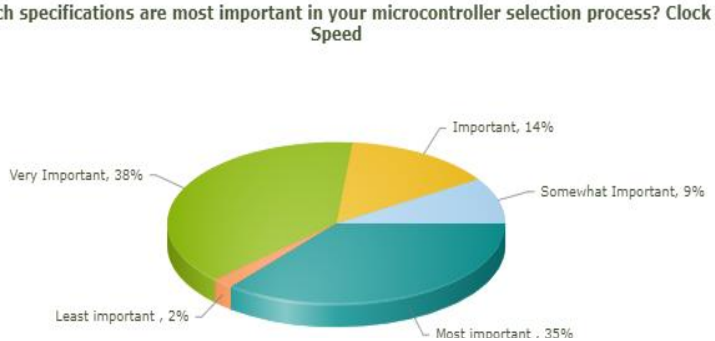
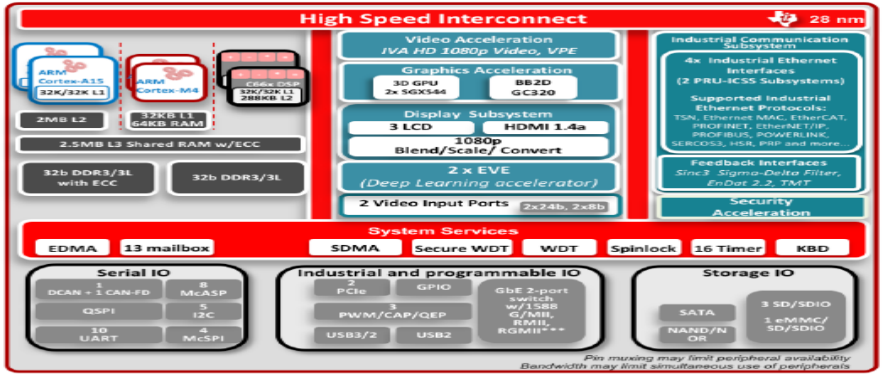
FPGA Dilemma: DLA

- **FPGA**: 35-year-old, one of the most impressive semiconductor devices ever created.
  - the more data you need to analyze, the better FPGA fits
  - To effectively support FPGA prototype platforms, FPGAs should trade off DSPs, SoCs and other embedded blocks for LUT area.
  - To serve the Deep Learning Acceleration market, FPGAs should trade off generic logic area for specialized silicon area.
  - DLA: favors higher growth in ASICs and GPUs, moderate growth for FPGAs and contraction for CPUs
  - Ages: Invention, Expansion, Accumulation, No Longer Programmable Logic/Artificial Intelligence. Like re-programmable ASICs?
  - Split into two branches? Xilinx new generation FPGA: ACAP - Adaptive Computer Acceleration Platform - Versal Family.



Larger Designs and Embedded AI





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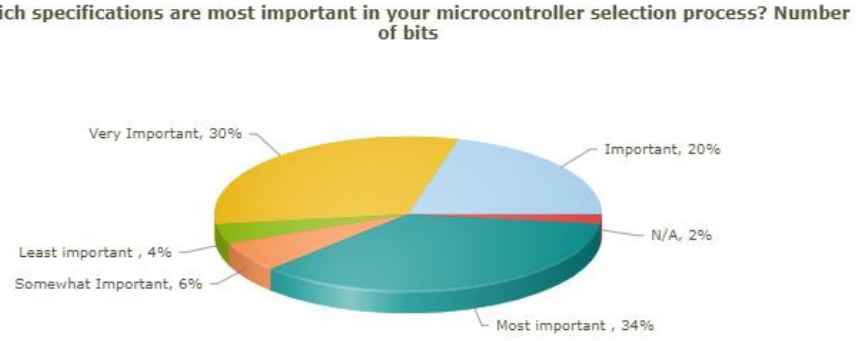
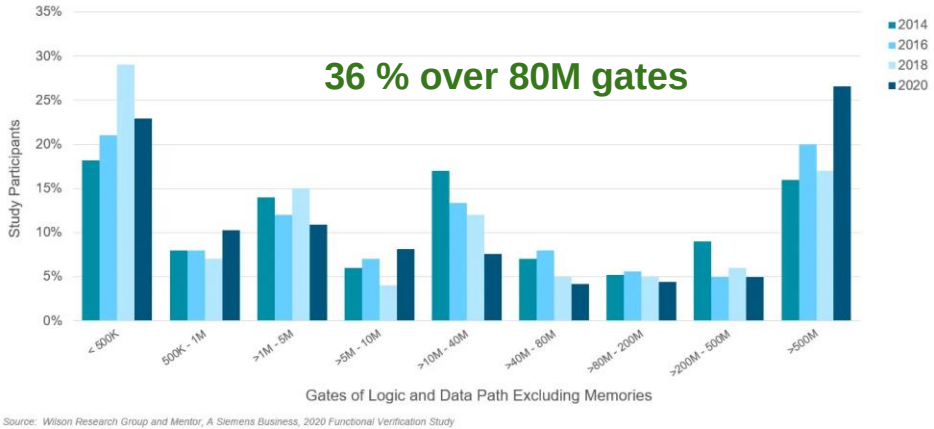




ASICS

(Marco Bregant, USP)

ASIC: Application Specific Integrated Circuit

Highly integrated electronic circuit, designed for a SPECIFIC “task”

In the HEP the most frequent case is the on-detector electronics that amplifies and digitizes the signals produced by a sensor; nevertheless there are as well plenty of examples of ASICs for signal processing/filtering or for data transmission (data link)

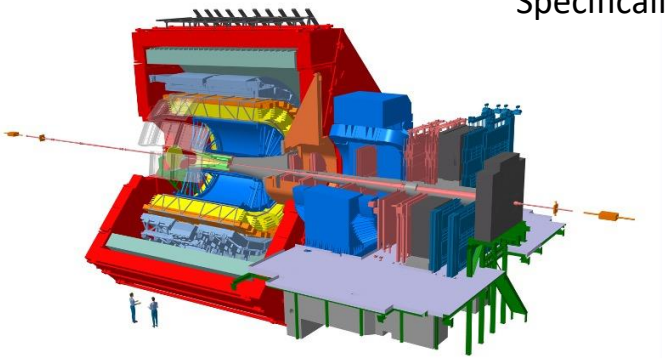
PRO:

- The only way to instrument high density, fine segmented, detectors (historically silicon trackers were the first using this approach for the front-end electronics) [btw, recent monolithic detector are just sensors with embedded ASIC…]
- Allows the highest efficiency in term of area and power
- Cost effective if the quantity of dies/chips is high (>several tens of thousands of chips)

CONS:

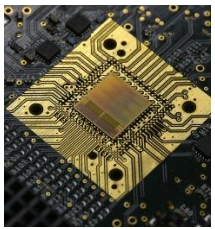
- Cannot be “re-programmed” after the fabrication, just configured choosing among the possibilities foreseen during the design.
- Long turn-around between fabrication of successive versions.
- Prototyping and production quite expensive (tens of kUSD for a small size, few samples, prototype (MPW runs), then for the mass production >>100kUSD just the masks for the wafer fabrication)

A recent* case of ASIC designed in Brazil: SAMPA



Specifically designed, in TSMC 130 nm technology, to attend ALICE TPC and MCH needs.

TPC Mode	MCH Mode
▪Negative Input charge ▪Sensor capacitance: 12 – 25 pF ▪Sensitivity: 20mV/fC & 30mV/fC ▪Noise: ENC ≤ 580 e^- @ 18.5pF ▪Peaking time: ~160 ns ▪Baseline return: <500 ns	▪Positive input charge ▪Sensor capacitance: 40–80 pF ▪Sensitivity: 4mV/fC ▪Noise: ENC ≤ 950 e- @ 40pF 1600 e- @80pF ▪Peaking time: ~300 ns ▪Baseline return: <550 ns



• 32 channels, Front-end + ADC + DSP, small footprint (dize size ~8x9 mm^2, BGA package size 15x15 mm^2)
• ADC: 10-bit resolution, 10MS/s, ENOB>9.2
(Alice TPC is eventually using: 5MS/s, to keep BW requirement in the readout chain lower)
• DSP functions: pedestal removal, baseline shift corrections, zero-suppression
SAMPA can be operated either in triggered or continuous readout (triggerless) mode.
Data transmission: up to 11 e-link at 320 Mbps to GBTx, SLVS I/O
Can sustain continuous readout, full data stream (no ZS), as far as ADC is operating at 10MSps or less.
• Power: for V4, in a typical DSP configuration, is usually 20mW/ch or less.

ALICE detector uses ~17,000 SAMPAs in the TPC, ~33000 in the MCH. Presently in data taking.

* Not at all the first! see, e.g., CARIOCA chip for LHCb

What was learned from SAMPA experience?

- We can do! It's tough, but all the competences are available locally (but we are in competition with private market for the most talented guys…)
- Modern front-end ASIC are "mixed", both analogue and digital specialist are needed to design the circuitry.
- Design the functional blocks, improve them, add special features is still a typical academic research task, it's R&D
- A complete ASIC is eventually a product! There are parts which implementation is just a "technical", often not so exciting, nevertheless requiring high skills, task that should be made with care and professionality.

A few engineers made most of the design job of the important functional blocks (FE, ADC, DSP), but a proper and detailed verification (via simulation and SW testbenches) kept busy more than ten people for several months.

- A front-end ASIC for HEP application may not have complete (and correct) specification at the beginning of the project. The detector is often developed in parallel, and proper and complete simulation of the condition of operation (spectra of the expected signals, burst of close signals and huge-signal probability) hard to be available since the beginning.

Collaboration and close information exchange with the people developing the detector should be pursued proactively.

How much "Specific" an ASIC needs to be?

Each detector category (TPC, Si-tracker, Gas-tracker, Timing, Calorimeters, …) has different needs in terms of:

1. Gain, noise floor, polarity, bandwidth, dynamic range, saturation and pile up signals, etc. for the analogue part
2. Digitalization rate and required number of bits
3. Filtering and data reduction (Zero suppression / hit construction / compression / etc.)
4. Number of channels/die, geometrical, power, and electrical limitation

Point 4 (and partially point 3) may be quite detector/experiment specific.

Point 1 and 2 are usually quite the same for the same category of detectors

With some coordination, an ASIC remains detector type specific, but may be not experiment specific

Also, if the technology (e.g. TSMC ## nm) is the same, functional blocks may be shared (as they are or with minimal adjustment) among different complete ASIC.

Even more important: the skills of the designer are NOT experiment specific, is there a way of profit of that?

Scenarios for the future

Several challenges:

- Microelectronics mainstream goes for smaller and smaller technology (already below “5 nm”)
- But that, beside being extremely expensive, is not a good technology for analogue design
- Likely the finest technology still adequate for analogue and mixed chips is 28 nm.
- Most of the present ASICs are designed in 65 nm technology: already quite expensive

Tight and strong collaboration among several institutes (in Brazil and abroad) will (already is) a must to reach the critical mass.

Already as Brazilian HEP community we should concentrate our effort.

What to chose?

- ASIC for projects/experiments (and detectors) were the “physicists” community have a direct interest appears as a wise choice.
- Nevertheless, as discussed yesterday at the round table, only HEP demand may not be continuous enough to keep active the engineers of microelectronic design.
- Presently the group @USP is collaborating with an european group in an evolution of the SAMPA

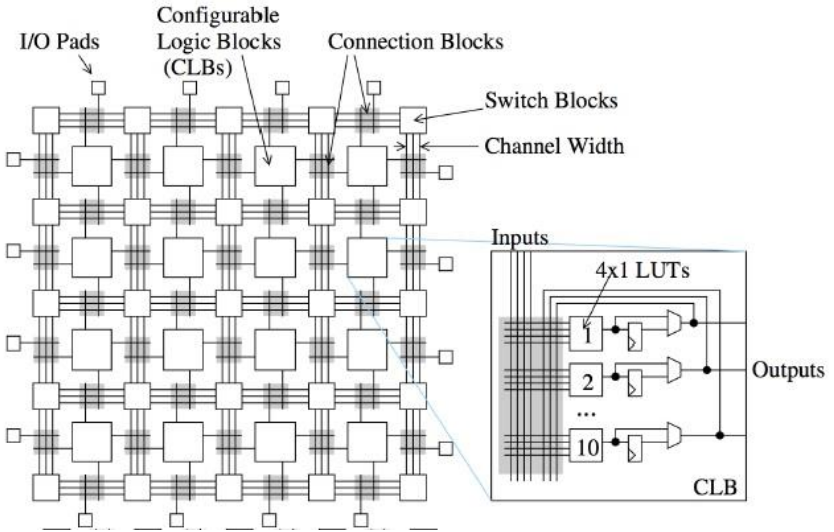
The electronic circuits that will read our detectors in 2030 (and beyond) are being defined and designed now.

FPGA

FPGA - Introduction

- Field Programmable Gate Arrays (FPGA) are digital circuits which can be programmable using hardware description languages (HDLs) to execute specific operations.

- FPGA technology can offer flexibility, speed, density and computational power to perform most tasks found in HEP, like:
  - data acquisition,
  - signal processing,
  - controls,
  - monitoring,
  - data transfer using high-speed links,
  - online trigger and
  - event reconstruction.

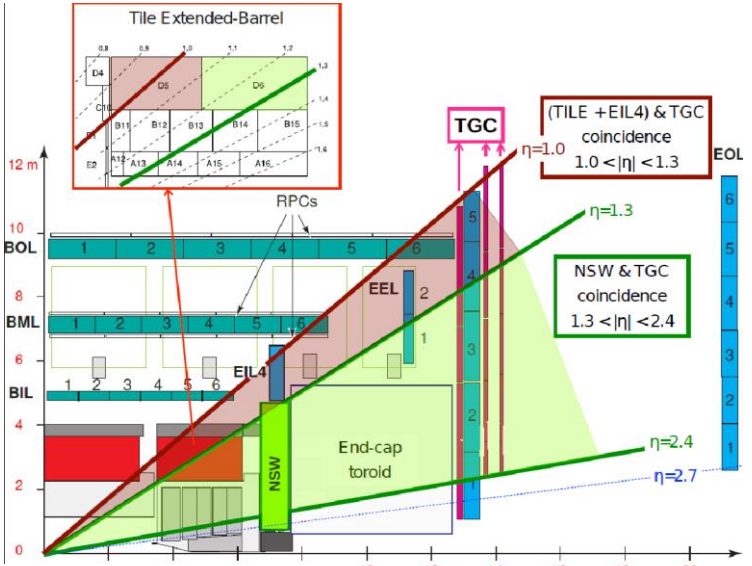


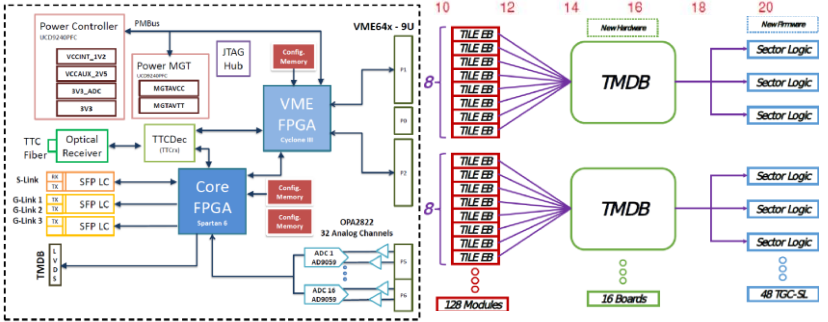
FPGA - Advantages of very deep-submicron FPGA

- State-of-the-art very deep-submicron FPGA technologies can offer to several technical and economic benefits
- Such advantages come from:
  - High volume
  - High yield low cost per wafer tab-lines in which these technologies are produced
  - Combined with the higher density
  - Intrinsic radiation tolerance
  - Low power inherent in deep-submicron CMOS

FPGA - ATLAS Level-1 Online Trigger (TMDB)

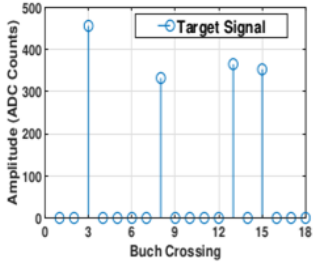
- A significant part of the muon trigger rate in the end-caps
  - Low energy particles (mainly protons) produce fake triggers by hitting the end-cap trigger chambers
  - For the region covered by 1.0<|η|<1.3, usage of the hadronic calorimetry (TileCal) D-layers in coincidence with the TGC inner station muon chambers can reduce the trigger rates
- New hardware and firmware to read-out analog cell output
  - TileMuon Digitizer Board (TMDB)
    - FPGA technology: fast
  - New firmware in TGC-Sector Logic
  - Design concept, development and testing: Brazilian
  - Production: Brazilian industry

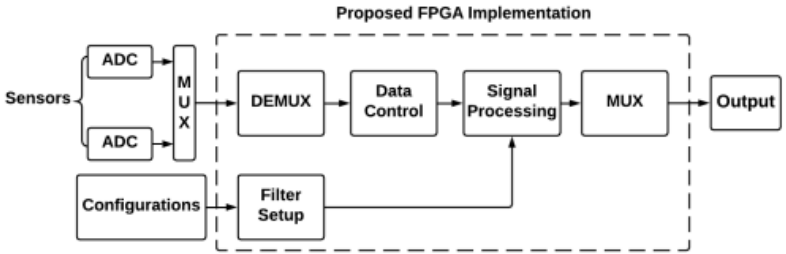


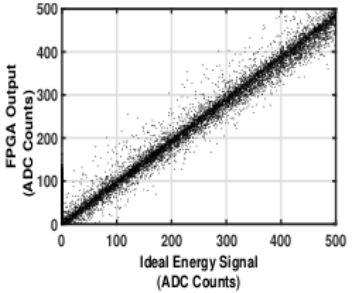


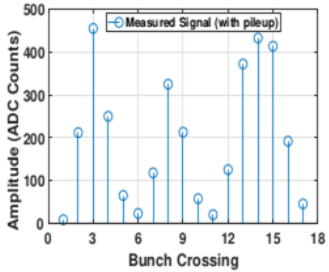
FPGA - Online Energy Estimation for Pileup Reduction

- If a given sensor receives a new input while it is still sensibilized by a previous event, the readout signal may be distorted. This problem is known as pileup.
- Pileup tends to increase in the operation of modern particle colliders.
- It is possible to reduce pileup influence by using an online signal processing solution embedded in FPGA.









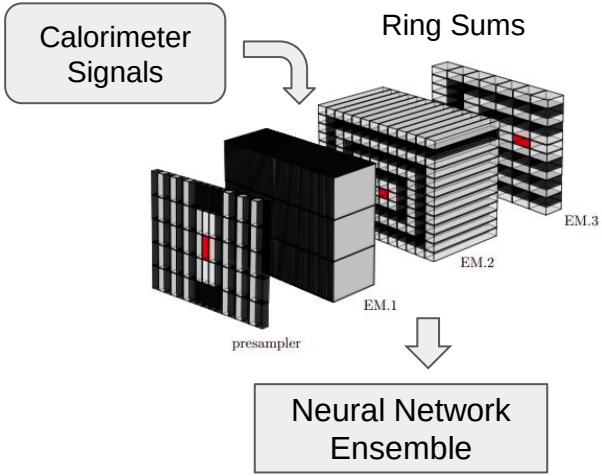
COMPARISON OF THE RESULTS OBTAINED WITH THE IMPLEMENTATION OF BOTH METHODS USING XILINX XC7VX485T.

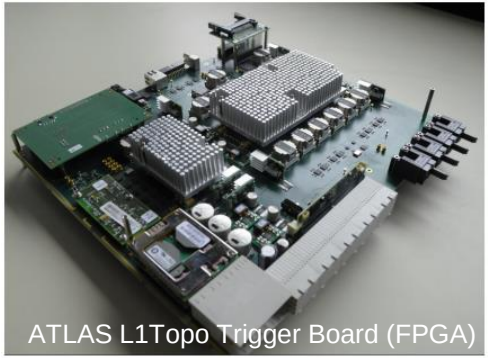
	FIR (20th order)	Iterative
RMSE (ADC Counts)	19.21	8.79
Minimum Clock period (ns)	1.879	1.896
Utilization of Logic elements (%)	1	5
Utilization of Registers (%)	0.245	4
Utilization of DSP Structure (%)	0.75	17
Total Power Consumption (mW)	423.66	550.85

RMSE: Root Mean Square Error measured in ADC Counts

FPGA - Level-1 Trigger based on Neural Networks

- The use of machine learning solutions for HEP has been experiencing a considerable increase, specially for particle identification and triggering.
- Online trigger systems require very short time latency for providing a decision and are often split into sequential selection levels.
- FPGAs are an interesting solution for the implementation of machine learning systems of L1 trigger systems in HEP.
- In ATLAS experiment, the High-Level trigger (HLT) based in calorimeters for electrons is based on an ensemble of feedforward neural networks.
- A future extension of this classifier is an equivalent implementation in FPGA to operate at L1 trigger.




ATLAS L1Topo Trigger Board (FPGA)

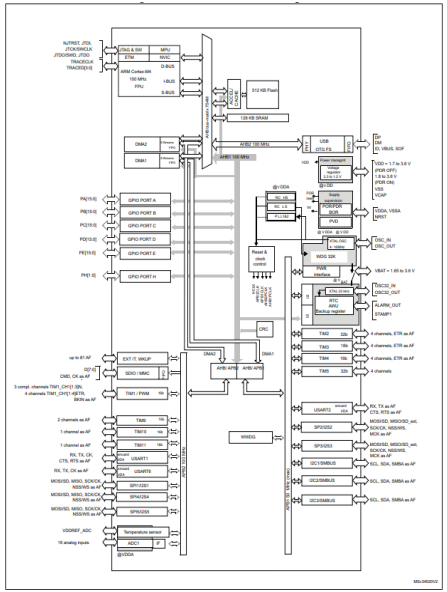
Microcontrollers and Embedded Systems

(Luigi Calligaris, SPRACE/UNESP)

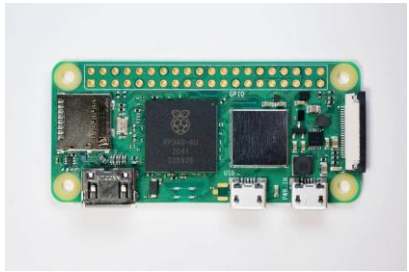
Microcontrollers and Systems on a Chip

- **MCUs**: most used piece of programmable electronics
  - Literally everywhere: appliances, cars, planes, toys, robots, …
  - Flexible solution to automate a device function
  - Compilers most commonly available in the very popular C language
  - **Cheap**, **low-power**, **reliable**, **low-level** control
- In many devices, MCUs manage low-level behavior
  - Sequencing of device power-up to ensure a safe boot
  - Closed-loop thermal management system monitoring and operation
  - Off-loading from a CPU real-time tasks, like reading out a sensor
- **SoCs**: usually more complex than a MCU
  - Supports large external RAM, i.e. can run standard Linux
  - Designed for **heavier loads**, less for low-level control
  - Can be the main “intelligent” device in a board
- SoCs usually run Linux or an RTOS
  - Standardized environment to run application software into
- ***Embedded systems***→MCU, SoC, FPGA, DSP,...

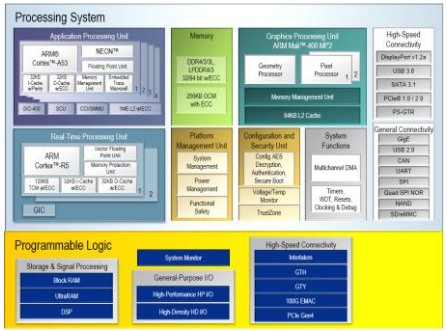
The Arduino Uno uses an ATMEGA328P MCU



Schematic of a STM32F411 MCU



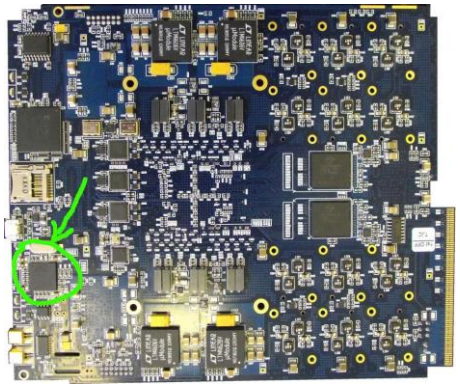
The Raspberry Pi Zero 2 uses a SoC



Schematic of a Zynq MPSoC EG

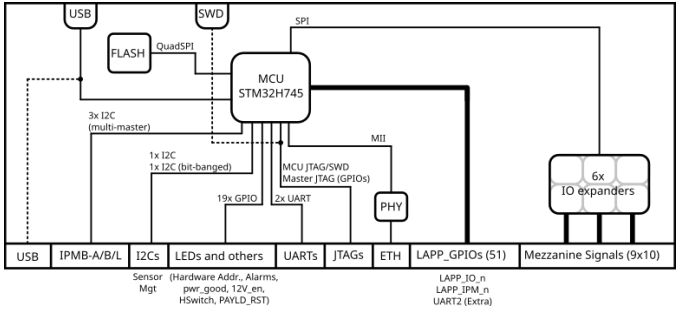
Embedded systems in HEP

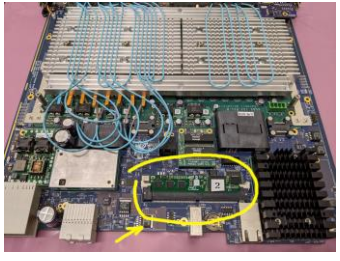
- Modern experiments heavily based on electronic components
  - Detector control & safety, sensor sampling & read-out, trigger, data decoding & processing
  - Electronics permit high-performance, consistent and reliable operation of the experiment
- Most electronic cards in detector back-ends use 1 or more MCUs & SoCs for their control
  - Knowledge of these systems is fundamental for the design of a board, important for development on it.
  - Boards shown in picture: Imperial MP7 (MicroTCA), Apollo (ATCA), Serenity (ATCA)



Example application: OpenIPMC project

- CMS Phase-2 Tracker back-end will use ATCA boards
  - These boards need to have an Intelligent Platform Media Controller
- OpenIPMC : software implementing an IPMController
  - Initially developed by SPRACE to run on Xilinx Zynq MPSoC
- OpenIPMC-HW : mezzanine suitable to run OpenIPMC
  - Designed around a powerful STM32H745 MCU
- OpenIPMC-FW : custom firmware for the mezzanine+ATCA
  - Ongoing effort to customize it to our target board applications
- This project develops local know-how on MCU/SoCs
  - 2 students and 2 senior so far
- We showed that OpenIPMC can be made locally
  - Can become a contribution of Brazilian science to CMS
- [See slides by André Cascadan (Sess. 1, 27/04 16:00)]





Technology Transfer

- Embedded systems find application in a vast group of high-tech products
  - **Medical**, **agricultural**, **security** & **safety**, **logistics**, **smart appliances**, **aerospace**, …
- Smarter devices → more embedded systems needed
  - Energy efficiency, green revolution, home gadgets, new transportation, …
- R&D on embedded systems in HEP→ advances in science and industry
  - Gives an edge to Brazilian science in this fundamental hardware sector
    - Contribution to experiments in High Energy Physics experiments
    - Contribution to experiments in related research topics (e.g. X-ray science)
  - Fosters local know-how in embedded system design
    - Designs used in HEP experiments have been transferred to industry (e.g. medical imaging)
  - Excellent training opportunity for students → tomorrow's industry developers

<u>example industrial application</u>

OLED screen

oxy sensor

firmware

MCU

<u>pulse oxymeter</u>
an inexpensive medical embedded system

Challenges on Embedded Systems in Brazilian HEP

- Problems in availability and import of electronic components from aboard
  - Needed for the assembly of custom-designed embedded systems.
  - Import process can delay significantly the order of components, meanwhile stocks can run out.
  - This has been a long-standing issue. The chip shortage made it worse.
- Relatively small number of national companies suitable for prototyping runs
  - Small number of boards to be produced and components to be sourced
  - Requirements for PCB manufacturing for HEP applications different than common boards
- Early training on the development of embedded systems
  - Not easy to find researchers with any level experience in embedded system design
  - *__But__* cheap Arduino, ESP32, STM32, Raspberry kits made entry-level training popular at home & uni
- Overall, these issues can be overcome, but they slow down development
  - Delays can lead to project cancellation, so these issues need to be addressed

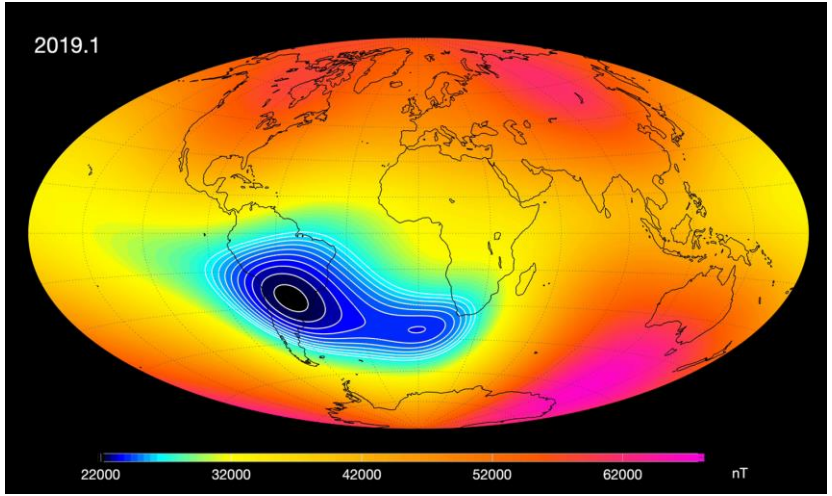
RADIATION HARD ELECTRONICS
(Marco Leite - USP)

RADIATION HARD ELECTRONICS

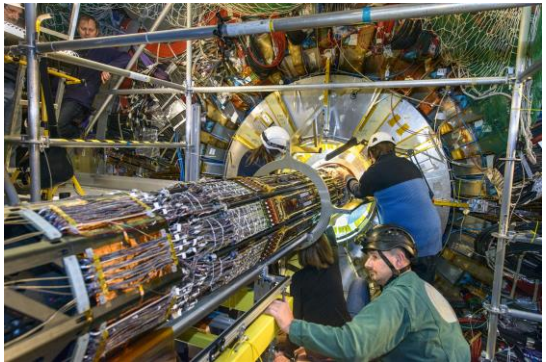
Some Key points

- Crucial for accelerator experiments (even low energy, non-colliders etc.)
- Specially critical for HL-LHC
- Also important in aerospace applications (see the SAM anomaly right above us…)
- Faster electronics →smaller structures →more sensitive to radiation effects
- Most commercial (active) devices will either die or malfunction in this environment
- Protected fabrication technology (defense)
- Protected testing information
- Needs a multi-disciplinary team (HEP, NP, SSP, EE…)

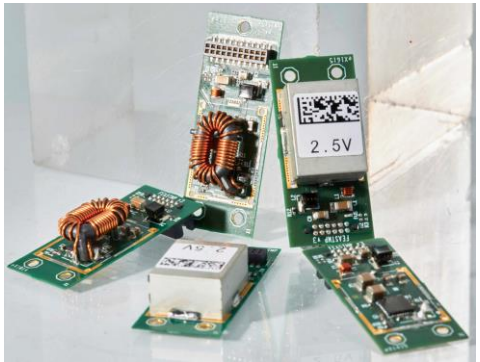
South Atlantic Magnetic Anomaly (ESA)



ATLAS Inner Tracker



CERN Rad Hard Voltage Regulators



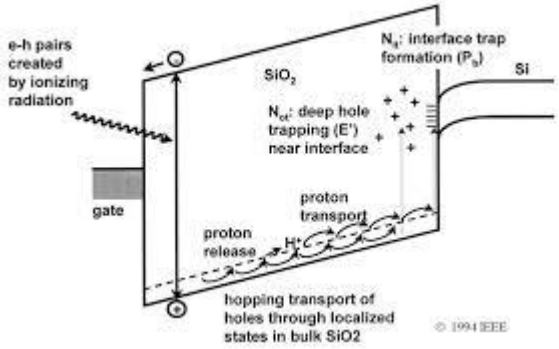
RADIATION EFFECTS IN ELECTRONICS

Mechanisms of energy loss

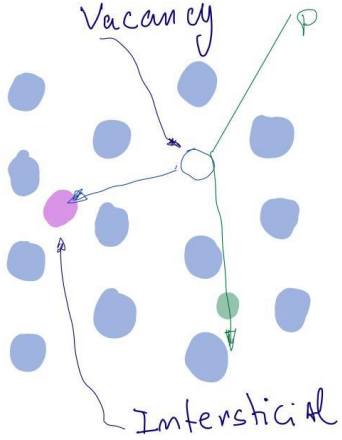
- Charge generation (ionization)
- Nuclear reaction (hadrons)
- Non-ionizing energy loss - NIEL (structural)

- **Dose Effects (cumulative)**
  - Total Ionization Dose (TID)
    - Enhanced Low Dose Rate Sensitivity
  - Displacement Damage (DD)

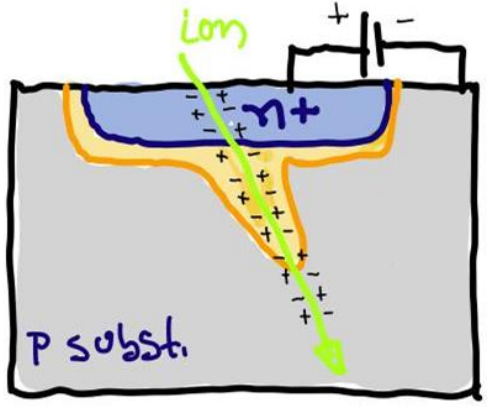
TID



DD



- **Single Event Effects (hadrons)**
  - Destructive
    - Single Event Latchup
    - Single Event Gate Rupture
    - Single Event Burnout
  - Non-destructive
    - Single-bit upset
    - Multiple bit upset
    - Multi-functional interrupt



SIMULATION OF RADIATION EFFECTS IN ELECTRONICS

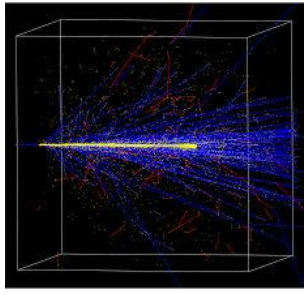
Physics

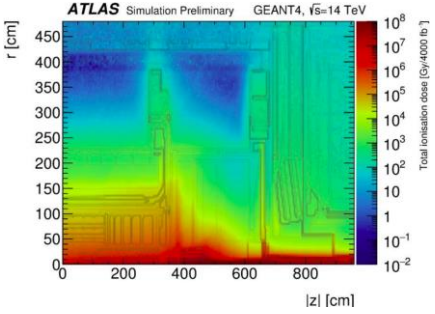
Engineering

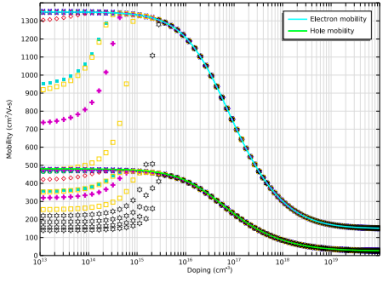
- Radiation interaction with matter
  - GEANT4
  - FLUKA
  - SRIM
  - …

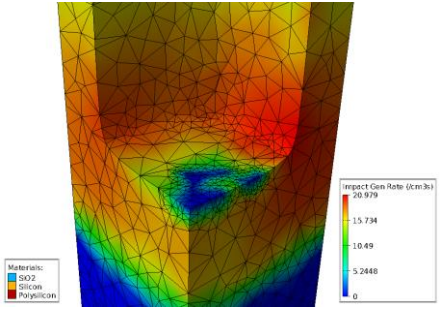
- Effects in device structure (**E**)
  - TCAD
  - COMSOL
  - Custom Code

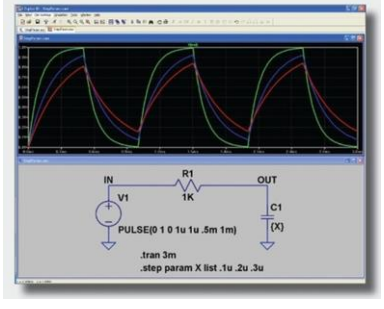
- Electrical/functional Simulation
  - SPICE
  - HDL Simulators
  - …

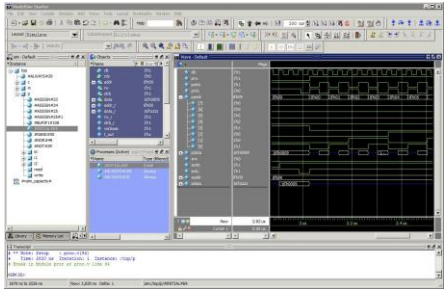








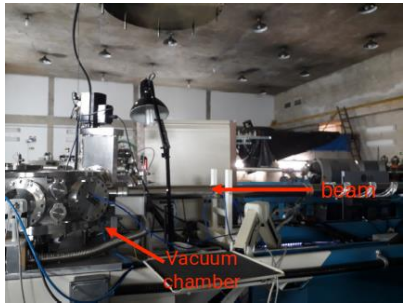


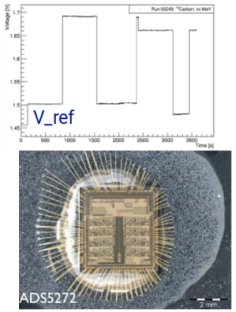


Testing

MIL-STD-883 TM 1019
ESA ESCC Basic Specification No. 22900
ASTM F 1892

USP Pelletron accelerator: p (14 MeV) to Ag (110MeV)
Device can be tested while irradiated
Ex. COTS ADC tested for ATLAS



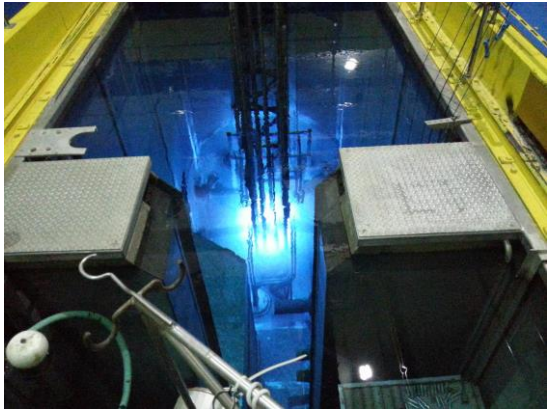


FEI x-Rays generator
Device can be tested while irradiated

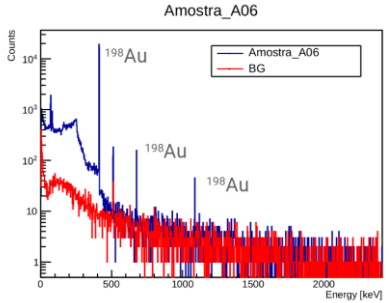
IeAV ^{60}Co source ~36 Gy/h collimated
Device can be tested while irradiated

Pulsed high power lasers

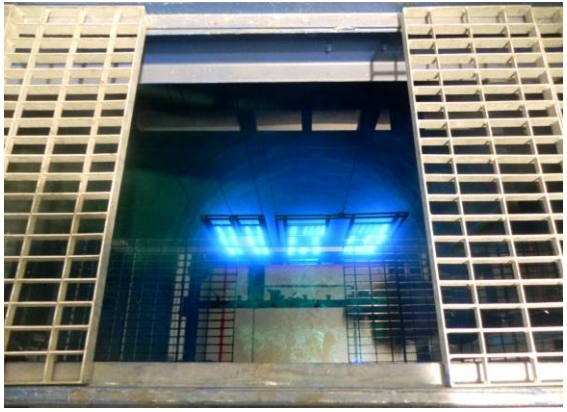
IPEN 5 MW research reactor
~10^{12} n_{eq}/cm^2s (up to 10^{13} near core)



Some LGAD Sensors already irradiated @IPEN
γ spec. used to estimate dose and activation



IPEN 1 MCu industrial ^{60}Co irradiator



Mitigation strategies

- Choose fabrication process proved to be radiation hard
- Choose the level of functionality (less is better)
- Provide redundancy, monitoring, calibration, testing, checksum
- Implement one or many level(s) of mitigation strategy(ies)
- Needs to take into account very large doses, accumulated over long periods of time (sensors and electronics, so indirect effects as well…)

- Device level

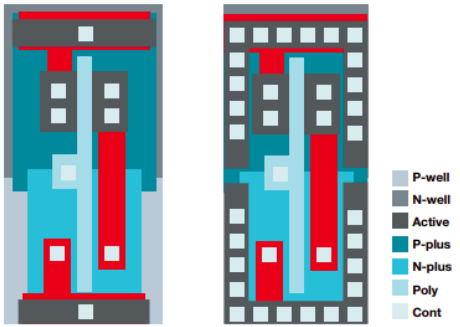
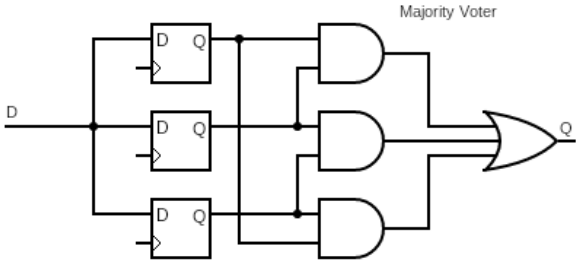
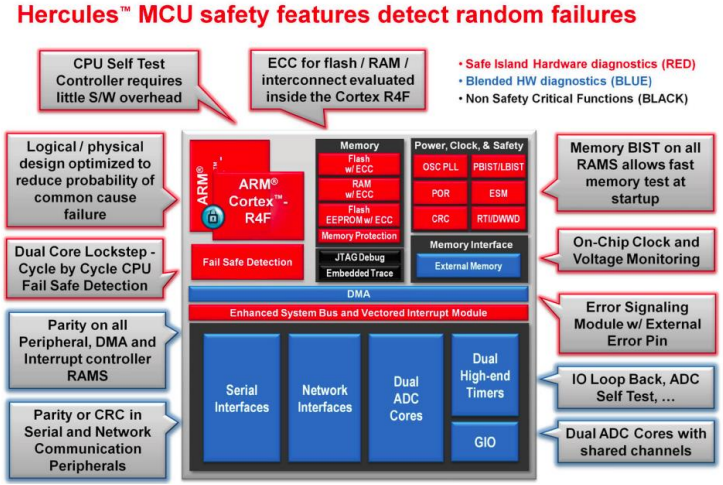


Figure 6-7. Conventional inverter layout (left) and inverter with guard rings (right). The area penalty is ~1.28x.[15]

- Circuit level



- System level



SUMMARY

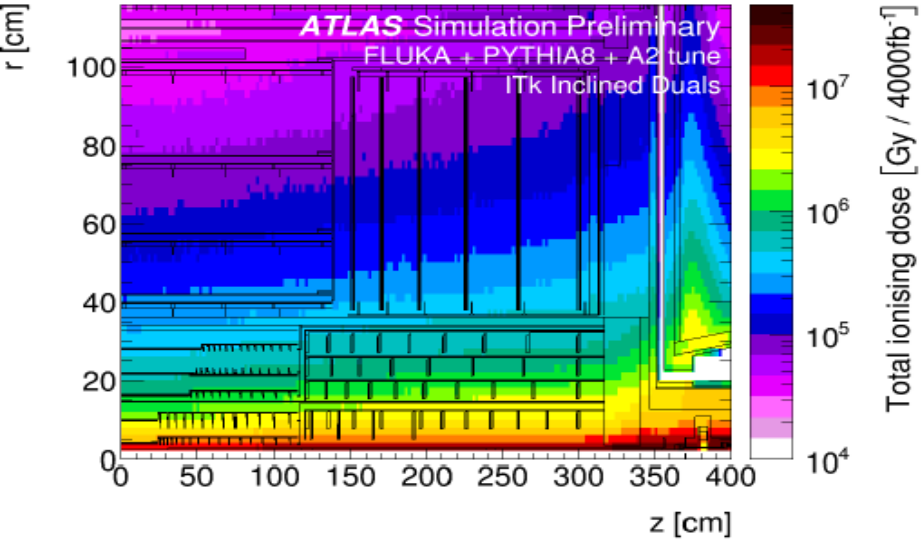
SUMMARY: Expertise

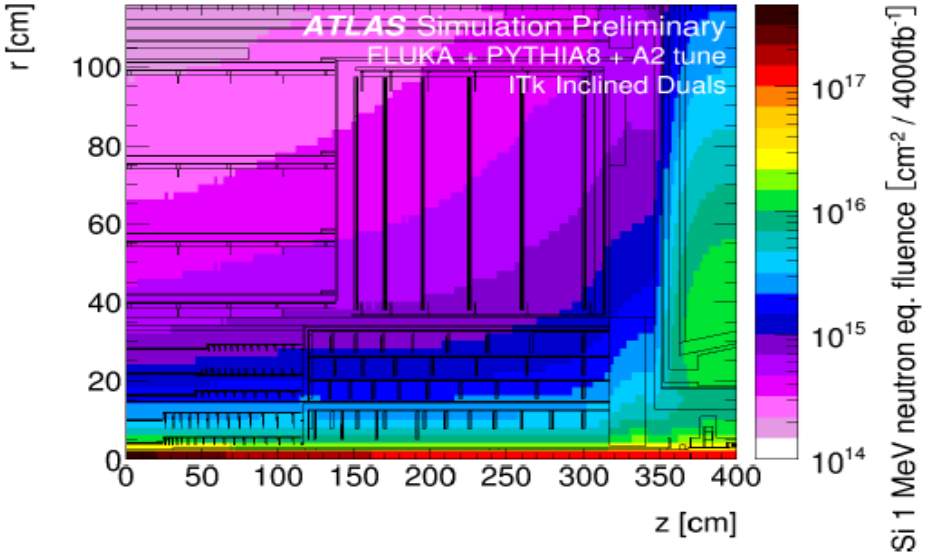
Developments with important Brazilian participation in designing and production

- ➢ ASIC: SAMPA
- ➢ FPGA: TMDB, Energy Estimation, Trigger (ML)
- ➢ MCU: everywhere, SoC.
- OpenIPMC : software implementing an Intelligent Platform Media Controller

Radiation-Hardness: a number of good facilities that can be used for design support and testing

SUMMARY: Rad-Hard in HL-LHC





- **TID > 10 MGy and 1016 1 MeV n/cm2 fluence in ITk inner system** *(100x Run-2 values)*: radiation tolerant ASIC designs
- **TID ~ 100 Gy and 1014 1 MeVn/cm2 in the outer layers of the detector** (20-30% increase): Allow using FPGA designs
- **Require qualification against TID (surface effects, transistor damage) and SEE (single event upsets, latch-up events)**