IFUSP
Instituto de Física da USP

HEPIC
IFUSP

Universidade de São Paulo

Workshop da Rede Nacional de Física de Altas Energias (RENAFAE) 2022

ASICs and Front-end electronics development at USP

Wednesday April 27th 2022

Marco Bregant

CNPq

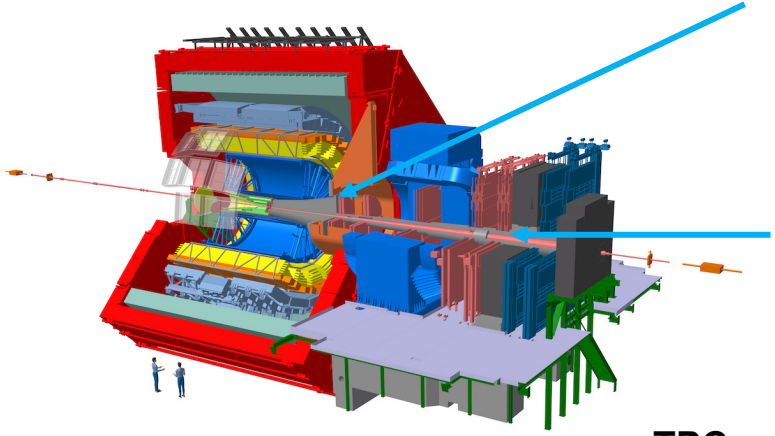
FAPESP

Outlook

HEPIC
IFUSP

- The beginning of the story
- SAMPA, what SAMPA can do / SAMPA performance
- A SAMPA-based small size acquisition system
- Future: a next generation ASIC

Why the SAMPA project? The motivations



For Run3 ALICE planed to operate at higher rate, recording all MB events

Goal: 50kHz in Pb-Pb (~10nb^{-1} in Run3 and Run4)

Upgrade detectors and electronics during Long Shutdown 2 (2020)

➢ Time Projection Chamber (TPC)

- GEM readout plane, high rate capability, continuous readout.

TPC electronics used till run2 was not made to amplify negative charge input (as GEMs provides) and cannot cope with the higher rate and with the continuous readout operation planned

➢ Muon Chamber (Forward muon spectrometer)

- Higher rate capability, new acquisition electronics chain in ALICE

new electronics needed

TPC required a new readout, MCH too.

A common project to design a new ASIC: SAMPA

Partnership IFUSP - LSI (EP-USP)

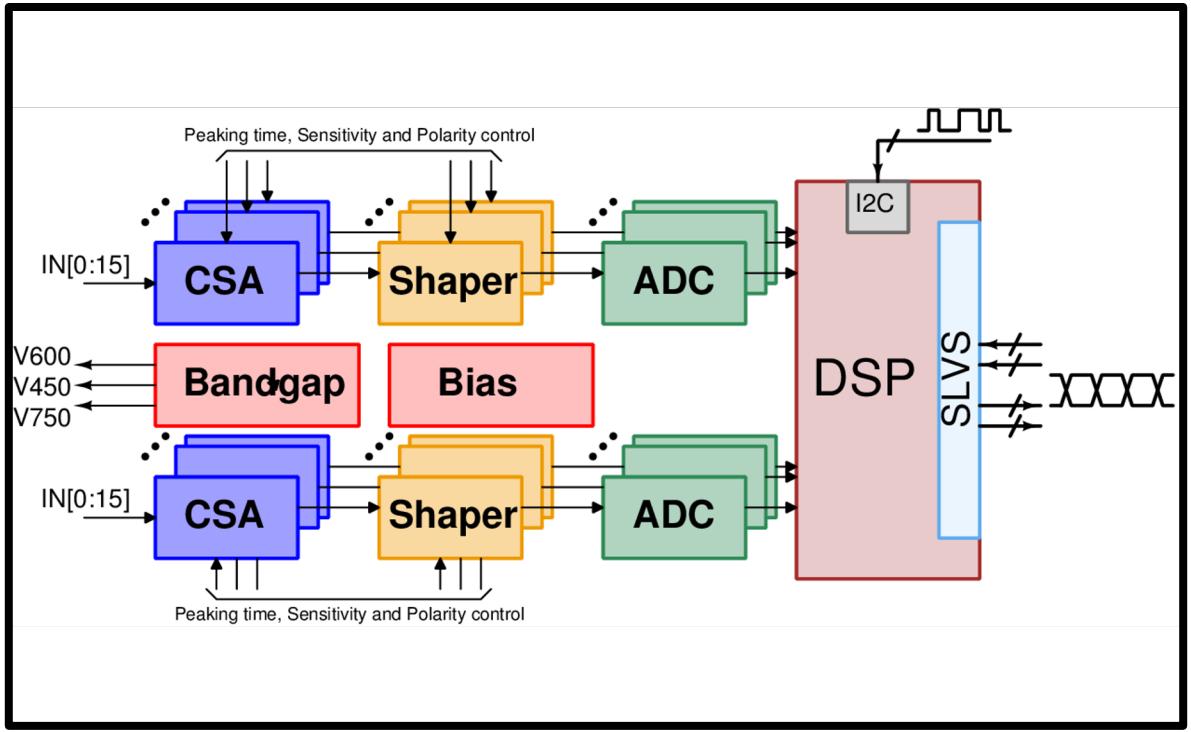
SAMPA Design Specifications Summary

- TSMC CMOS 130 nm, 1.25V technology
- 32 channels, Front-end + ADC + DSP
- package size ≤15x15mm^2 (total footprint)
- ADC: 10-bit resolution, 10MS/s, ENOB>9.2 (20 MS/s)
  (Alice TPC is eventually using: 5MS/s, to keep BW requirement in the readout chain lower)
- DSP functions: pedestal removal, baseline shift corrections, zero-suppression
- Data transmission: up to 11 e-link at 320 Mbps to GBTx, SLVS I/O
- Power < 32 mW/channel (Front End + ADC)

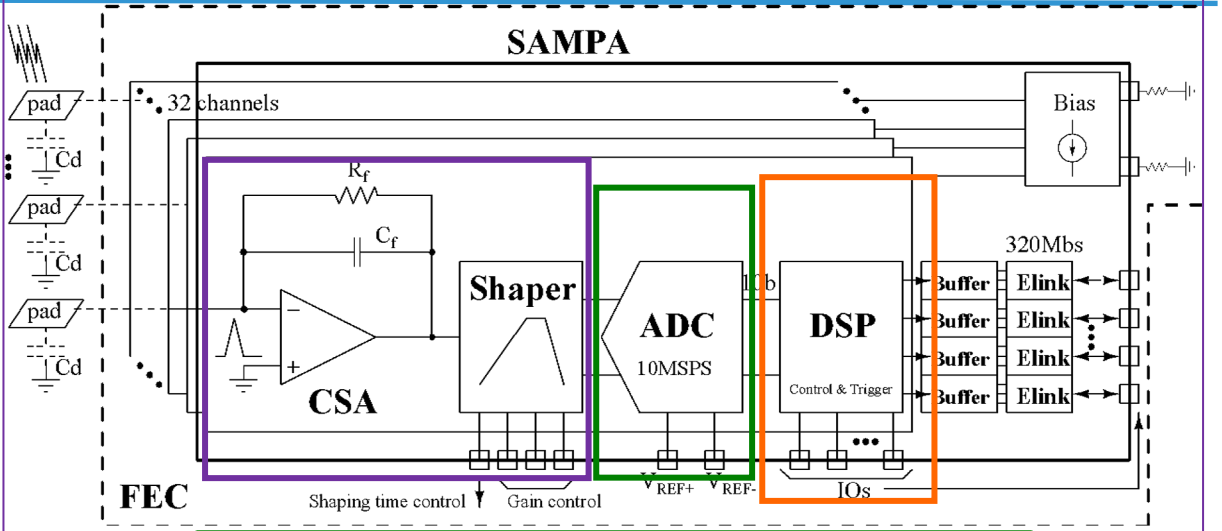
ALICE (V4)		sPHENIX (V5)
TPC Mode (V4)	MCH Mode (V4)	
▪ Negative Input charge ▪ Sensor capacitance: 12 – 25 pF ▪ Sensitivity: 20mV/fC & 30mV/fC ▪ Noise: ENC ≤ 580 e$^-$ @ 18.5pF ▪ Peaking time: ~160 ns ▪ Baseline return: <500 ns	▪ Positive input charge ▪ Sensor capacitance: 40–80 pF ▪ Sensitivity: 4mV/fC ▪ Noise: ENC ≤ 950 e- @ 40pF 1600 e- @80pF ▪ Peaking time: ~300 ns ▪ Baseline return: <550 ns	▪ Negative Input charge ▪ Sensor capacitance: 12 – 25 pF ▪ Sensitivity: 20mV/fC & 30mV/fC ▪ Noise: ENC ≤ 580 e$^-$ @ 18.5pF ▪ Peaking time: 80/160 ns ▪ Baseline return: <500 ns

SAMPA Block Diagram

One ASIC (preAmp, shaper, ADC, DSP), for 32 Chs



SAMPA Block Diagram



ADC:

- 10 bits SAR ADC, ENOB ≥ 9 bits (@10MS/s)
- A version to operate @20MS/s (V5) fabricated and available

Analogue part:

- Neg. Charge Pulse 20/30 mV/fC , 160 ns shaping, ENC < 500 @C_{det}=18.5 pF (v4)
- Pos. Charge Pulse 4 mV/fC , 300 ns shaping, ENC< 1000 @C_{det}=40 pF
- Version Neg/Pos 20/30 mV/fC 80/160 ns shaping (no low gain anymore) available too (V5)

Digital signal processor:

- Digital filters;
- ZS, data compression

Top Level Functionality

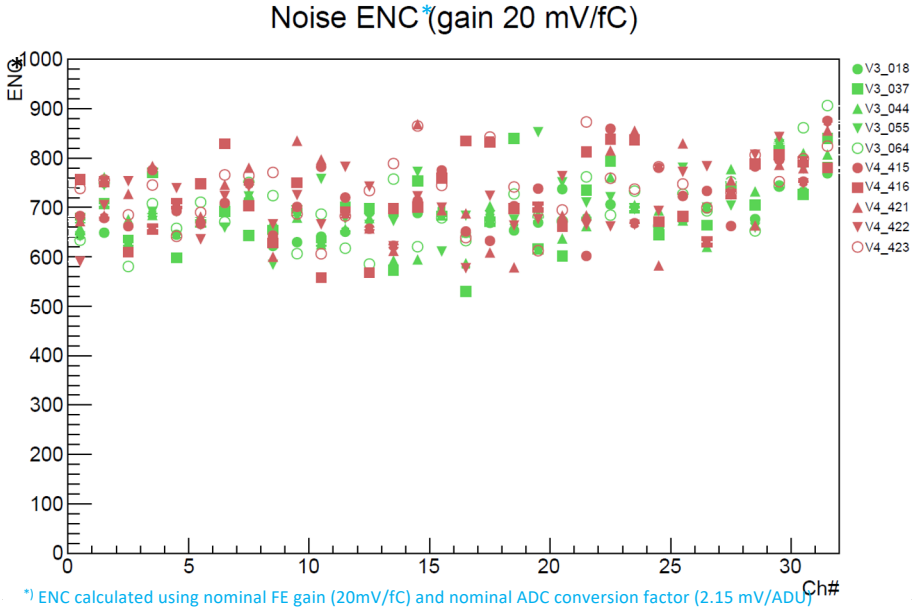
- 4 primary filter blocks
  - Individual correction per channel
  - Baseline correction
    - 1 FIR filter
    - 1 Slope based filter
    - 1 IIR filter
    - Lookup table correction(Pedestal Memory) f(t);f(din)
    - Conversion f(din)
    - Fixed correction
  - Tail cancellation
    - 1 IIR filter
- Configuration
  - Configurable through I2C
  - 1 global register unit, 32 sets of channel registers
- Radiation tolerant
  - TMR on almost all flip-flops
    - except on part of data path
  - Hamming protected headers
- Compression
  - Zero suppression with run length encoding
    - Forward linked list for easier decoding
  - Cluster sum
    - Uses zero suppression with run length encoding , but sums cluster into 20bit word
  - Huffman
    - Differential encoded data
    - Programmable table of codes for +17 to -17
    - Values outside table have special Huffman code prepended to raw 10bit value
- Design for test
  - JTAG boundary scan
  - Built in memory tester
  - Scan chain (on >98% of digital block flops)

Readout

- Selectable number of serial links up to 11
  - 320/160/80Mbps
  - Channels divided among links, no load sharing
  - Which channel goes to which link and in which order can be selected
  - Data is packet based (header + payload)
    - One packet per channel per event
- Event modes
  - Triggered
  - Continuous
  - Selectable event length up to 1024 samples
  - 192 pre-trigger samples
- Event buffer per channel
  - 6144(6K) words of compressed samples
  - 256 words of headers
  - Header still created if data memory goes full
- Daisy chain
  - Multiple devices can share a single serial link to readout unit
  - 2K word buffer in the receiving side
- Direct ADC serialization
  - Data serialized directly from ADC at 32xADC speed over 10 links
  - Raw data, no filtering, no headers
  - Sync pattern on startup, receiver should maintain sync after that
  - 2 modes
    - 10 bits is sent consecutively for channel 0-31 each 32xADC cycle
    - 5 lower bits, then 5 higher bits consecutively for channel 0-15 is sent on link 0-4 and for channel 16-31 on link 5-9
  - Clockgate the rest of the system to save power

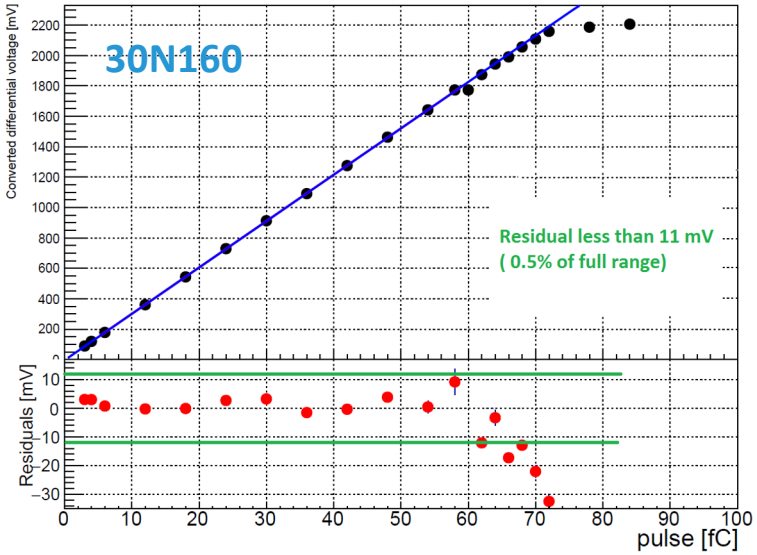
Example results from SAMPA qualification

(example of inside chip noise distribution)



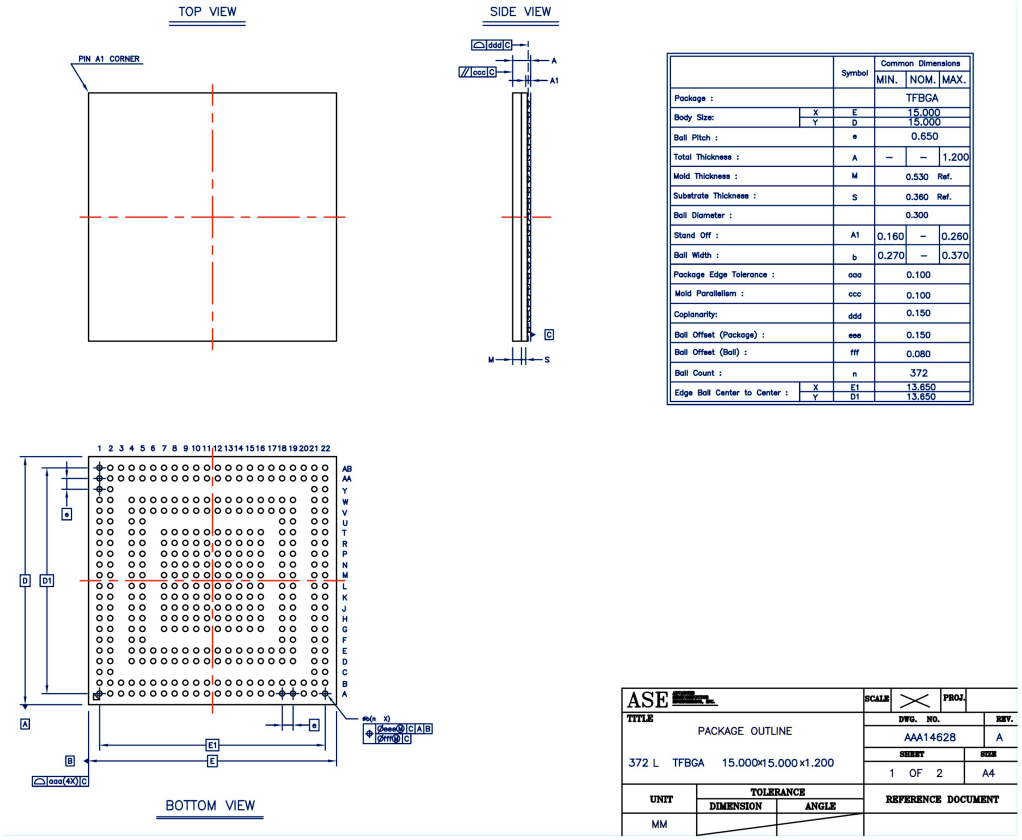
*) ENC calculated using nominal FE gain (20mV/fC) and nominal ADC conversion factor (2.15 mV/ADU)

Linearity and Residual – an example



SAMPA Package

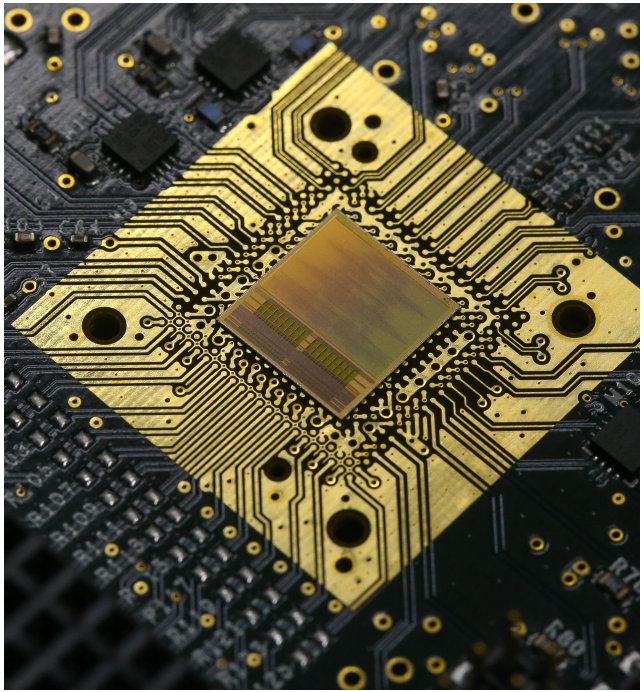
- TFBGA package
- 15 mm x 15 mm body size
- 1.2 mm thickness
- 0.65 mm ball pitch.
- 372 balls
  - 4-substrate layers



		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package :				TFBGA	
Body Size:	X	E		15.000	
	Y	D		15.000	
Ball Pitch :		e		0.650	
Total Thickness :		A	–	–	1.200
Mold Thickness :		M		0.530 Ref.	
Substrate Thickness :		S		0.360 Ref.	
Ball Diameter :				0.300	
Stand Off :		A1	0.160	–	0.260
Ball Width :		b	0.270	–	0.370
Package Edge Tolerance :		aaa		0.100	
Mold Parallelism :		ccc		0.100	
Coplanarity:		ddd		0.150	
Ball Offset (Package) :		eee		0.150	
Ball Offset (Ball) :		fff		0.080	
Ball Count :		n		372	
Edge Ball Center to Center :	X	E1		13.650	
	Y	D1		13.650	

ASE	SCALE:	PROJ.	
TITLE: PACKAGE OUTLINE		DWG. NO.	REV.
		AAA14628	A
372 L TFBGA 15.000x15.000x1.200		SHEET 1 OF 2	SIZE A4
UNIT: MM	TOLERANCE: DIMENSION / ANGLE	REFERENCE DOCUMENT	

SAMPA is a presently available chip!



No doubt, it's a nice ASIC!

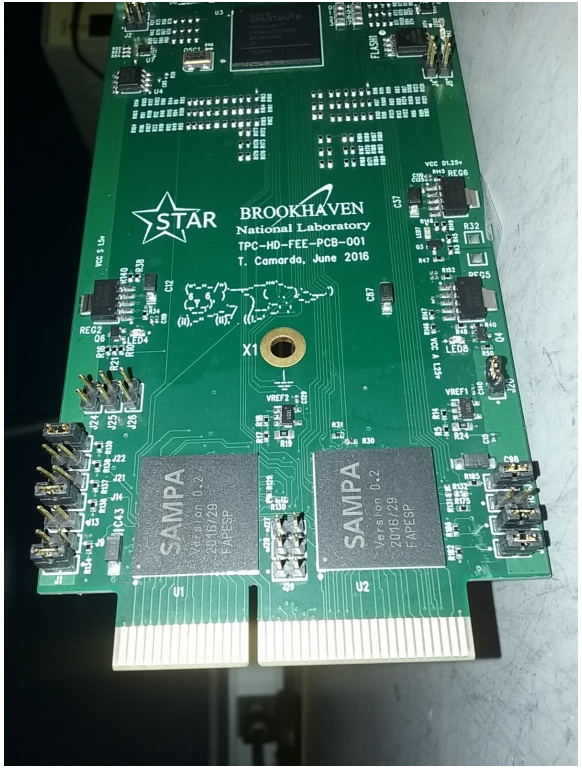
Nevertheless 'useless' on its own!

It needs to be host in a card that allows to plug its inputs to the detector, and the communication lines to an acquisition system (not mentioning providing power)

not only ALICE

How is it being used?

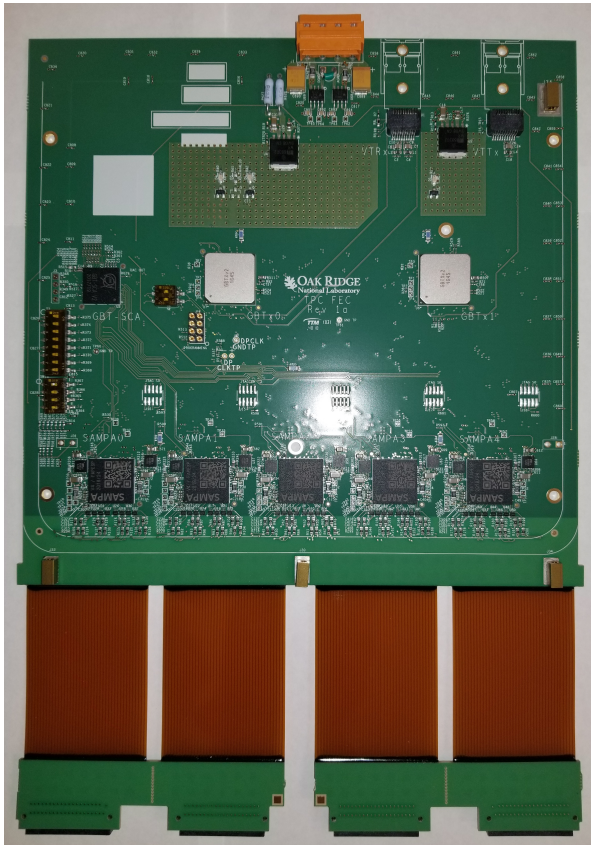
Already in use! (custom FE of the experiments)



STAR (@BNL) FEC.
FIRST use of SAMPA in a operational experiment

ALICE MCH FECs

ALICE TPC FEC



Can we use that on our lab?

- Three different systems already developed front-end cards for SAMPA.
- All of them are very custom:
  - #chs/card fitting detector needs
  - Connections and card size optimized for the specific detector
  - Designed to be integrated in a complex acquisition system (e.g. ROC->CRU->CPU) specific of the experiment.
  - Complete system with heavy overhead, e.g. custom chips

Very difficult to (re-)use any of them for daily activity in the lab or for small scale experiment.

The SRS system by RD51

How to have a readout for local use and small experiments

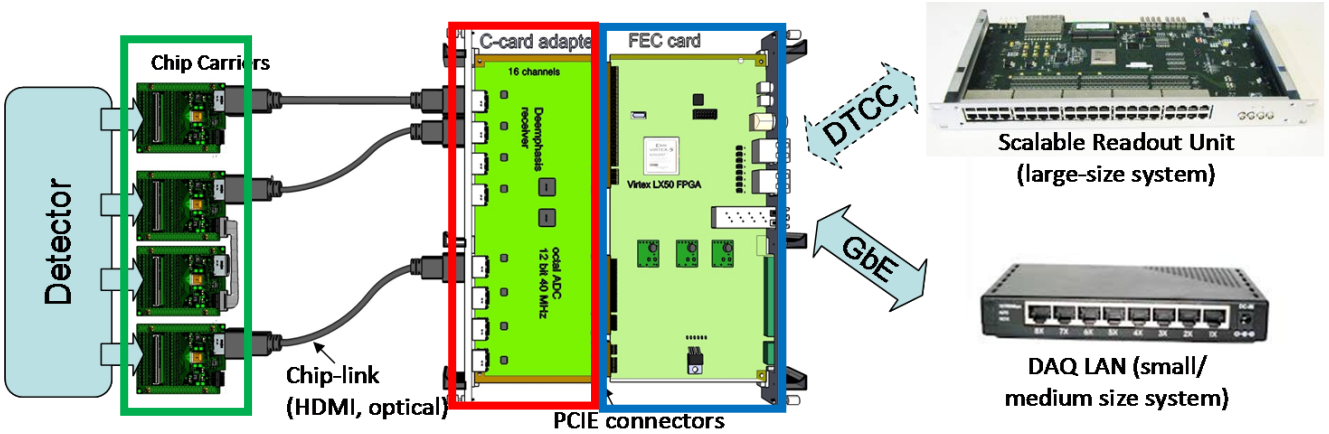
The SRS system

A Readout system developed inside/by the RD51 community (project ongoing since more than 10 years)

- A complete Scalable Readout System
- Using DATE Online system
- Modular structure
  - A Scalable Readout Unit (SRU)
  - A Programmable Front End Cards (FECs)
  - ASIC specific hybrid

The SRS idea

crate close to the experimental apparatus



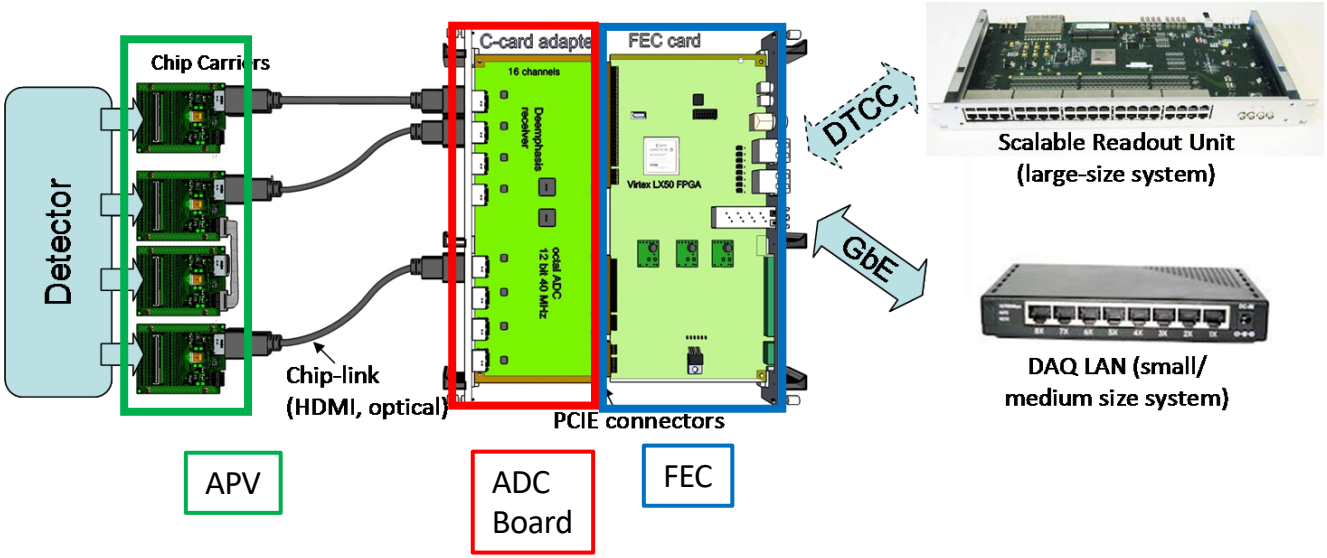
Front-end ASIC (close to detector)

An interface between ASIC and FEC card

FEC: handle the data taking of a set of ASIC. Handle the communication with the Readout Unit / DAQ

e.g. System used for now (by many groups around the world)

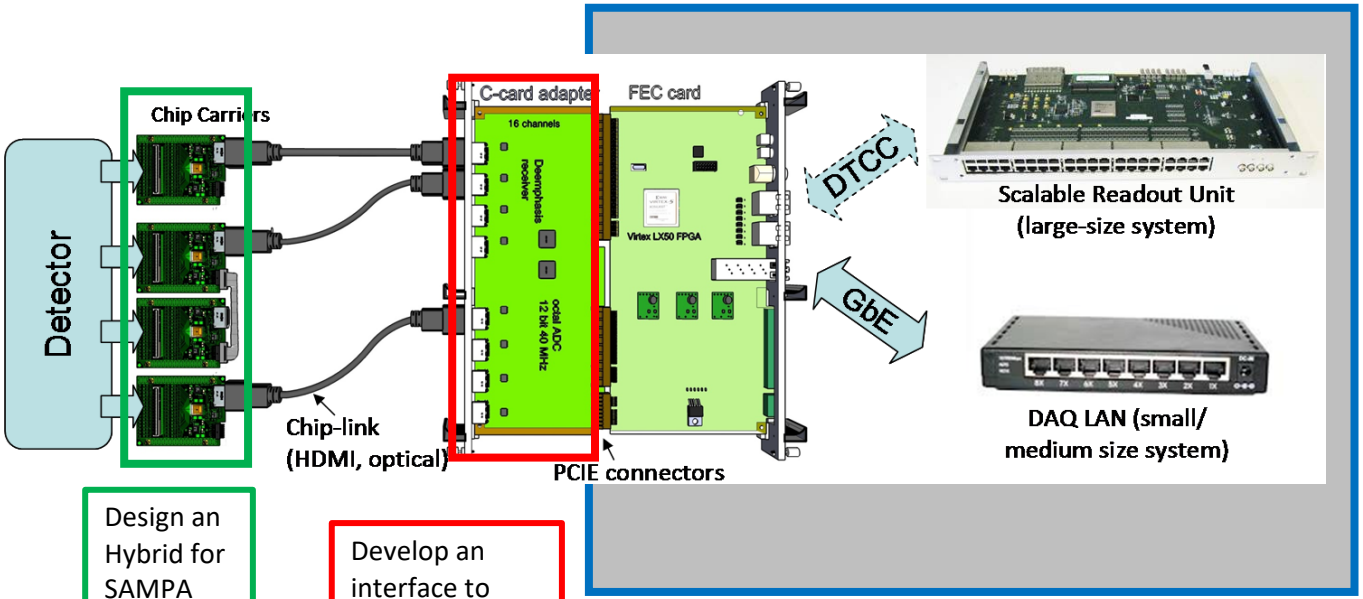
crate close to the experimental apparatus



APV is (was) a nice ASIC... But limited in acquisition rate..

A faster, VMM-based system, in under development, becoming available

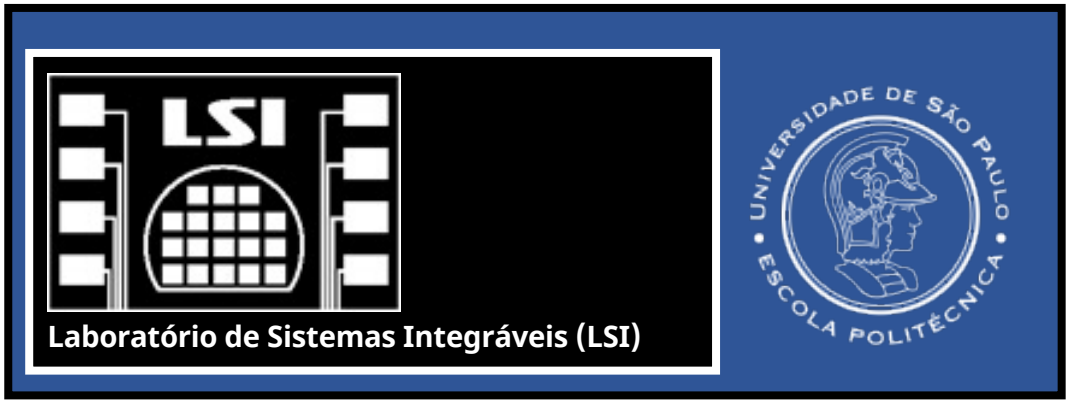
“Our short” term plan



Design an Hybrid for SAMPA

Develop an interface to manage the communication with SAMPA

KEEP/reuse, but FEC FPGA firmware

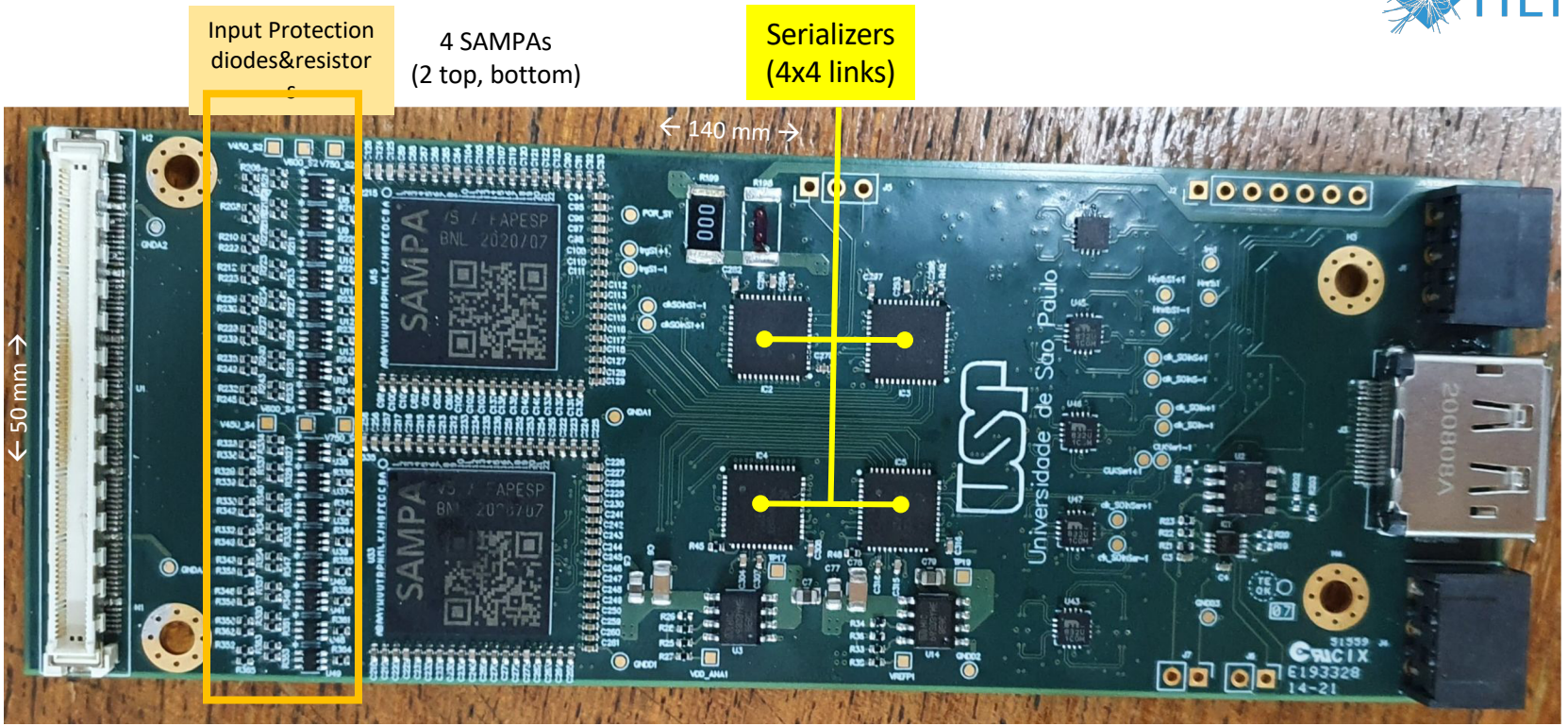


SAMPA into SRS, R&D

A joint effort IFUSP/EPUSP,

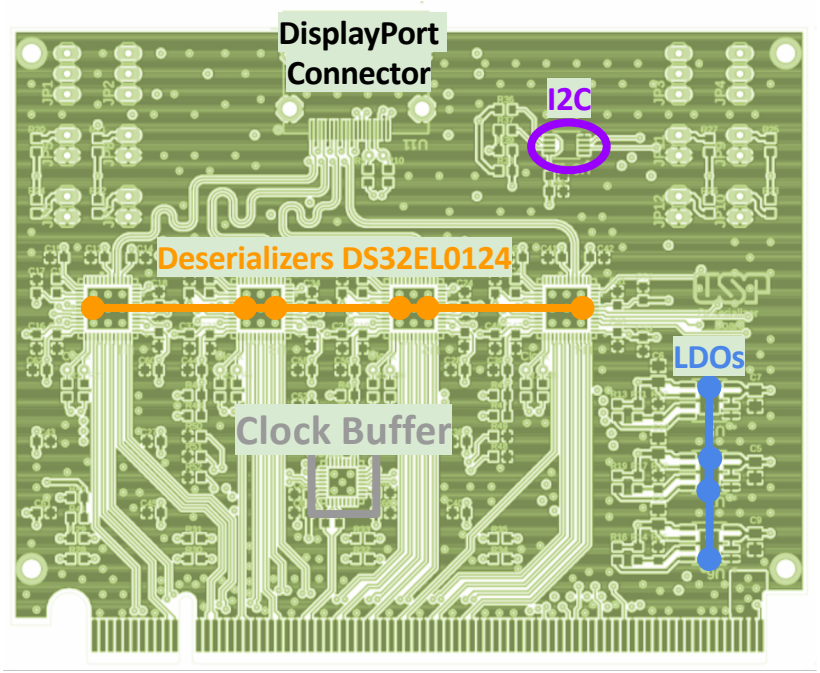
Tarciso Alvim Martins, Cesar Giacomini Penteado, Bruno Sanches, Hugo Daniel Hernandez, Marco Bregant, Marcelo Gameiro Munhoz, Wilhelmus Van Noije

Status/ Hybrid Board



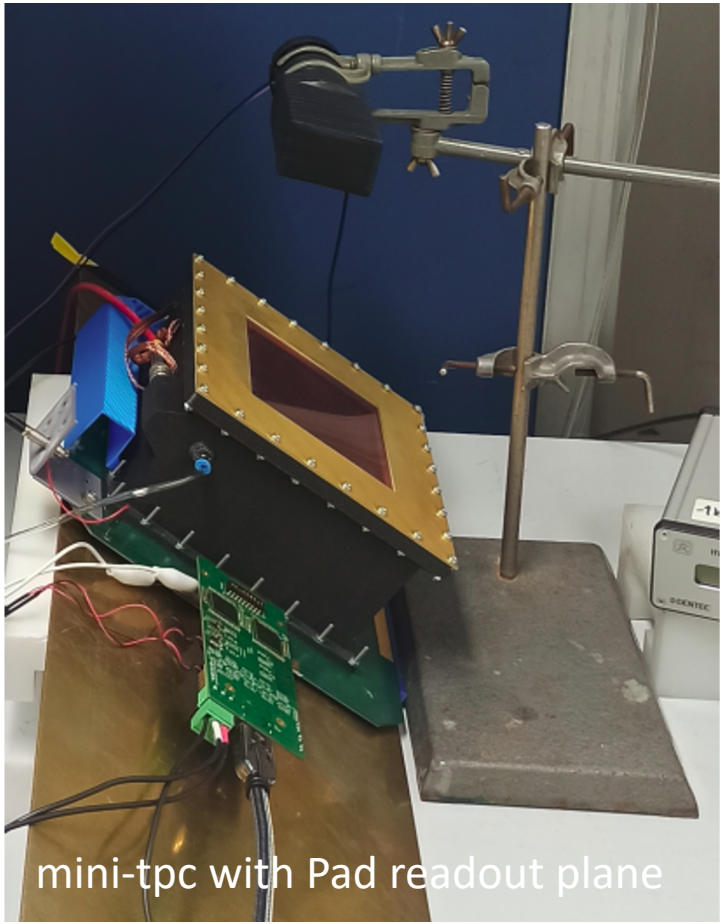
- DisplayPort connector - 5 DIFF lanes + 4 SE lanes.
- Serializer: DS32EL0421 - Translates 4 SAMPAs e-links to 1.
- I2C communication for configuration (SRS Slow Control).

Status/ Interface Board prototype

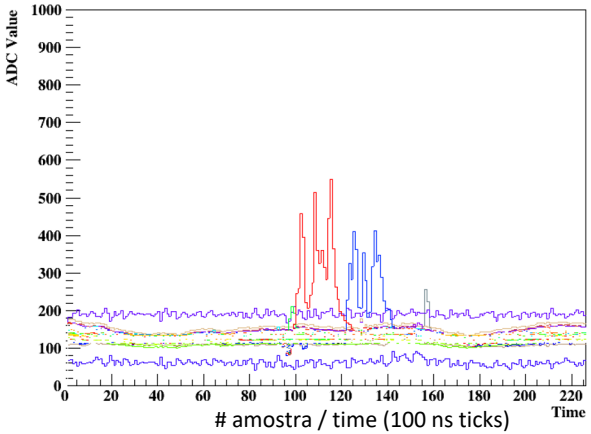


- DisplayPort Connector - 4 data links + 1 CLK + RST + TRG + I2C .
- Deserializer : DS32EL0124 - Recover the 4 SAMPA e-links.
- Only 1 Hybrid for now (16 ADIFFs for SAMPA serial Links + 1 Clock + 4 recovered clocks) at PCI connector.

Prototype in use @ÚTEF-CTU (Prague)



SAMPA-SRS prototype tested by a collaborating Group

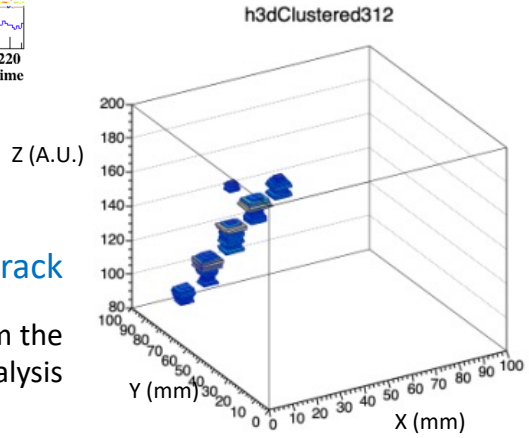


the waveforms of a event

SAMPA latency was set to 10 ns (100 amostras do ADC) for sake of developping and debugging studies

A reconsructed track

A first result from the preliminarly analysis



What's about ASIC "core" activities?

We learned so much, we acquired a lot of experience, during the SAMPA development.
Of course we DO continue direct involvement in ASIC design and qualification

FoCal-E Pad Readout Electronics

A new Forward Calorimeter for the ALICE experiment.

- It's a calorimeter, high dynamical range is required
- Our SAMPA does not meet that.
- Developing a brand new ASIC not feasible
  - would take years
  - FoCal need just few thousands chips (scale too low for a reasonable cost/chip!)
- there is on the market an existing ASIC: HGCROC, but need to be characterized for FoCal use

Participation in the study, characterization, and validation

i.e. profiting of the lab and the large experience acquired while deeply testing the SAMPA

A next generation SAMPA? .

SAMPA represented quite a success, it's presently THE choice for the readout of several TPC across the world.

- 130 nm technology? available for how long?
- Fits well TPC-like use, less gaseous tracker needs
- Gaseous detector still foreseen for several applications in the next decade and beyond

A collaboration with IRFU (Saclay, France) has been set up. Target:

- a versatile FrontEnd ASIC in 65 nm technology.

"versatile" = Large ranges in term of signal amplitudes, electrode capacitances, peaking times.
Sampling rate: 40 MSps minimum.

Applied for an ANR/FAPESP joint grant.

Conclusions and outlook

- SAMPA chip was developed and validate mainly locally at USP: a lot of experience acquired
- The ASIC is quite a success: beside ALICE, used by STAR@RHIC, MPD@NICA, sPHENIX@RHIC …
- **But we were not able to use it for our detectors in the lab!**
  - Action: Integrate the SAMPA in the SRS:
    - Entering in a ecosystem already in use
    - Small system, best fitting lab needs
    - That will allow also other small groups to make use of SAMPA (complete acquisition system, not just “a chip”)
    - Still scalable up to thousand of Chs.
  - **First complete SAMPA-SRS acquisition prototype fabricated and successfully tested.**
- Keeping us active with ASICs verification and design
  - participating to the project for the FoCal-E Pad readout electronics (testing and validation)
  - partnership with a French group to start the design of a next generation ASIC for gaseous detector (and, if feasible, make it versatile enough for an even wider use)

Thanks!