

Workshop da Rede Nacional de Física de Altas Energias (RENAFAE) 2022

Trigger de Múons de Primeiro Nível Assistido pela Calorimetria (TileCal) no Experimento ATLAS







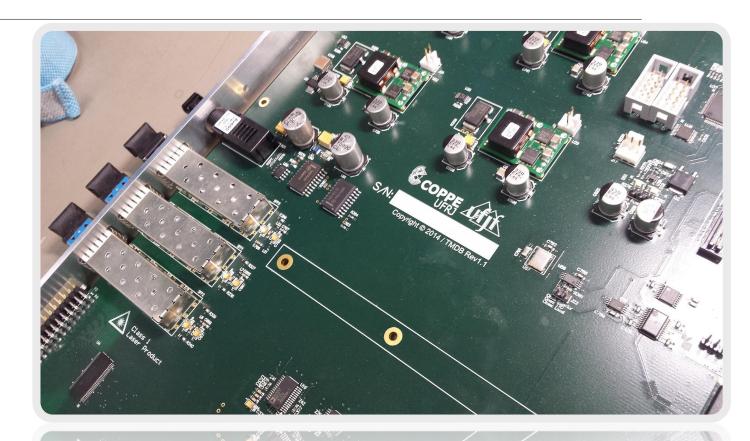
VICTOR A. FERRAZ on behalf of TMDB team





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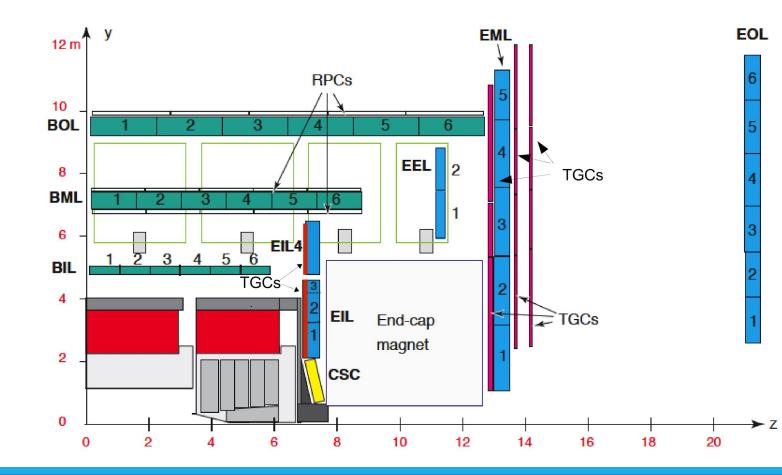
- Muon Trigger Assisted from TileCal
- System Overview
- Operation results
- Updates





Introduction

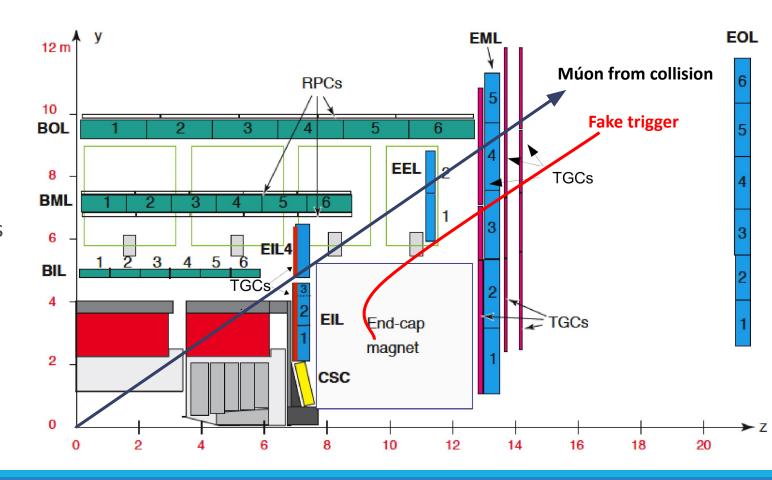
A significant part of the muon trigger rate in the end-caps is background





Introduction

- A significant part of the muon trigger rate in the end-caps is background
 - Low energy particles (mainly protons) produce fake triggers by hitting the end-cap trigger chambers





Introduction

Expected single-muon Level-1 rate (based on 2012 data and 8 TeV) with bunch spacing 25 ns and instantaneous luminosity 3 ×10³⁴ cm⁻² s⁻¹ for online p_T > 20 GeV

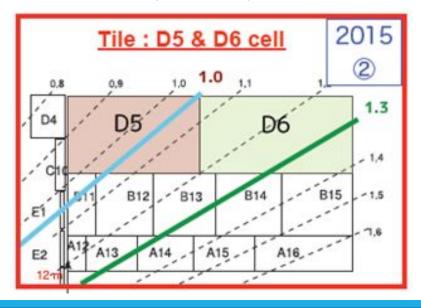
• From ATLAS TDAQ System: Phase-I Upgrade TDR

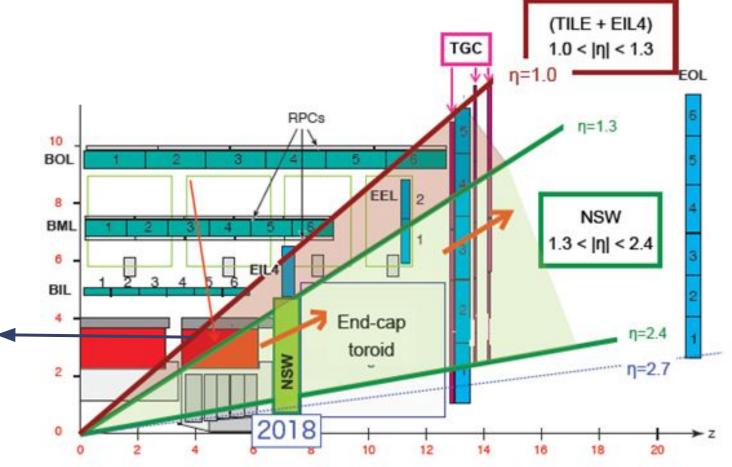
Online	No	TGC EIL4 +	TGC EIL4 +	TGC EIL4 +
$p_{\rm T} > 20 { m GeV}$	Change	(TGC FI or NSW)	(TGC FI orNSW)	(TGC FI or NSW)
$3 \times 10^{34} \mathrm{cm}^{-2} \mathrm{s}^{-1}$		w	+ Tile Cal.	+ Tile Cal.
				+ low field mask
	Rate [kHz]	Rate [kHz]	Rate [kHz]	Rate [kHz]
Run 2 (pre NSW)	51	34	31	28
Run 3 (post NSW)	51	17	15	13



Introduction

The Tile-μ trigger aim to improve the rejection of fake triggers, by using the using the energy loss in the TileCal outermost layer (D-layer)

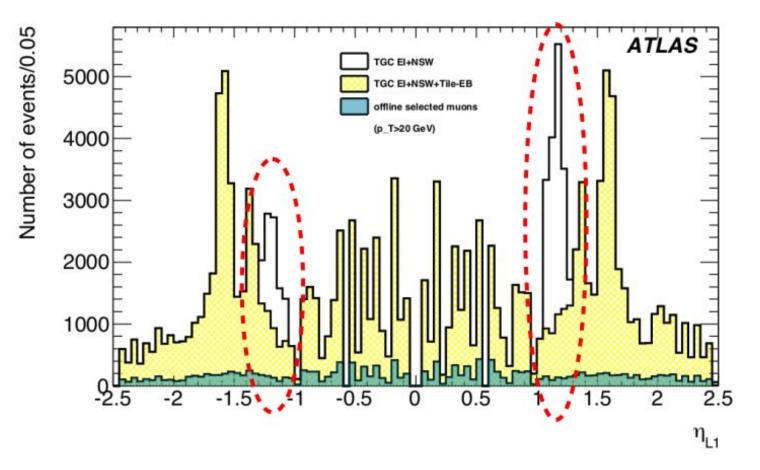




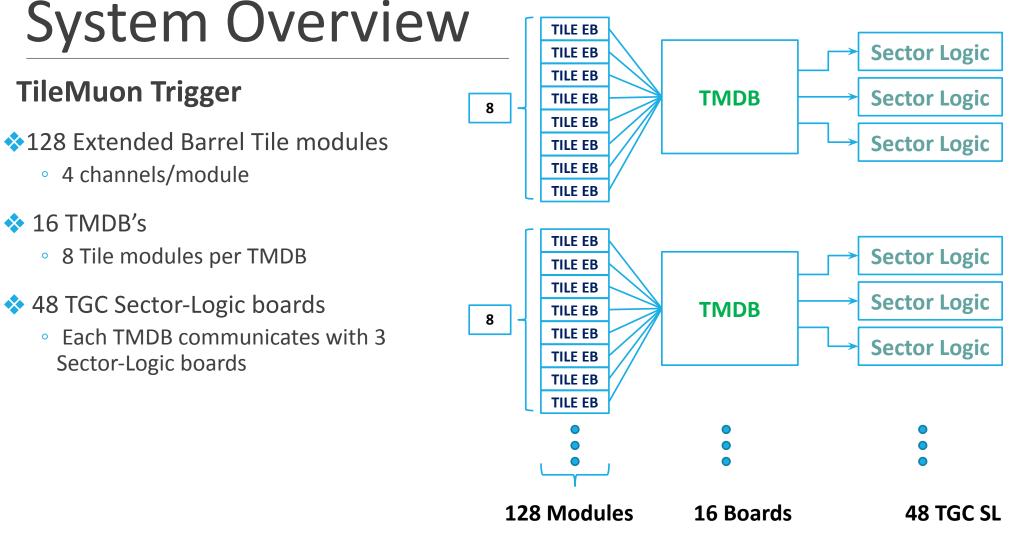


Introduction

- Use Tile Calorimeter D-layers in the region 1<|η|<1.3 in coincidence with the TGC inner station chambers
- By simulation, using a threshold of 500 MeV:
 - 97 % efficiency
 - 17 % rate reduction







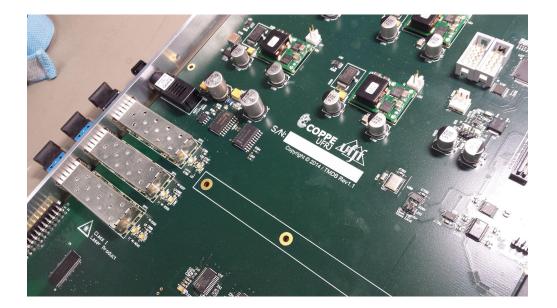
27/04/2022

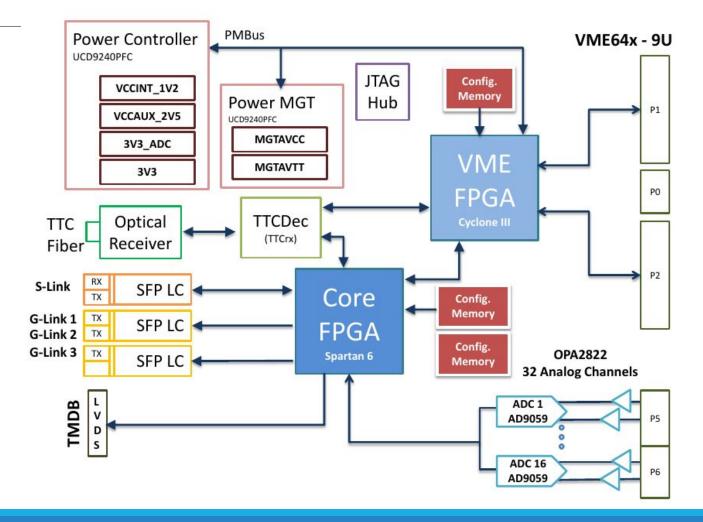


System Overview

Hardware

TileMuon Digitizer Board

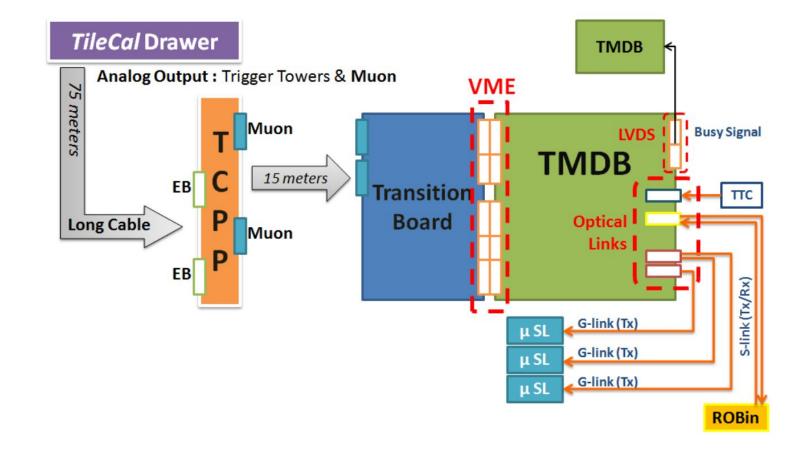




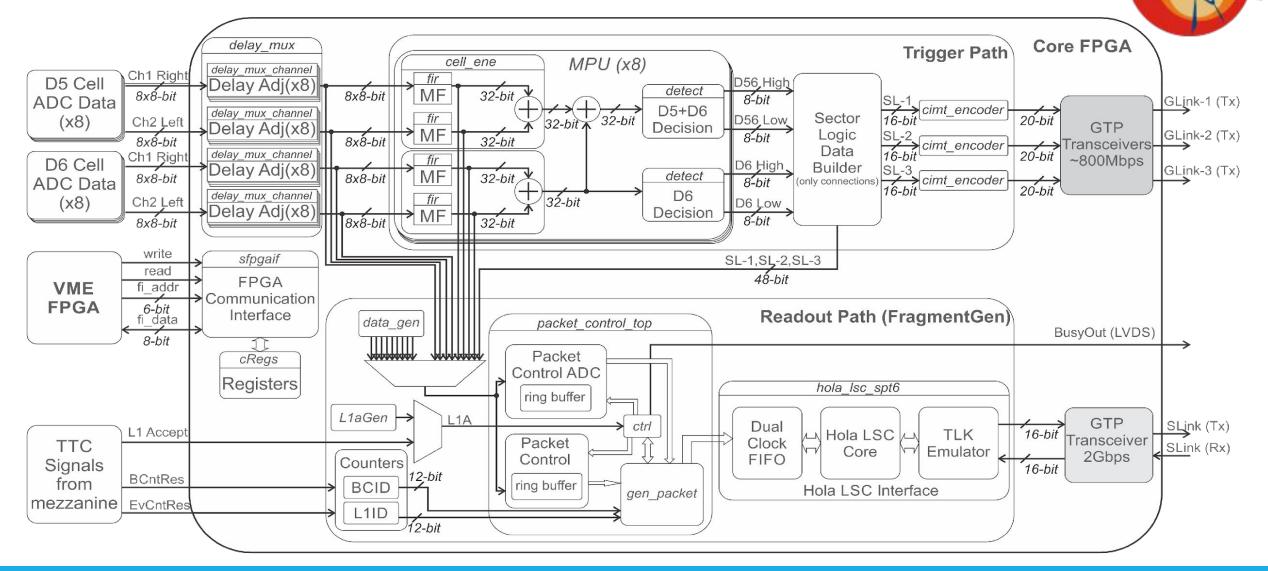


System Overview

♦ Signal Path



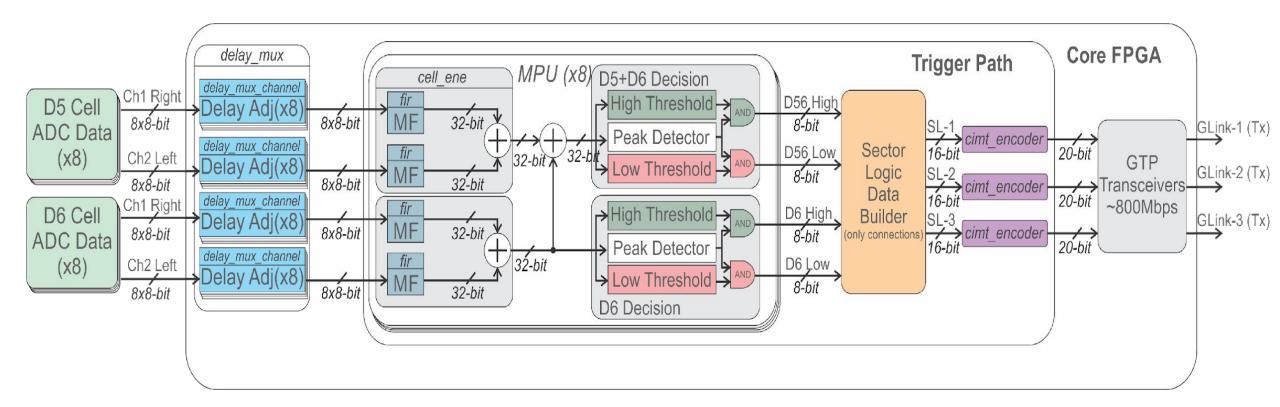
FPGA Implementation: core



FPGA Implementation: core **Core FPGA** delay mux Trigger Path cell ene MPU (x8) delay mux channel Ch1 Right fir D5 Cell D56, High Delay Adj(x8) detect MF 32-bit 8x8-bit 8xế-bit 8-bit GLįnk-1 (Tx) ADC Data SL-1 *cimt_encoder* D5+D6 delay mux channel 20-bit fir 32-bit 🖌 32-bit Sector (x8) D56 Low Ch2 Left Delay Adi(v8) GTP Decision k-2 (Tx) TRIGGER Ank-3 (Tx) (only connections) 32-bit detect ЦÌ 8x8-bit 8x8-bit ADC Data 8-bit 20-bit delay mux channel D6 32-bit D6 Low (x8) Ch2 Left Delay Adj(x8) Decision 8xế-bit 8x8-bit 32-bit write sfpgaif SL-1,SL-2,SL-3 read 48-bit FPGA VME fi addr Communication **FPGA** 6-bit Interface Readout Path (FragmentGen) fi data data g packet control top BusyOut (LVD 8-bit ĴĹ Packet cRegs Registers READOUT L1aGen L1A GTP SLink (Tx) Dual ctrl L1 Accept Hola LSC TLK 16-bit Transceive Packet Clock TTC SLink (Rx) Emulator Core 2Gbps FIFO Control Counters Signals 16-bit 12-bit **BCntRes** from ring buffer BCID Hola LSC Interface gen packet mezzanine EvCntRes L1ID J12-bit

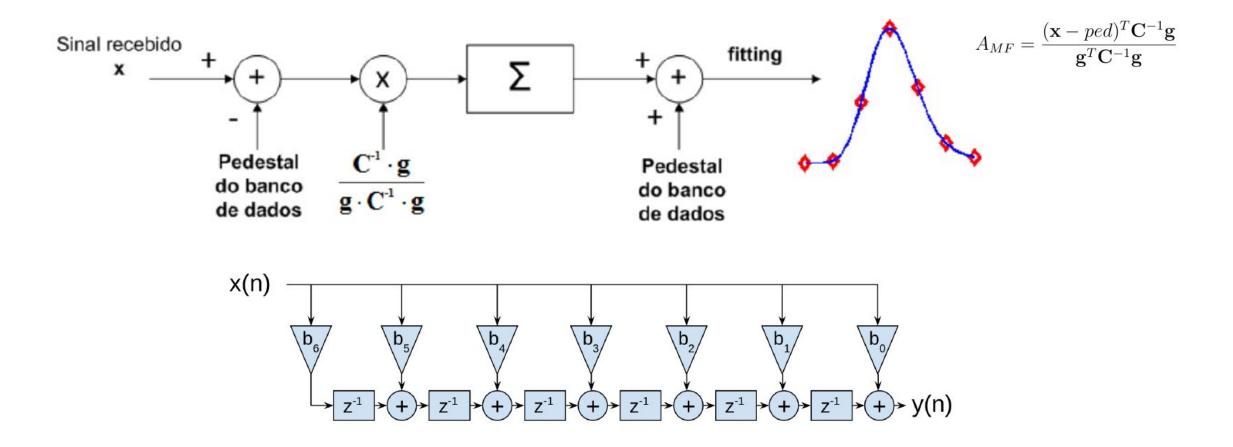


FPGA Implementation: Trigger





FPGA Implementation: Matched Filter

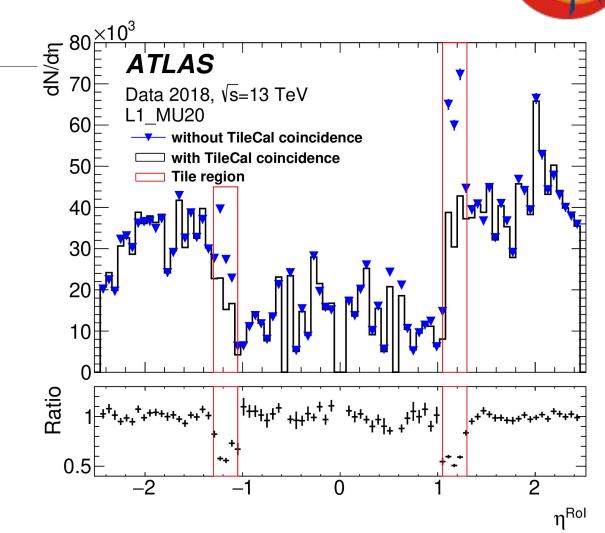




Operation Results

The L1 MU20 candidates

A comparison between η^{Rol} of all the L1 MU20 entries (white histogram) and the subset which passes the TileCal coincidence requirement (blue histogram) shows the amount of the additional reduction at 1.05 < |η^{Rol}| < 1.3 by the TileCal coincidence.

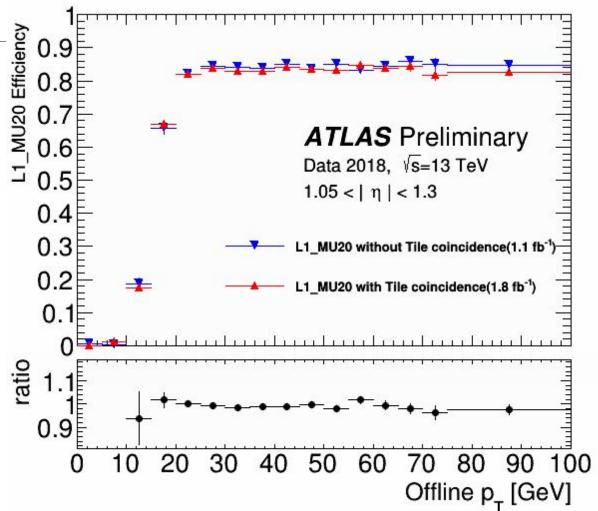




Operation Results

The L1 MU20 efficiency

- The trigger efficiency is compared between runs when TileCal coincidence is used in the Level-1 trigger decision (red) and is not used in the decision (blue)
- Additional inefficiency due to the TileCal coincidence is limited up to: ~ 2.5%

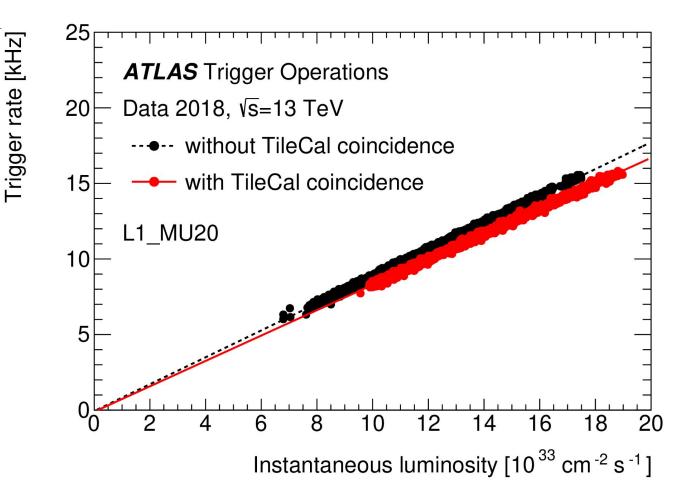




Operation Results

The L1 MU20 trigger rate

- Coincidence at 1.05 < |η| < 1.3 discards charged particles that only traverse the big wheel, which are originated from secondary interactions in the ATLAS Endcap toroid of the beam backgrounds
- The comparison of the fit results shows that the reduction of the L1_MU20 trigger rate for all the muon spectrometer coverage is about 6% owing to the new TileCal coincidence requirement





Updates for Run 3

New "Firmware"

- Add Idle words for Sector Logic-TGC communication
- New Data Fragment for S-Link
- > Inclusion of new information from cell D5 (new MF as well)
- New Data Frame for Sector Logic-TGC
- Analysis
 - > Testing the wiener filter efficiency
 - > Performing Matched Filters calibration (new coefficients, including D5 cells)
- Extended Applying deep learning/ neural networks to classifying muons
 - Using the offline information to acquire muon event
 - Separating the training/test dataset
 - Implementing deep learning (CNN and RNN LSTM (Long Short-Term Memory)
 - Increasing statistics