CBPF
Centro Brasileiro de Pesquisas Físicas

MINISTÉRIO DA CIÊNCIA, TECNOLOGIA E INOVAÇÕES

PÁTRIA AMADA BRASIL GOVERNO FEDERAL

Development of the Slow Controller of the RPC System Link for LS2 Update of the CMS/HL-LHC Experiment

Workshop RENAFAE 2022 - CBPF-Rio Collaboration

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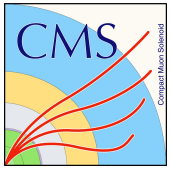


April 27th, 2022 - fmarujod@cern.ch

Overview

- **Muon System**
  - RPC Muon
  - Link Board/Control Board
  - New Link Board/Control Board
- **Slow Controller**
  - uTCA CRATE
    - **AMC13/MCH**
    - **uHTR**
    - **Kintex-7 EVB**
- **Preliminary and Expected Results**
  - Overview

RPC Muon - CMS HL-LHC Upgrade (Phase-2):

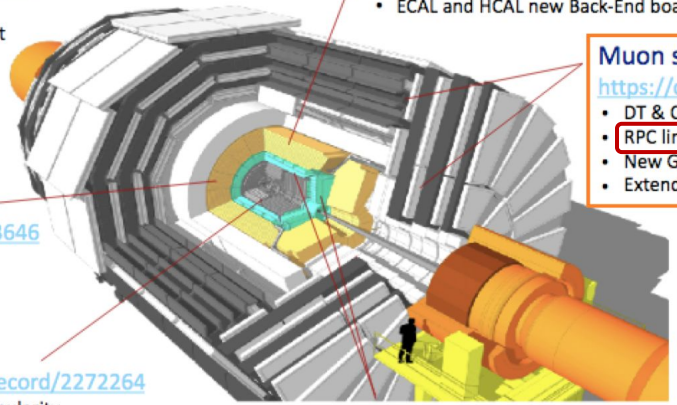
System Muon: Upgrade nas FE/BE readout e RPC Link Board

Technical proposal CERN-LHCC-2015-010 https://cds.cern.ch/record/2020886
Scope Document CERN-LHCC-2015-019 https://cds.cern.ch/record/2055167/files/LHCC-G-165.pdf

L1-Trigger/HLT/DAQ
https://cds.cern.ch/record/2283192
https://cds.cern.ch/record/2283193
- Tracks in L1-Trigger at 40 MHz
- PFlow-like selection 750 kHz output
- HLT output 7.5 kHz

Barrel Calorimeters
https://cds.cern.ch/record/2283187
- ECAL crystal granularity readout at 40 MHz with precise timing for e/γ at 30 GeV
- ECAL and HCAL new Back-End boards

Muon systems
https://cds.cern.ch/record/2283189
- DT & CSC new FE/BE readout
- RPC link -board
- New GEM/RPC $1.6 < \eta < 2.4$
- Extended coverage to $\eta \simeq 3$



Calorimeter Endcap
https://cds.cern.ch/record/2293646
- 3D showers and precise timing
- Si, Scint+SiPM in Pb/W-SS

Beam Radiation Instr. and Luminosity, and Common Systems and Infrastructure
https://cds.cern.ch/record/2020886

Tracker https://cds.cern.ch/record/2272264
- Si-Strip and Pixels increased granularity
- Design for tracking in L1-Trigger
- Extended coverage to $\eta \simeq 3.8$

MIP Timing Detector
https://cds.cern.ch/record/2296612
Precision timing with:
- Barrel layer: Crystals + SiPMs
- Endcap layer: Low Gain Avalanche Diodes

Innovative and extremely challenging new capabilities

New Hardware

- Control Board
- Link Board

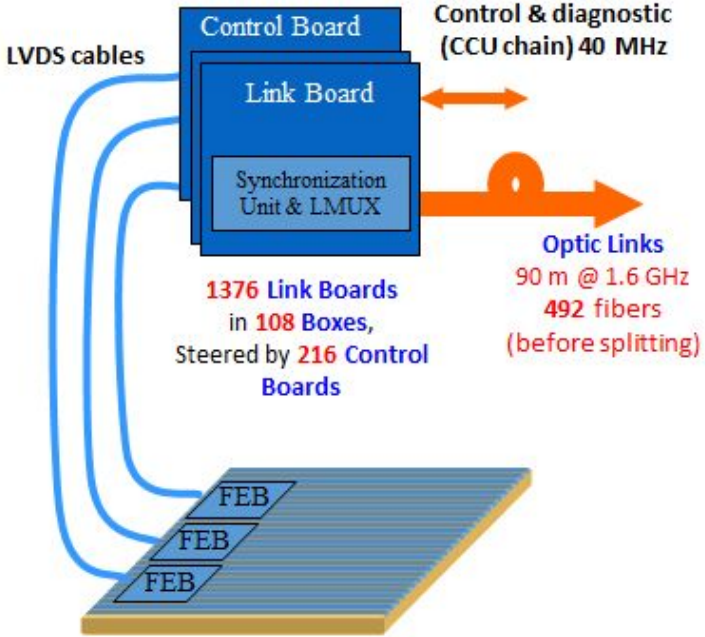
New Slow Controller

- Control Board
- Link Board
- Online RPC
  - Real Time
  - Dashboard

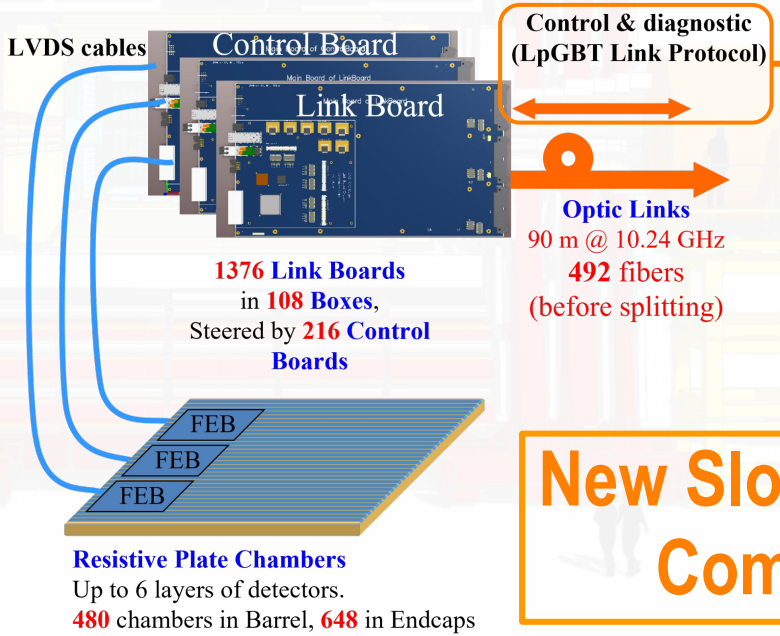
Link Board system Overview

Update motivation

Present Link Board System



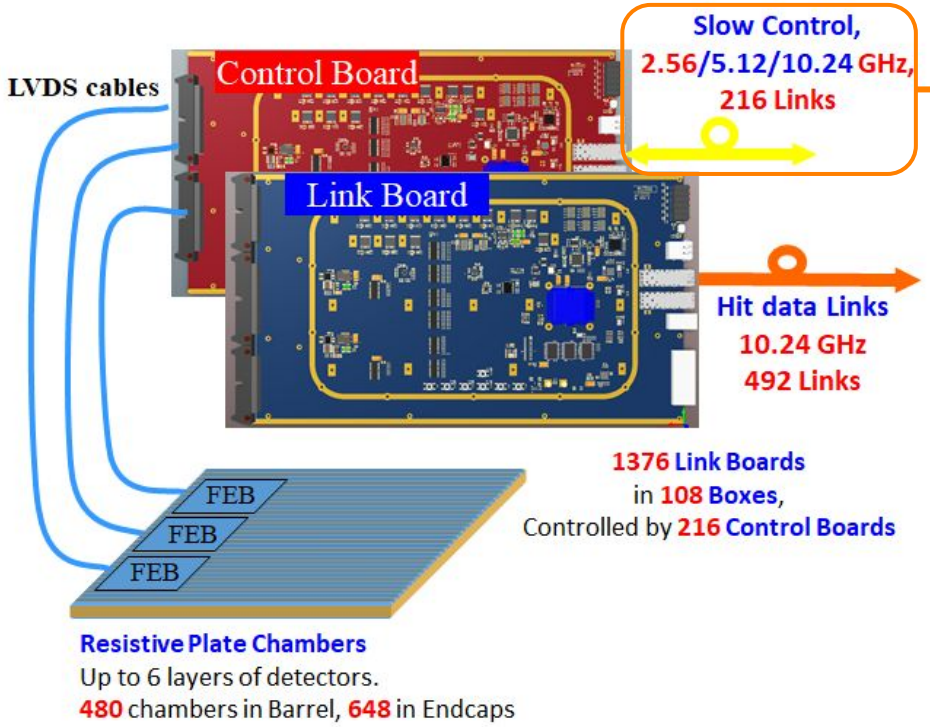
Upgrade Phase-II of New Link system



New Slow Controller Components

New Link Board system Overview

Based on Xilinx's Kintex-7 FPGA

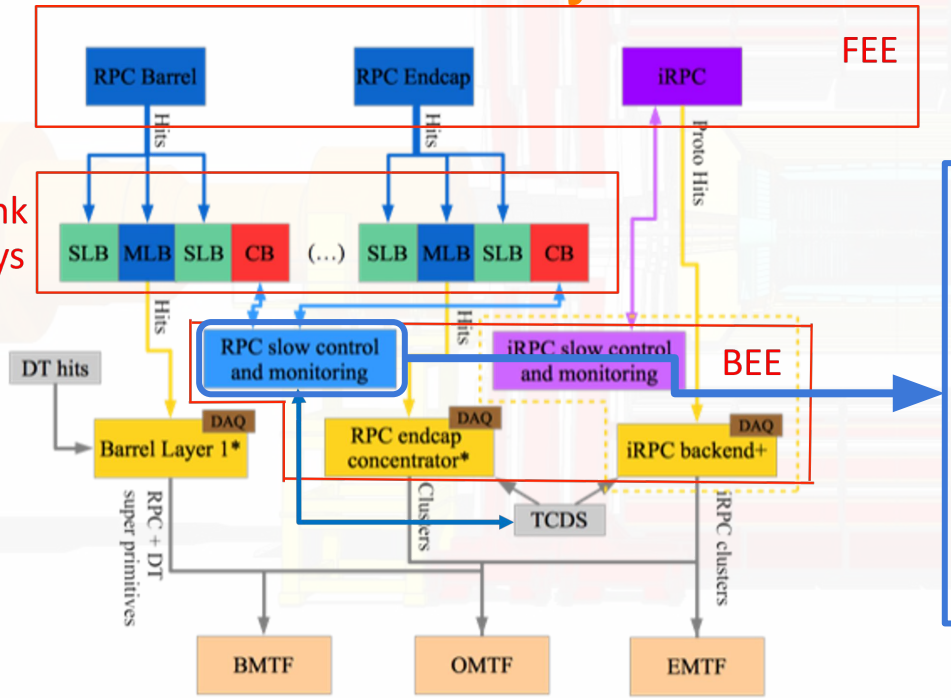


New Slow Controller

- FPGA XC7K160T - Version Industrial
- Redundant optical link
- Remote programming
- High-speed data transmission at FIXED LATENCE
- Point-to-point fiber optic connection between the control boards and the Slow Controller

What is Slow Controller?

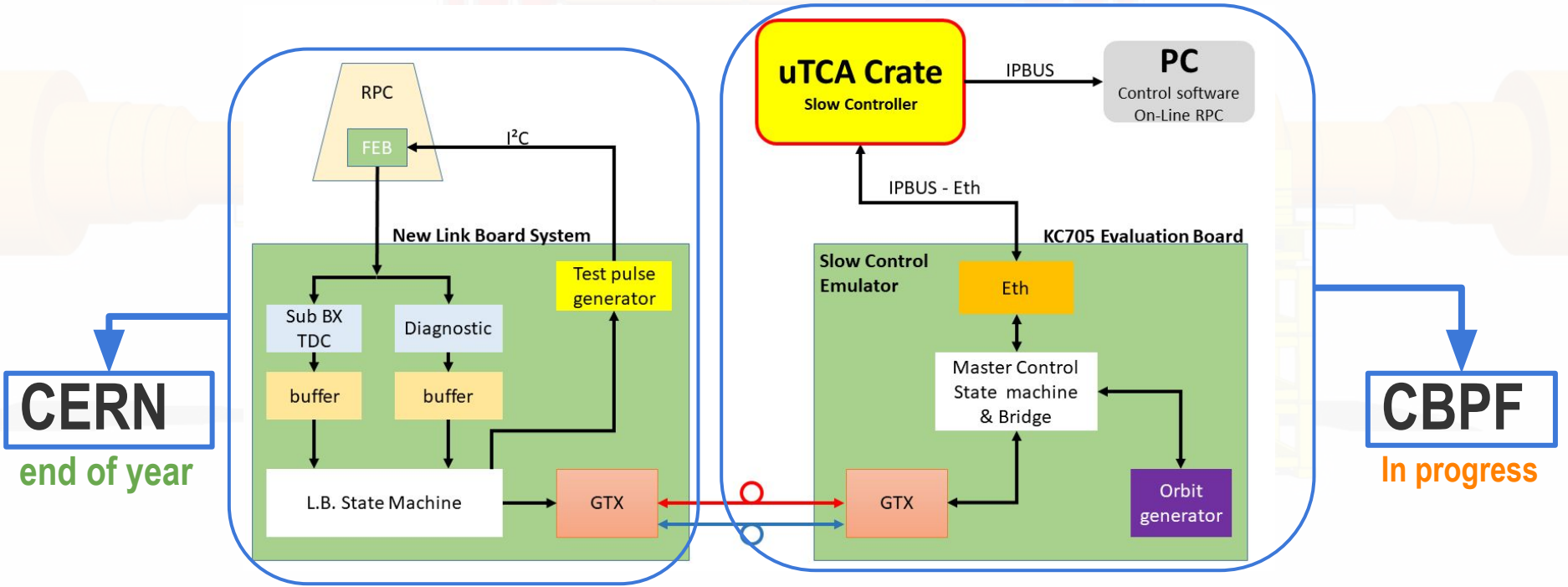
Slow Controller is Subsystem to monitor/control one or more systems



The main function of the Slow Controller in this project is to prevent failures, monitor, and control directly by the user or automated control.

Slow Controller development

Implementation: FPGA-Kintex7, Rack uTCA and AMC13

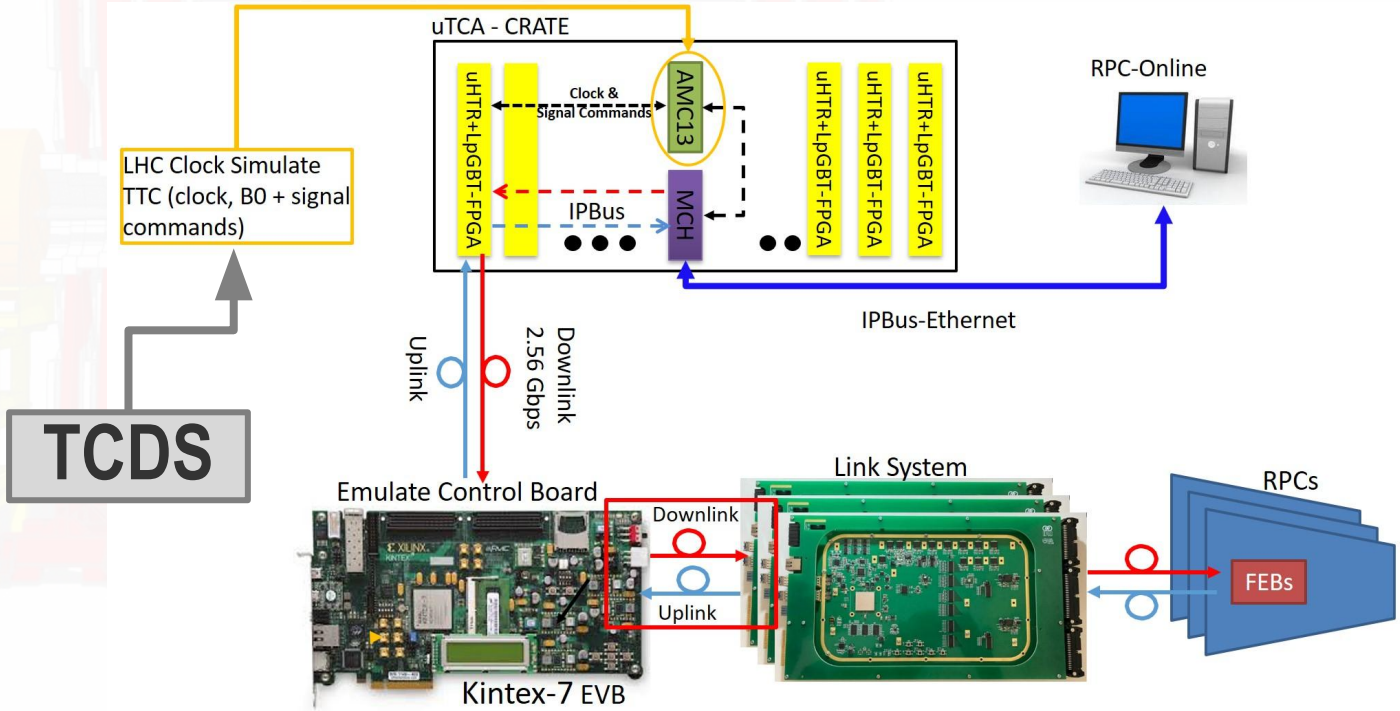


Slow Controller development

Hardware Implementation for Slow Controller

Big Challenge:
Integrate The CMS Timing and Control Distribution System (TCDS)

In progress

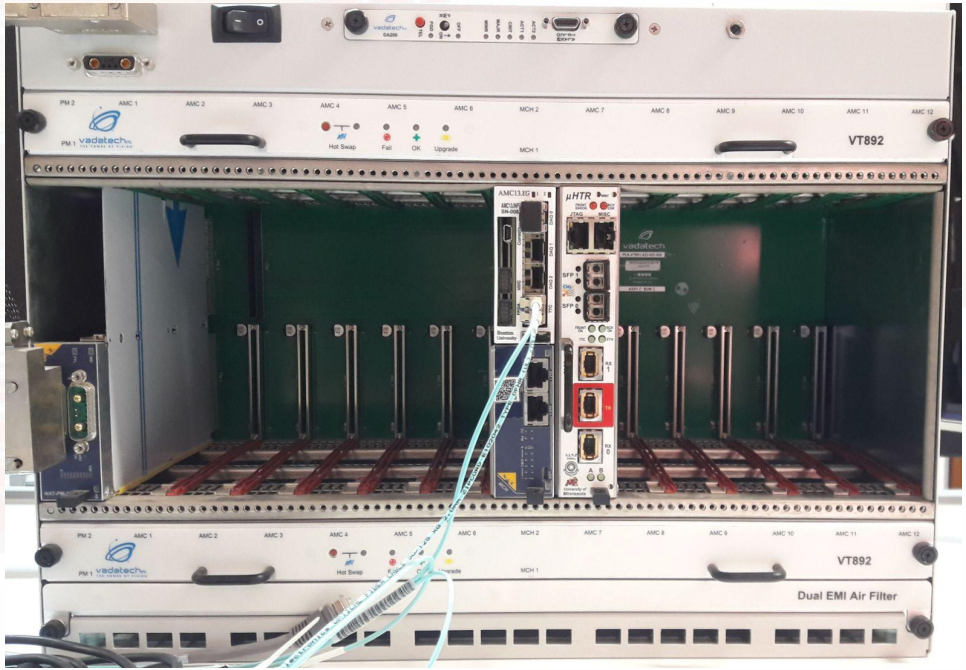


uTCA CRATE

Main Hardware modules

µTCA main KEY FEATURES

- High-speed µTCA connectors (12.5 GHz)
- Up to twelve AMCs: 12 full-size double-width
  - AMC 13 + MCH
  - µHTR

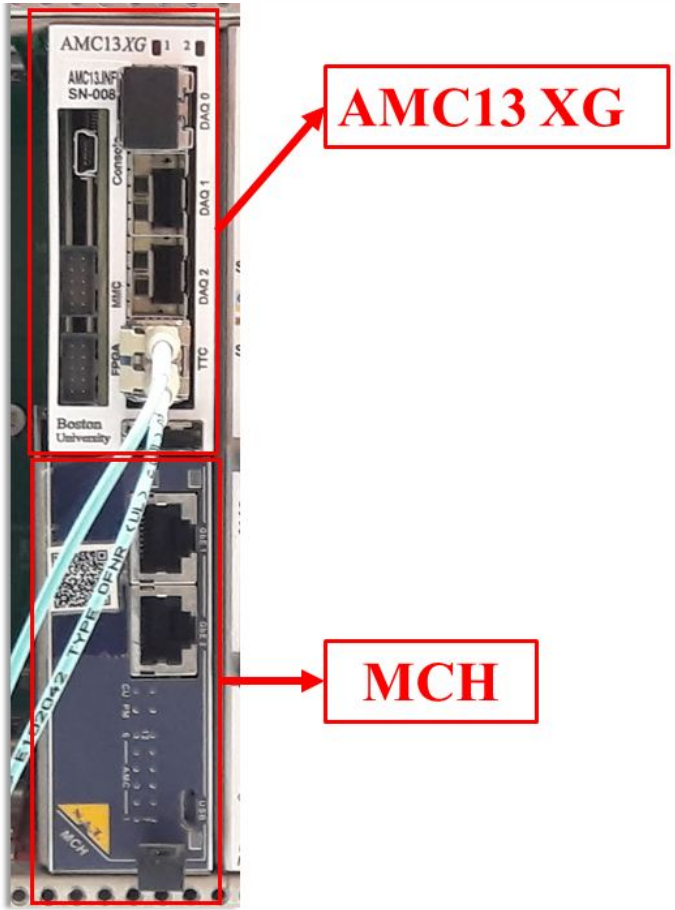


AMC13/MCH

Main Hardware modules

The AMC13XG: a new generation clock/timing/DAQ module for CMS µTCA

- Supports 10 gigabit optical fiber and backplane interfaces
- Implementation using Xilinx Kintex-7TM FPGAs
- µTCA MCH Ethernet switch
  - External applications can perform READ, WRITE, and RMW transactions on this bus by way of Internet Protocol (IP) packets



uHTR

Main Hardware modules

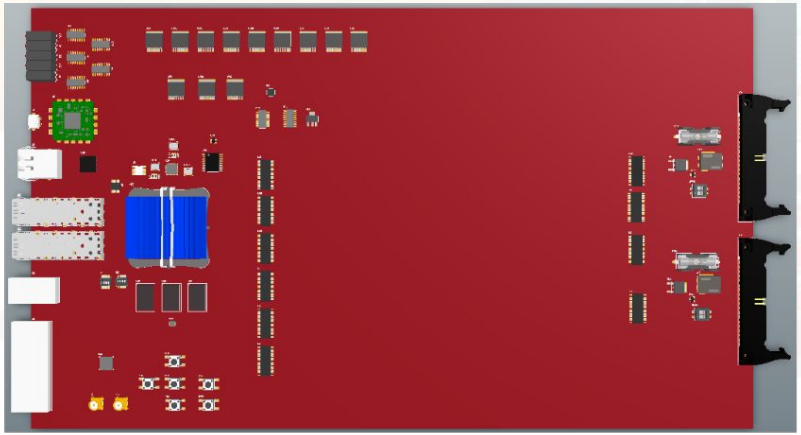
µTCA Trigger and Readout Module (uHTR)

- Front-end data links (1.6 Gbps and 4.8/5.0 Gbps)
- Data links which carry DAQ data from front FPGA to back FPGA (4 Gbps)
- DAQ data output format to AMC13/DTC
  - "QIE Reset" broadcast TTC/TCDS command

Kintex-7 EVB

Main Hardware modules

New Control Board Unavailable yet! Solution: Using Kit KC705 Evaluation Board

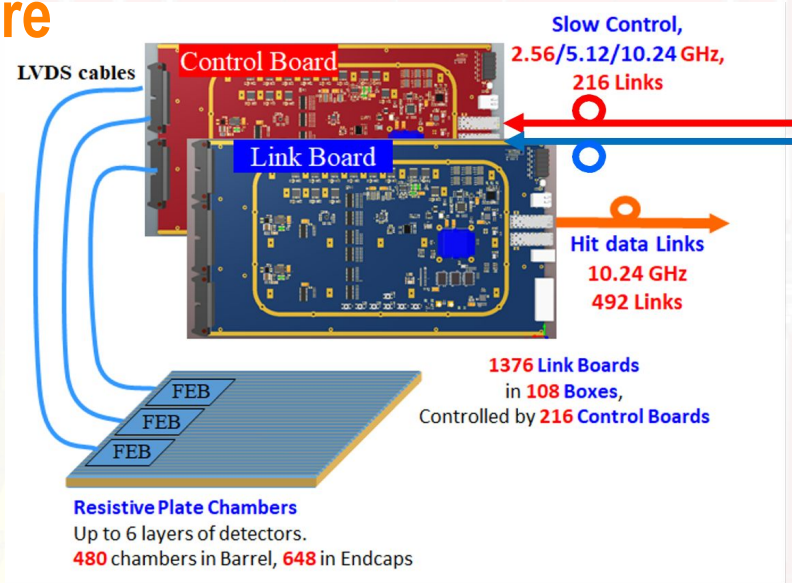


In process: New Control Board

Kit KC705 Emulate Control Board

Overview

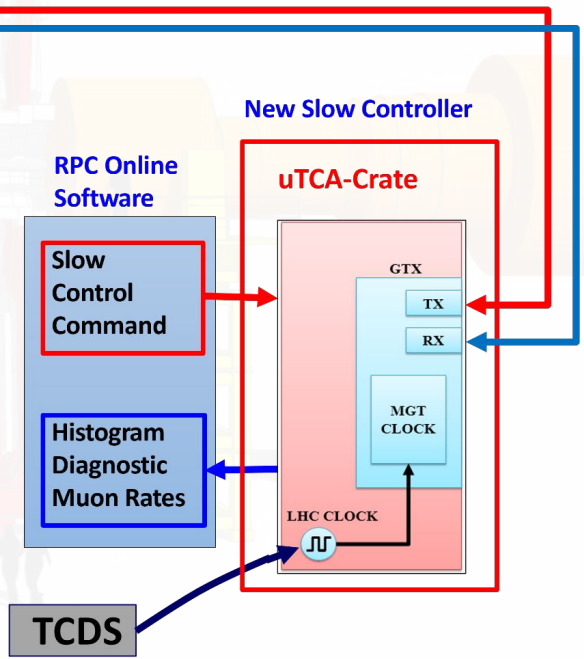
Now Setup Hardware



Solution CBPF

- Test individual modules
- Connectivity
- Hardware Integration

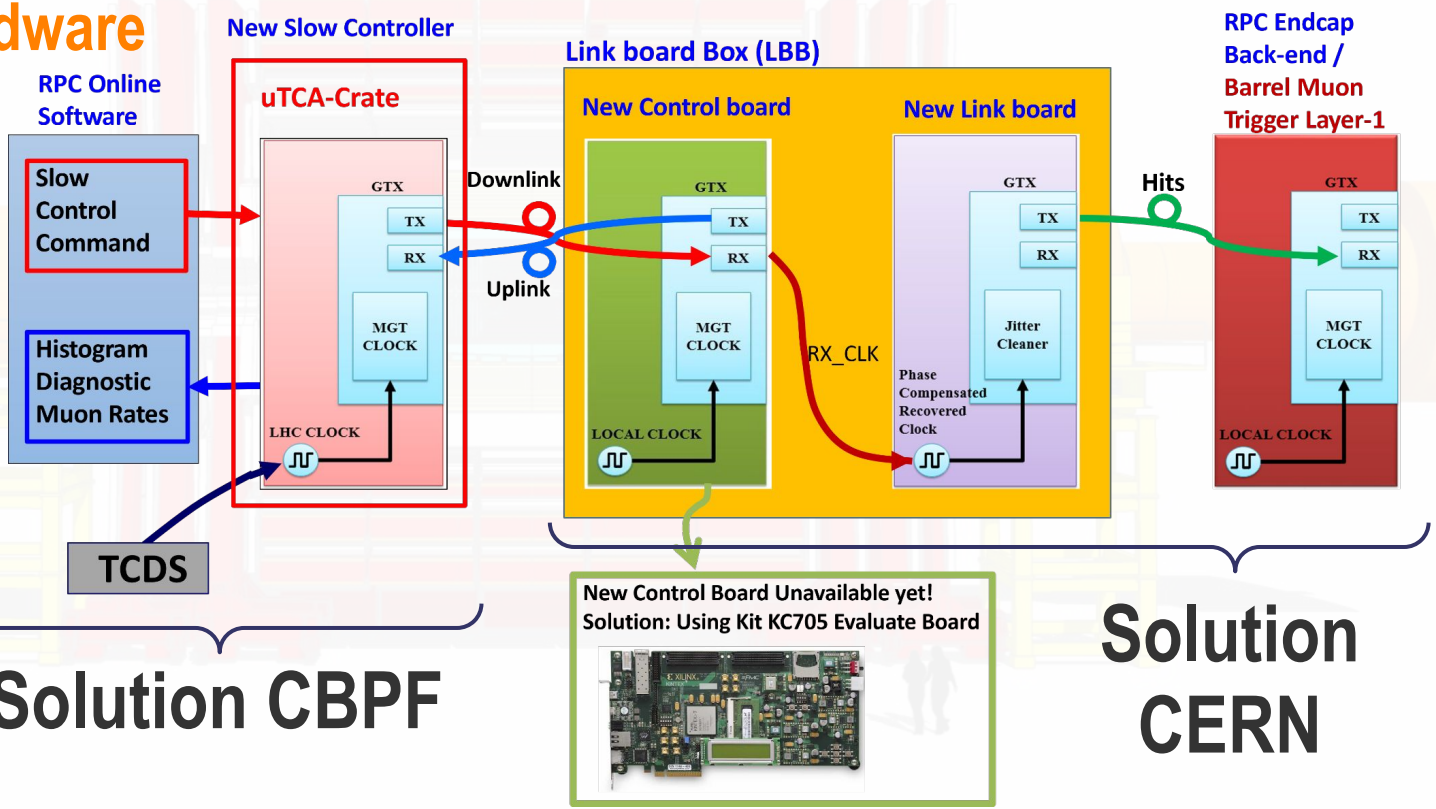
Final Goal in 2022/23



Overview

Final Setup Hardware

Final Goal in 2026



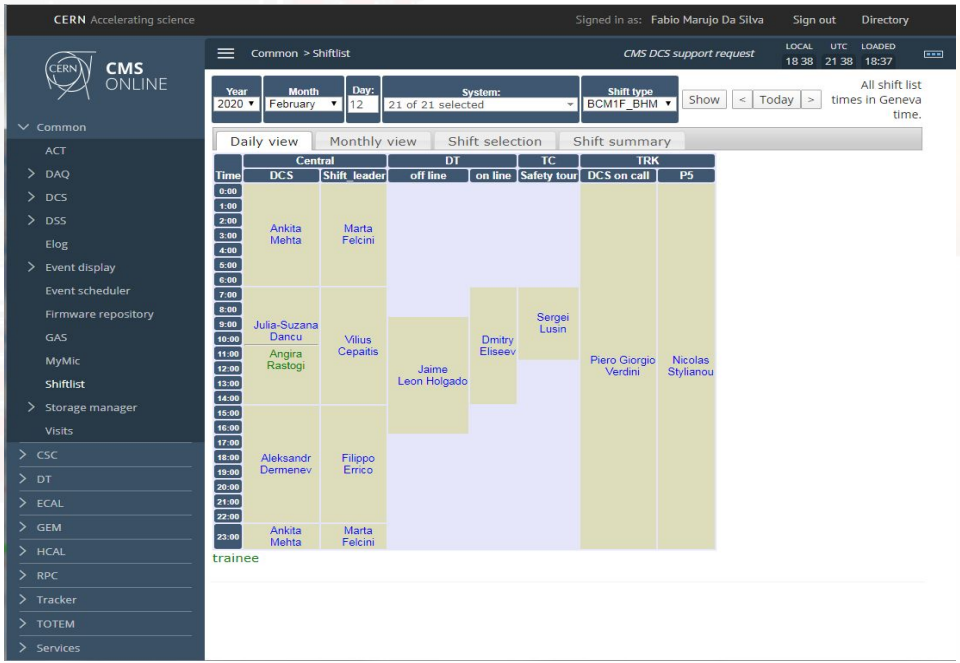
Overview

Expected Results in 2026

Slow Controller Operation-Online RPC (Back-End) software uses Slow Controller

By Online RPC

- ❑ FEB Threshold Setting
- ❑ TTC clock precision adjustment (LHC)
- ❑ windows configuration open/closed
- ❑ FPGA configuration file (remote programming)



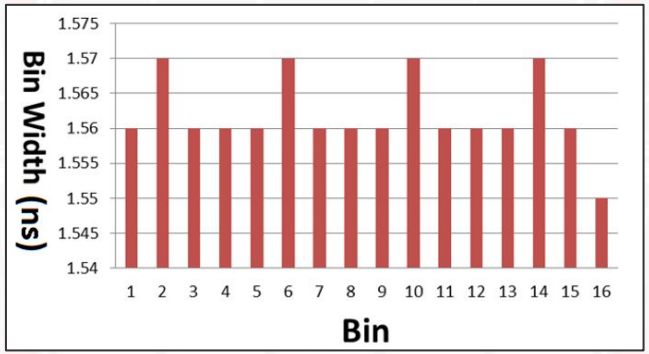
Overview

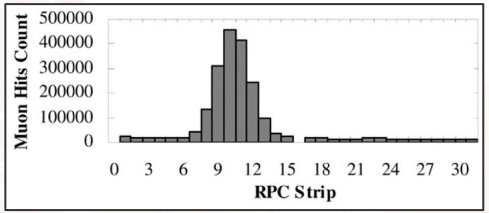
Expected Results in 2026

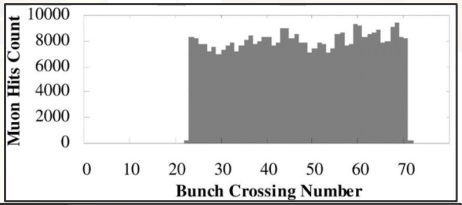
The ONLINE Software: Request/control services through Slow controller

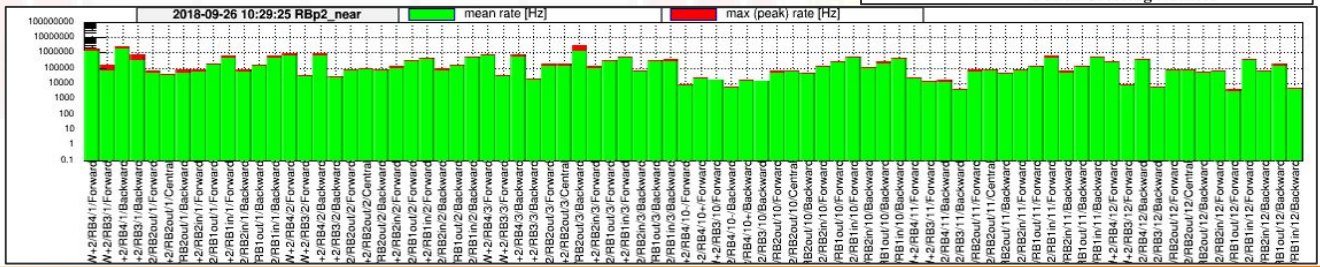
CMS Online RPC

- Slow Controller
  - Calibration mode
  - Link Board Parameter
  - Setting
  - Control Board
  - Parameter setting
  - Physics RUN
  - Standby
  - Histogram
  - Diagnostic
  - FEB Test









Back-Up