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Development of the Slow Controller of the RPC System Link for LS2 Update of the CMS/HL-LHC Experiment

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The upgrade phase II of the RPC Link system is ongoing to meet all requirements for the HL-LHC. Capability to work in a high radiation environment, improvement of timing resolution, and increasing the incoming rate capability of system and output bandwidth of system are the main goals of this project. In this project, the new RPC Back-End electronics which is a new scope in this era also will be responsible to receive the hits and sending them to the next Muon Track Finder Layers. Additionally, the new link system must be controlled by the new version of Slow Controller. The distribution of the TTC clock and fast trigger commands, setting the FEB's thresholds, reconfiguration of the Link system FPGAs, and reading the Link system Status are the main functionalities of the new Slow Controller. It should be notice that the new Slow Controller will be controlled by the RPC online software. In this project, we are going to define all necessary functions of the new Slow Controller in more detail. All of these functions will be implemented into the FPGA. In the first step, we will study all necessary functions requested by the new Link system. Then, these functions are translated to the corresponding firmware and implemented into the FPGA and equipment for high-speed data communications. In parallel, the necessary software routines will be developed on the RPC online software. Finally, the proper functionality of the control and communication chain will be surveyed.

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