Interfaces of Power and Beam Interlock Controller to other systems

- Cables between systems needed to be defined … if not yet one, this is urgent!
  - What type of cable, how many pins?
  - From where to where?
- To define cable types, one must define what signals are exchanged
- In these days limited budget needs to be considered (economic solutions)
- For the PIC (Powering Interlock Controller), time for a signal to be exchanged is not critical (some ms) => **current loops**
- For the BIC (Beam Interlock Controller), time for some of the signals to be exchanged is very critical (less than 0.1 ms) => **frequency signal**

Interfaces of Powering Interlock Controller to Power Converter and Quench Protection System

- Cables have been defined – the exchange signal has been defined
  - See presentation in MPWG and minutes of meetings on the WEB
  - Some details still to be discussed

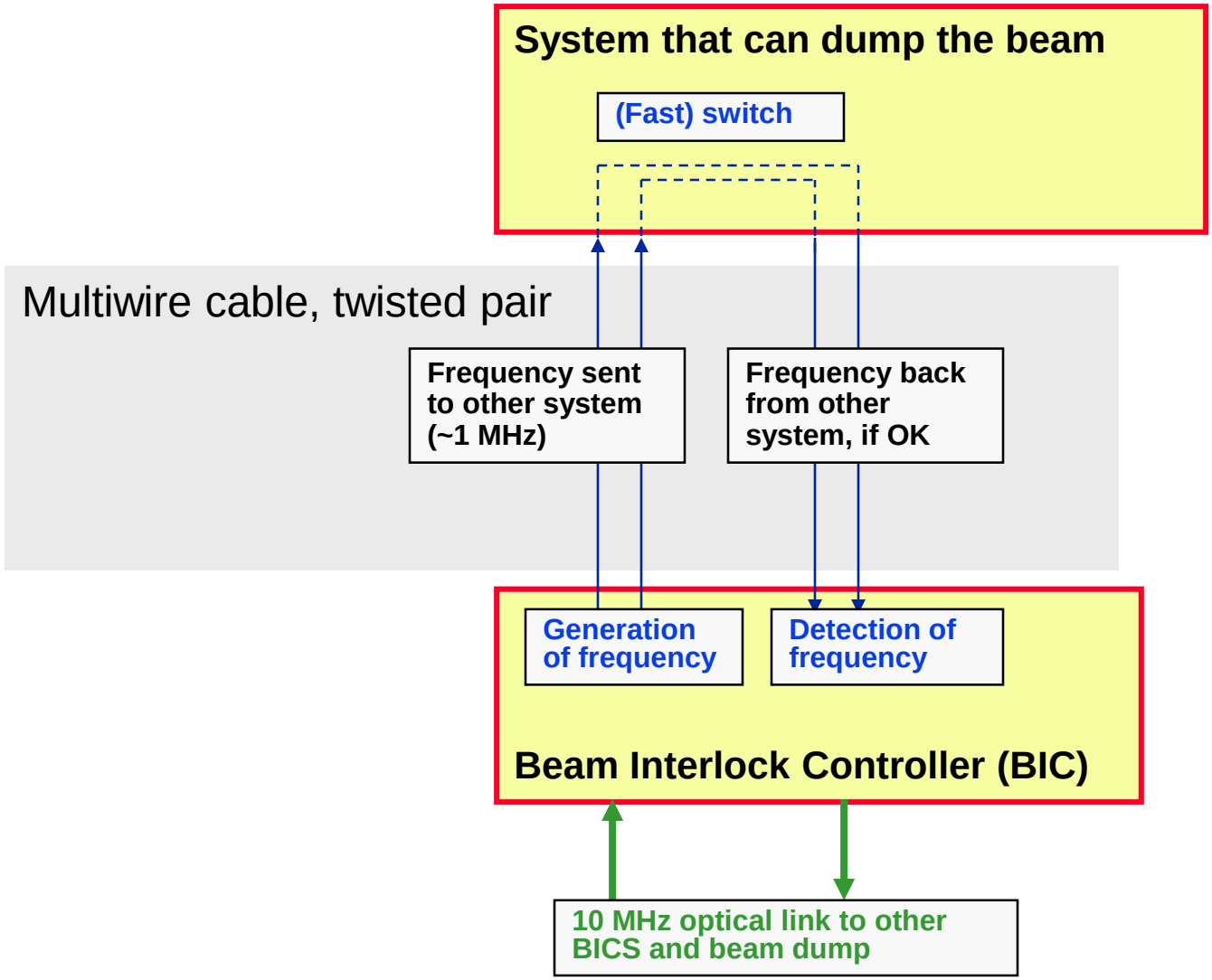
- The number and the position of the cables is know (EXCEL lists for all electrical circuits – collaboration between interlock team, and QPS / PC teams)

- About 30-35 km of cables will be required

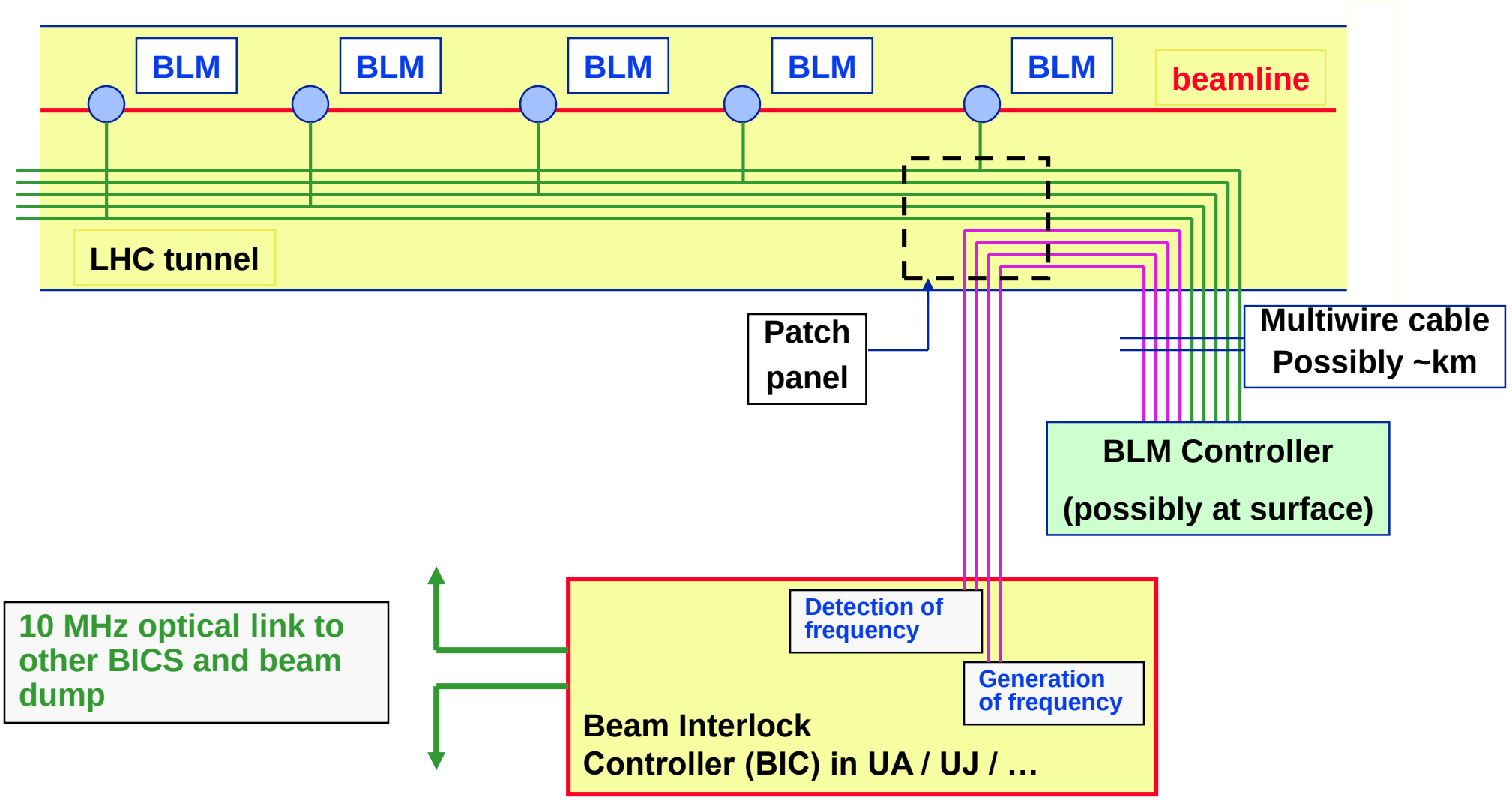
Interfaces of Beam Interlock Controller to other systems

- Cables are being defined – signal exchange has been discussed with some users of the BIC, but not finalised
- The Beam Interlock System **interfaces with many systems**, therefore **ONE type of signal exchange** is proposed
  - Interface PIC to PIC ok - done in the same team
  - Interface to BLMs discussed, to be finalised
  - Interface to interlocks for resistive magnets discussed, to be finalised
- Requirements for the exchange of signals
  - For some systems (for example BLM) - the beam dump signal must be fast
  - In general, one beam dump signal for both beams, but in some cases, one beam dump signal for each beam (vacuum)

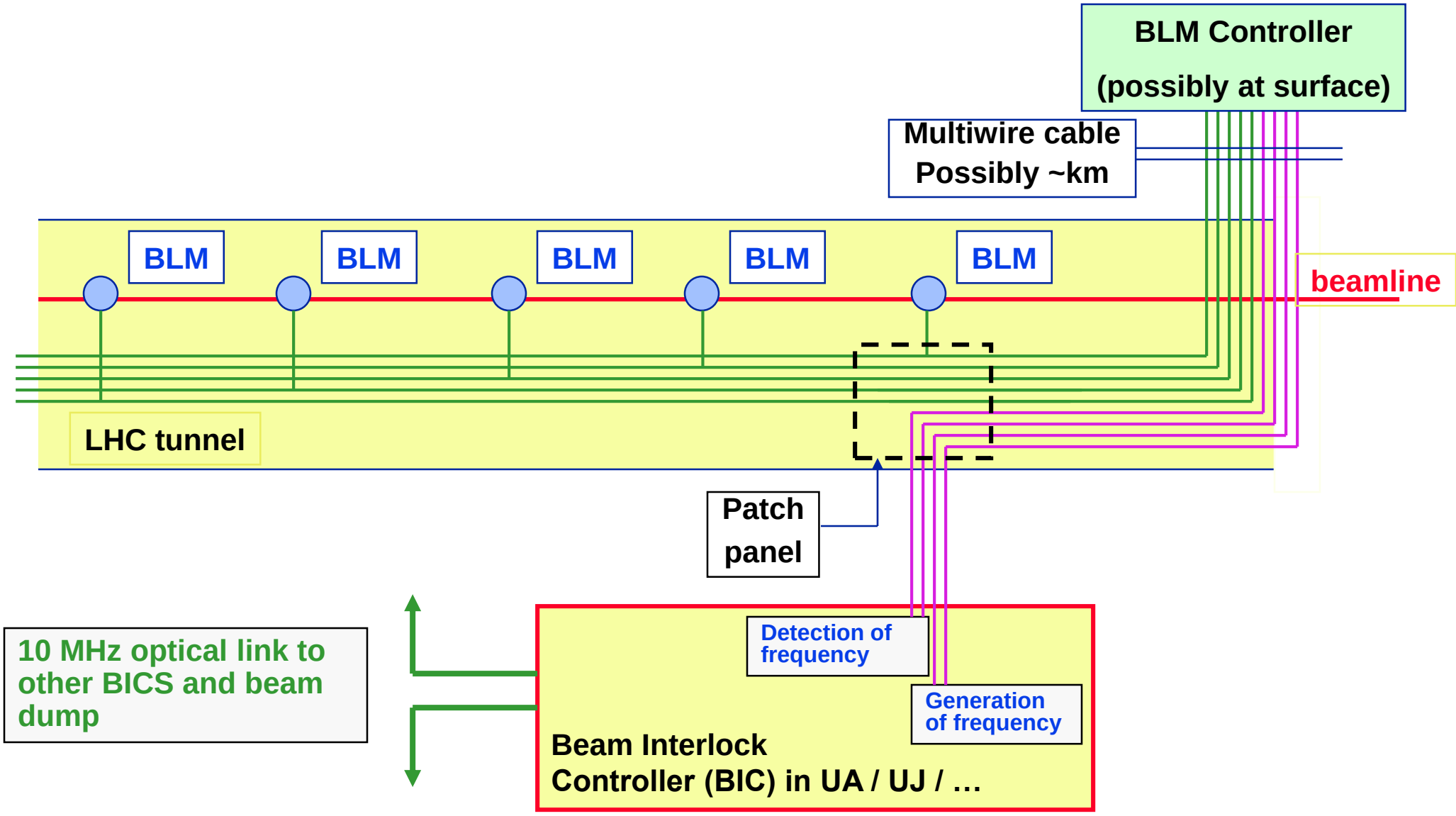
Interfaces of Beam Interlock Controller to other systems



Interfaces of Beam Interlock Controller to Beam Loss Monitors (preliminary)



Interfaces of Beam Interlock Controller to Beam Loss Monitors (preliminary)



Interfaces between interlock for resistive magnets and Beam Interlock Controller (preliminary)