Machine Protection Working Group

Minutes of the 15th meeting held on September 20th 2002

Present: J-C. Billy, F. Balda, E. Carlier, E. Cennini, P. Charrue, E. Ciappala, C. Dehavay, B. Dehning, B. Jeanneret, R. Lauckner, F. Locci, D. Macina, V. Montabonnet, R. Schmidt, F. Szoncso, J. Wenninger, M. Zeara Sanz, M. Zerlauth

Excused : B. Puccio, R. Giachino

Main topics of this meeting:

- Status of the SPS Hardware Interlock System (J. Wenninger)
- Evaluation of a Fast PLC Module for the Beam Interlock System (M. Zaera Sanz)
- AOB (R. Schmidt)

Status of the SPS Hardware Interlock System (J. Wenninger)

J. Wenninger presented the status of the new hardware interlock system for the SPS. The new system is subdivided into a beam dump and into an extraction interlock system for the beam extractions in LSS2, LSS4 and LSS6 (LSS = Long Straight Section). One important requirement is that the interlock system must be compatible with fast cycle changes in the SPS. This requirement implies that the interlock logic must adapt automatically to the new beam conditions and that the machine timing must be handled by the interlock clients and by the extraction interlock system.

The present design is based on two different interlock modules, the SPS Local Interlock Controller (SLIC) and the SPS Central Interlock Controller (SCIC). The SLIC module is essentially identical to the future LHC Beam Interlock Controller. It applies a fixed interlock logic and generates an output signal and/or acts on a beam interlock loop. Monitoring of the input and output signals must be provided, but this information is not safety critical. It is always possible to stop the beams by a software interlock system whenever the communication with a module is lost.

The SCIC module is basically identical to the SLIC except that its interlock logic must switch according to the beam type. Machine timing events are used to trigger a change of the interlock conditions. Three SCIC modules are required to manage the extractions in LSS2, LSS4 and LSS6. Each module must provide an enable signal to the extraction kickers and a dump trigger whenever the extraction enable is not given or disappears during the extraction process. This feature is required for the slow extractions (with beam extracted over ~ 6 seconds) and in case of a bad kicker pulse.

For each extraction a number of SLIC modules will concentrate the input interlock signals, each SLIC being assigned to a zone corresponding to certain parts of the lines or

to logically grouped equipment systems. The outputs of the SLIC modules serve as inputs to a SCIC module that enables the extraction in the absence of interlocks. For the SPS beam dump, the layout is conceptually identical to the LHC layout: a beam interlock loop connects SLIC modules installed in each of the 6 SPS access points (BA1 to BA6) to the SPS beam dump and to the SPS injection kicker.

The present interface between the SPS beam dump and the clients is based on a current loop. For the new system, a decision must be taken on the interface type, i.e. frequency signal or current loop. The same interface should be used for the SPS and the LHC.

The SPS timing system is presently unable to distinguish between different beam types. This information must be provided in the future together with the length of the cycle and the unique cycle identification.

The surveillance of the power converters in the transfer lines (including septa magnets) is a critical client of the interlock system. Since for the moment no surveillance is provided, a new system must be developed for the extraction lines. The currents of critical power converters must be checked against reference values (within a given tolerance) just before the extraction time (over an interval of 20 to 100 ms). The reference currents must be stored independently of the current references for the power converters in order to maximize the reliability.

The next milestones for the interlock system are the extraction tests in 2003 and 2004. If by that time the system is not operational, it will not be possible to extract high intensity beams, but this will not be a serious limitation, at least for 2003. A request for manpower has been made to the AB/CO group to build the system which should also provide useful experience for the LHC.

Evaluation of a Fast PLC Module for the Beam Interlock System (M. Zaera Sanz)

M. Zaera Sanz presented test results for a fast PLC module that is a potential candidate for the heart of the Beam Interlock System Controller. The full details of this work will be published in the near future in the form of an LHC note. The BIC module must be fast and reliable, and different candidate implementations exist, for example C-PCI, VME or PLC. An implementation based on PLCs has many advantages, but the slowness of the PLC poses a problem. This speed issue can be solved with a high speed boolean processor (FM352-5). This processor provides fast and independent control within a larger PLC control system. The module scan cycle is 1 μs and it provides 15 digital inputs and 8 digital outputs. The response time of 3-4 μs is independent of the number of inputs to an AND or OR gate and of the program size. The response times for output activation and deactivation are 3, respectively 6 μs. Those numbers are consistent with the module specifications. It is possible to control a process with a granularity of 6 μs for a single module and of 12 μs in a chained configuration.

A continuous monitoring of all input signals must also be provided for a BIC, and every state change must be recorded and time stamped. There are several solutions for the absolute time stamping. The time intervals between state changes could be determined with a precision of up to 2.5 μs.

M. Zaera Sanz concluded that the Fm352-5 module is a promising control and monitoring device for the BIC. The price of the FM module is ~ 600 Euro.

During the discussion**, E. Cennini** asked if there was any watchdog to verify the functioning of the boolean processor. **M. Zaera Sanz** replied that a build-in self-diagnostics interrupts the CPU in case of problems or errors, in which case the output signal are set to a safe state. It is however not clear that this can be guaranteed for all failure scenarios. **E. Carlier** wondered if it is possible to read back the program that is executed, and it seems that it is possible to quickly read back an identifier of the program that is being executed, or even read the entire program to check it. **E. Ciapala** said that the RF group is developing a hardwired interlock logic for the LHC RF system, with software for monitoring. This system will be presented in a future meeting. **R. Lauckner** remarked that the possibility to re-program the logic could be a step towards less safety.

AOB

R. Schmidt presented the list of presentations that have been given on machine protection in various committees, in particular at the LCC. He also gave the status on the discussions with SL/PO about the energy tracking. Essentially the SL/PO group proposes to modify slightly the design of their PC boards in order to provide a digital or analogue signal derived from the DCCT. SL/PO suggest that SL/BT takes the responsibility to build the energy meter (to convert the current to an energy) and the module to compare energies. As a next step, a functional specification should be produced for the energy meter. **Action :** **E. Carlier**, **R. Schmidt**, **J. Wenninger** and a representative from SL/PO should prepare the specifications for the energy meter.