SPS Hardware Interlocks

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- Design Status.
- Interlock client & timing issues.
- LHC extraction tests 2003 & 2004.

Scope

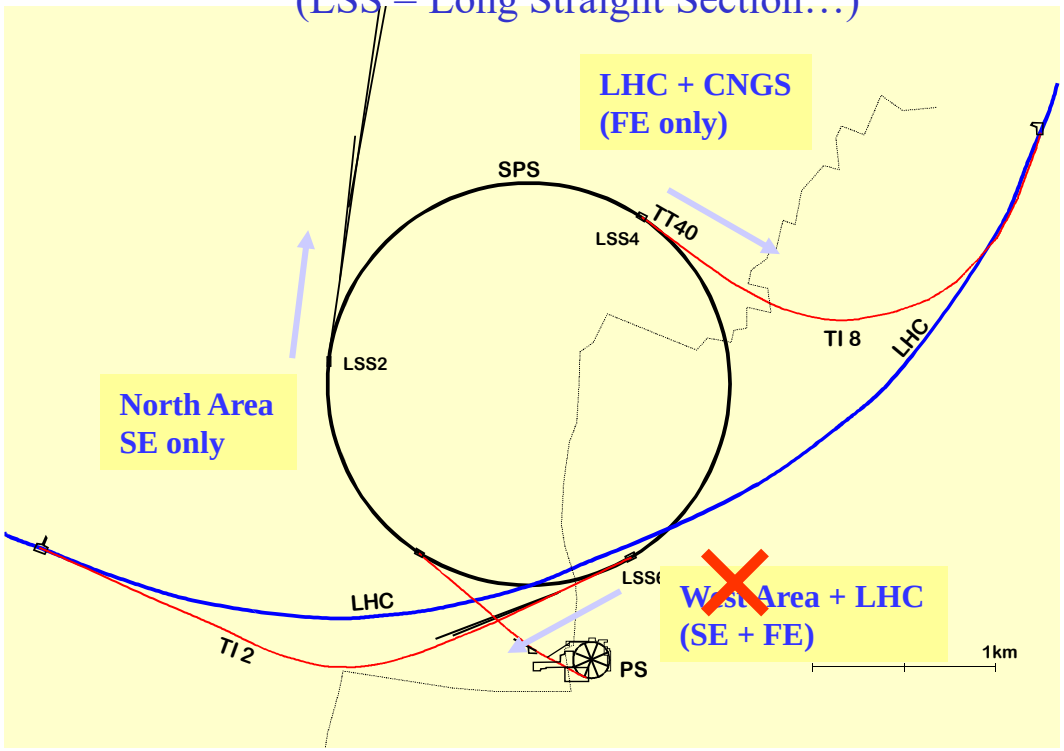
The SPS interlock system includes the following components :

- The SPS emergency beam dump system, with a functionality similar to the LHC beam interlock system.
- The SPS extraction interlocks for LSS2, LSS4 and LSS6.

(LSS = Long Straight Section…)

Boundary condition :

The system must handle fast cycle changes, i.e. must adapt to cycle changes WITHOUT operator intervention.



Multi-cycling / I

Multi-cycling in the SPS implies that :

- The machine should switch between different beam types (fixed target, LHC, CNGS…) from one cycle to the next (cycle length ~ 15 to 40 seconds).
- Such a scheme only works if all components and equipments are able to switch their settings, working points.... without operator intervention.

→ applies also to the interlock system !

Multi-cycling / II

The information on which cycle should be played is transmitted by the timing system, implying that machine timing must be handled by :

- The interlock clients for interlock generation (power converter, instrumentation, kickers…).
- The extraction interlock system itself to apply the correct conditions.

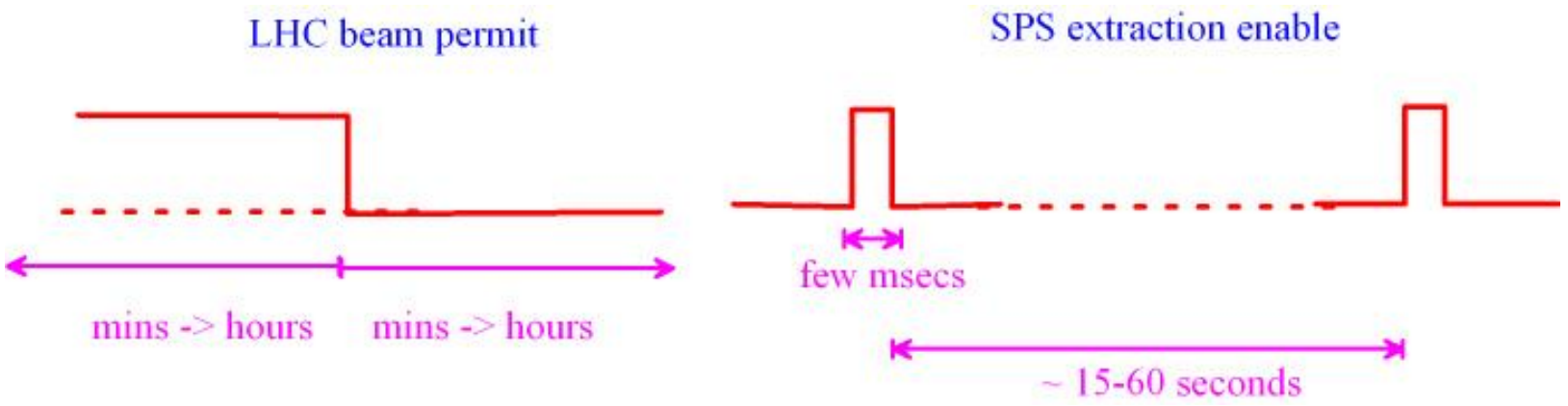
- Beam dump interlock system : we try to maintain it independent of timing.
  → the clients "continue" to handle ALL the timing.

We need fail-safe handling of machine timing inside many systems.

SPS versus LHC

Some differences between SPS and LHC beam interlocks :

- The machine timing must be used in the SPS to determine which interlocks have to be applied.
- The short SPS cycle → more tricky to monitor & diagnose.



- Time-stamping of events :
  - LHC : can use any reference time (UTC…).
  - SPS : we are mainly interested in the time in the cycle & the cycle #.

Conceptual Design

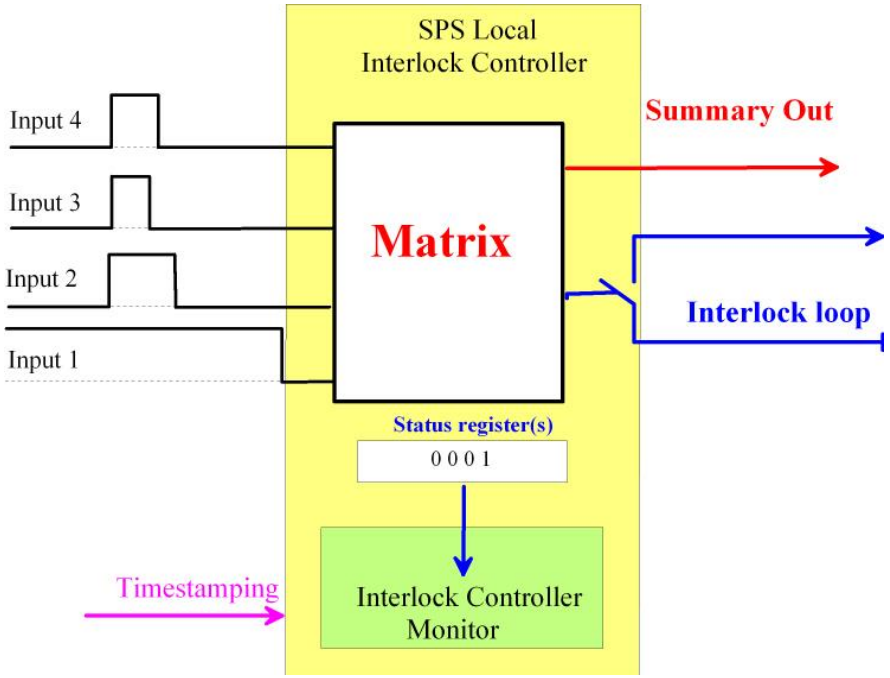
We are trying to design a system that should be as similar to the LHC as possible… Presently we have in mind a system based on 2 modules :

- The SPS Local Interlock Controller – SLIC
  - Interlock logic is independent of the machine timing.
  - Controls interlocks that are logically linked together (to the same beam(s)), for example all extraction elements of a given LSS, the CNGS transfer line, the LHC TI8 transfer line,…

- The SPS Central Interlock Controller - SCIC
  - Manages the output signals of a number of SLICs.
  - Provides the main interlock signal for each extraction.
  - Handles machine timing to take decisions.

SPS Local Interlock Controller

- Applies a FIXED interlock logic/matrix to its inputs.
- Generates an output signal or closes/opens an interlock loop.
- The monitoring of inputs and outputs requires a connection to the machine timing / time reference. Not safety critical – only diagnostics !



This module is ~ identical to the FUTURE LHC Beam Interlock Controller !

SPS Central Interlock Controller

The basic functionality of the SCIC is similar to the SLIC, except :

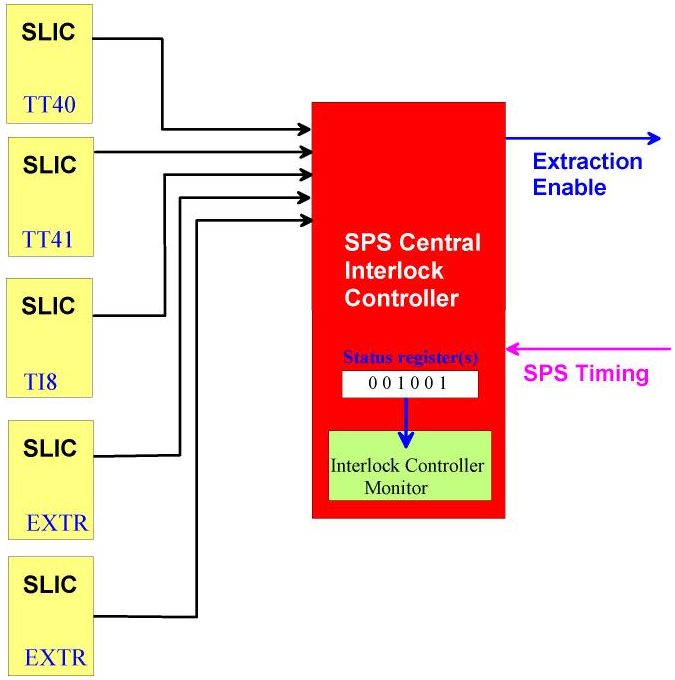
- The interlock logic depends on the SPS cycle.
- We use one controller for each of the 3 extractions in LSS2/4/6, even if only LSS4 requires the full functionality.
- It must provide :
  - An enable signal for the extraction kickers.
  - A beam dump trigger if no extraction enable is given or extraction enable “disappears” (slow extractions, kicker misfiring).

SPS Extraction Interlock Layout

Schematic layout of the interlock system for an extraction point (here LSS4) :

- A number of SLIC modules are assigned to interlock zones and "concentrate" interlock signals that can be grouped logically.
- One SCIC :
  - Receives all summary signals and applies the cycle dependent logic.
  - Generates the extraction enable signal.

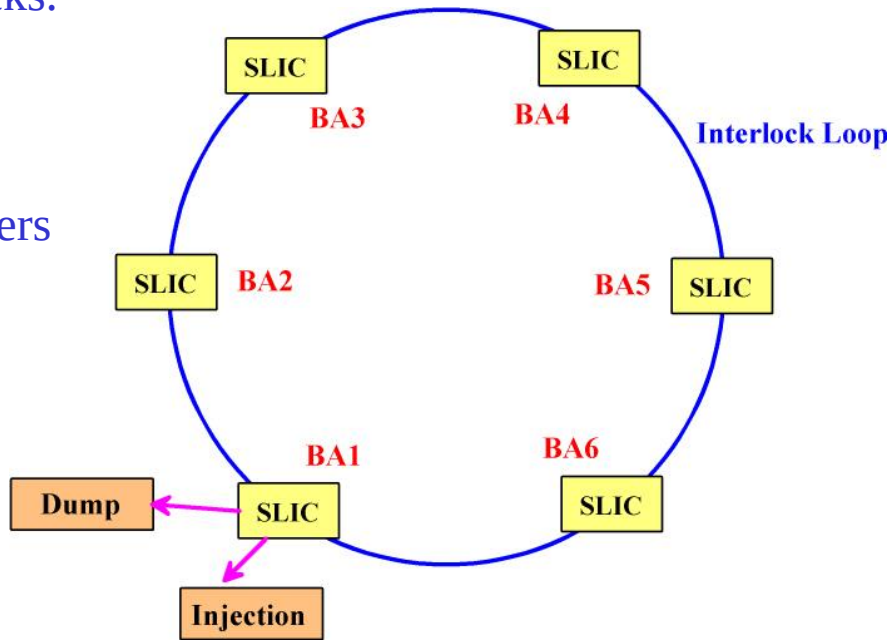
Automatically ignores any interlock that is irrelevant for the beam in the machine.



SPS Beam Interlock System

The layout of the future SPS emergency beam dump system would be identical to the LHC layout :

- One or two SLIC modules are installed in each BA to collect all local interlocks. signals and apply an interlock matrix.
- The SLICs are linked together by an interlock loop.
- An interrupt of the interlock loop triggers a beam dump.



Interface to the clients

The interface to the clients must be defined :

- Present SPS emergency dump :
  - Current loop (source provided by the client).
- LHC beam interlock :
  - Frequency signal (1 – 10 MHz) or current loop. To be decided !
  - Interlock system provides the source & detection, client establishes contact.

To use the same interface for the SPS,
we must make a decision here soon !

Timing System

The present SPS machine timing :

- Does not provide any identification of the beam type.
- Uses identical timing signals for all cycles (FT, LHC, lead…).

Additional information must be provided in the future :

- Information on the beam type :
  - LHC, CNGS, FT, Lead…
  - Dense, pilot ? ⇔ philosophy of "interlock relaxing" for low intensity.
- Cycle length.
- Unique cycle identification.

Power Converter Surveillance / I

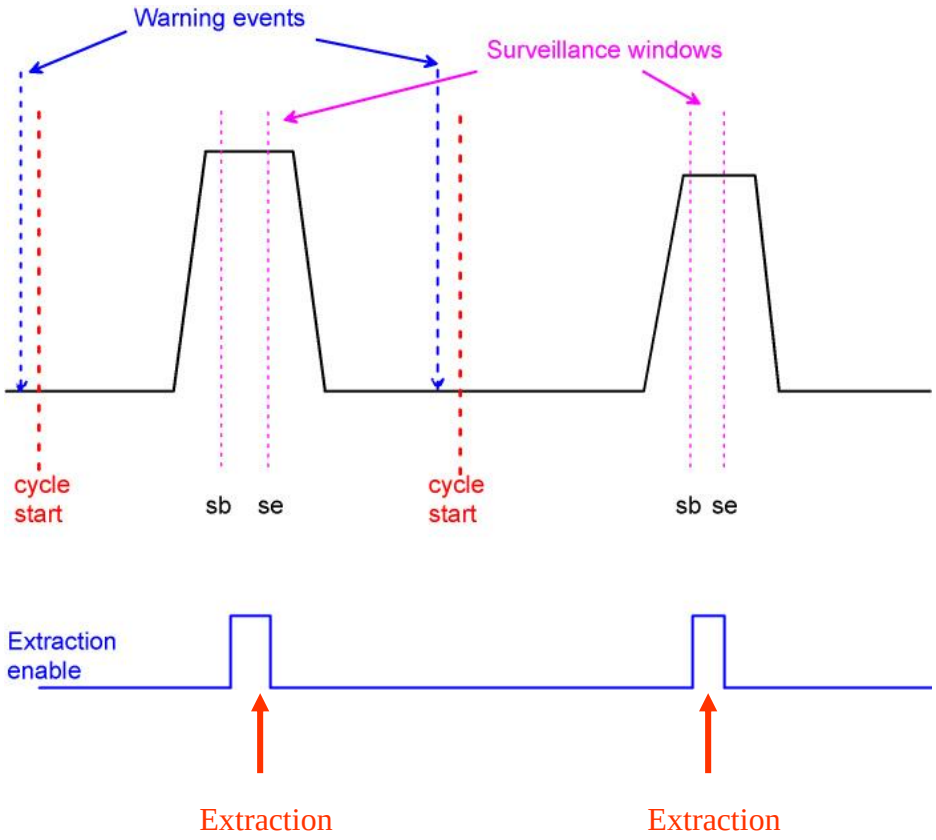
- In the SPS there is presently no hardware surveillance of PC currents.
- For the fast extractions, we must provide a fast power converter surveillance (the slow extractions will also profit from it !).
- For the LHC extractions, surveillance will be required for :
  - Extraction bumpers (tolerance 0.2%)
  - Septa (0.4%)
  - Transfer line elements :
    - Main elements : tight surveillance (0.1% to 1%).
    - Steering elements : loose surveillance, need room for steering.

A very critical interlock client !

Power Converter Surveillance / II

Proposed surveillance scheme, tailored to the extractions :

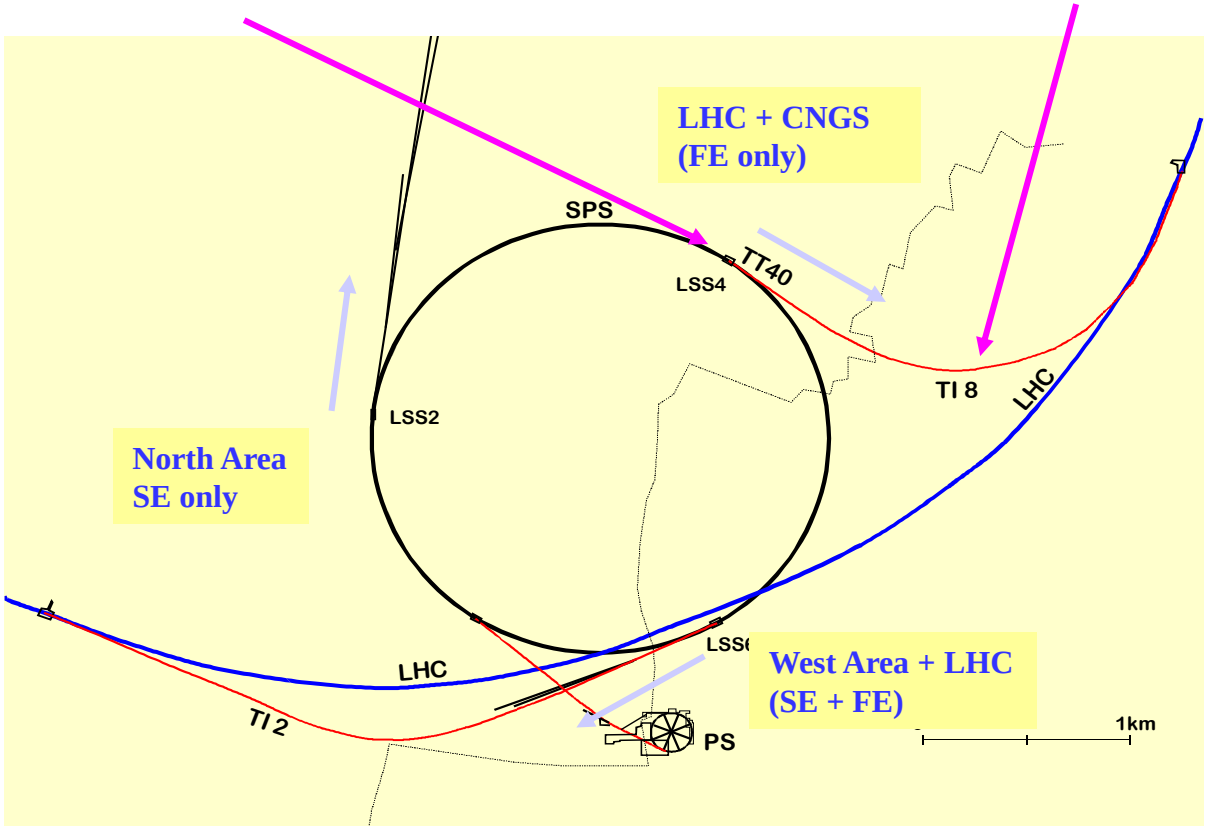
- The currents are checked within a defined window against a reference VALUE (with a certain tolerance).
- Reference value and tolerance :
  - Depend on cycle/beam type.
  - Are loaded independently of the usual functions.



LHC Extraction Tests /I

Fall 2003 : test of the TT40 line & extraction channel.

2004 : test of the full TI8 line down to the LHC ring.



LHC Extraction Tests / II

The tests will use LHC beams in dedicated MDs :

- A SLIC (proto-type) module is required & sufficient – no multi-cycling !
- Interface must be selected and available for clients.
- The interlock clients must be ready ..

If we are not ready for the test(s) :

- we must limit the beam intensity (below damage threshold)

  ~ Ok for most components tests.
- we loose precious time to gain experience (even for the LHC).

Summary

- In the past year we have advanced the design of the SPS system – we should be ready by the end of the year with a complete specification.

- We have asked for manpower from AB/CO to evaluate possible solutions (VME, PLC…), build prototypes… Waiting for decisions…

- We must test and decide soon on the interface between interlock clients and interlock system.