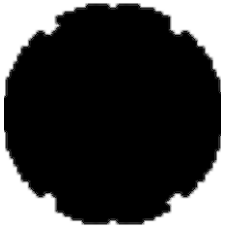

EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH
European Laboratory for Particle Physics

Large Hadron Collider Project

EVALUATION OF A HIGH SPEED BOOLEAN PROCESSOR PLC MODULE IN PROSPECT OF THE LHC BEAM INTERLOCK SYSTEM

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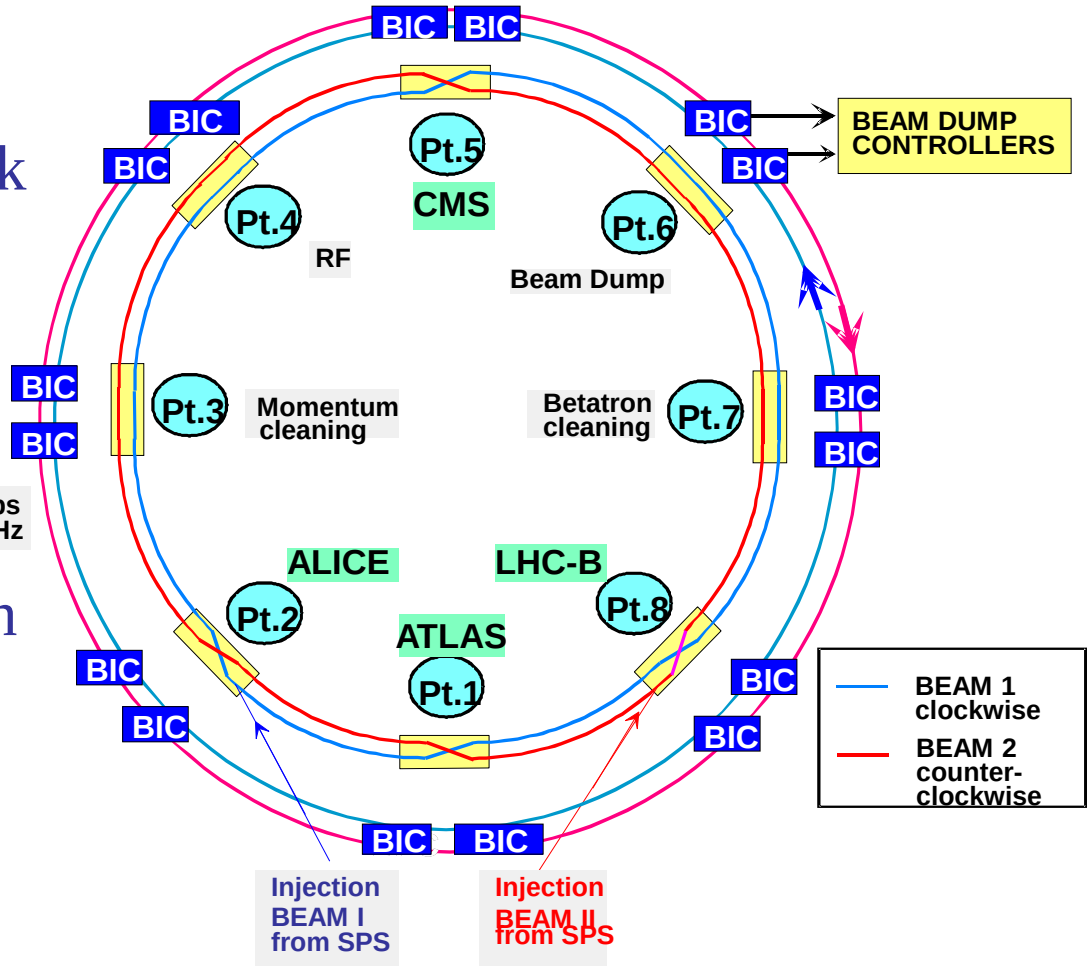
Outline

- Introduction to the LHC Beam Interlock System
- BIC Implementation Solutions
- An Overview of the FM 352-5 module
- Programming and Operating the FM 352-5
- Control: Program and Response Time Analysis
- Monitoring: Requirements and Programming
- Conclusions and Further work

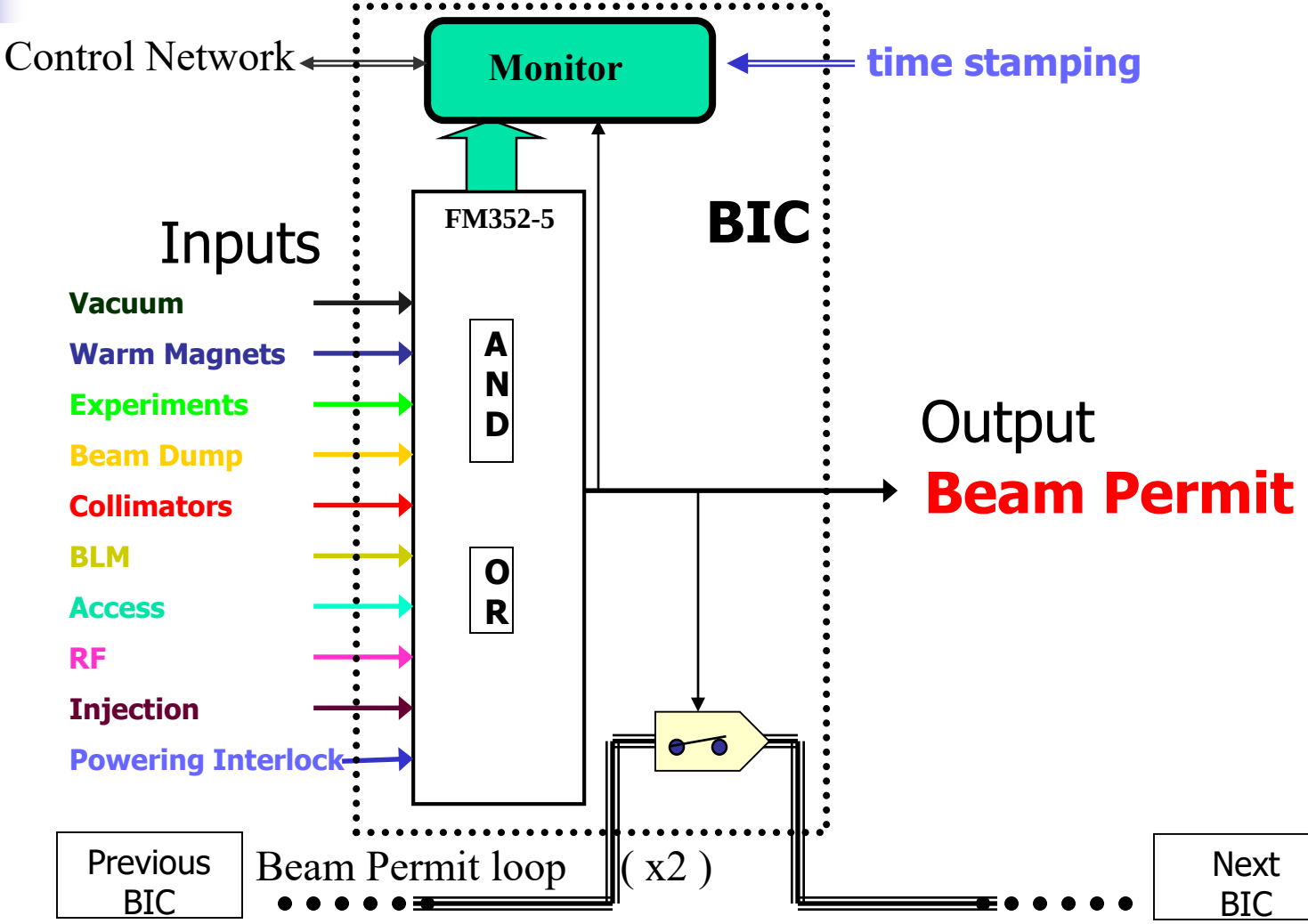
Layout of the LHC Beam Interlock System

- 16 **B**eam **I**nterlock **C**ontrollers
- 2 fast links

  Beam Interlock Loops optical fiber at 10 MHz
- if one loop broken ⇒ Beam Dump

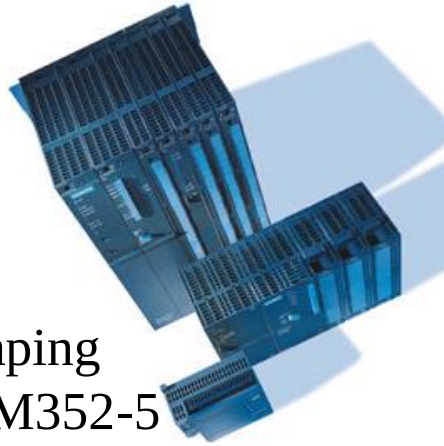


Beam Interlock Controller



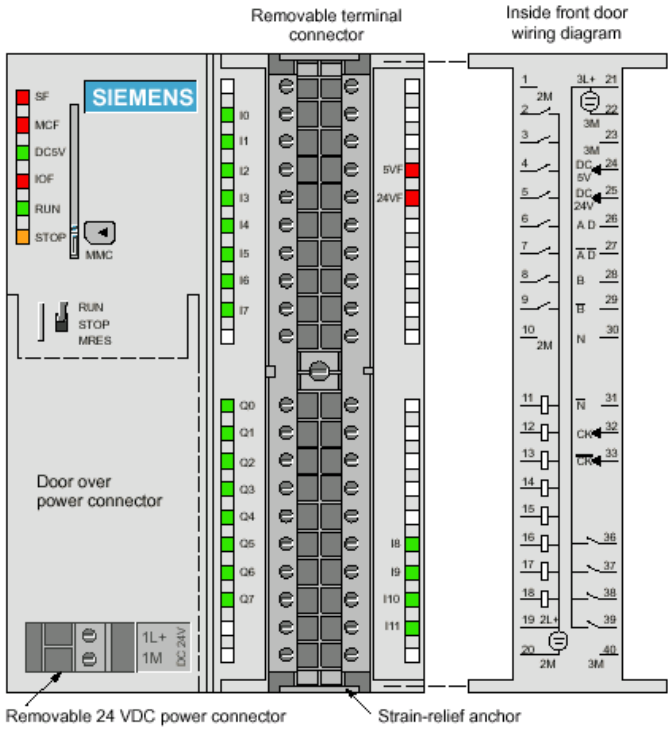
BIC Implementation Solutions

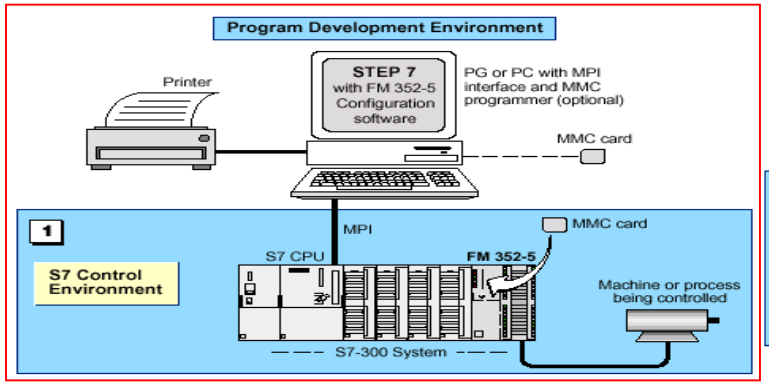
- BIC features: Fast (order of µs), reliable, embedded in host system (all in one), and fast link to carry the Beam Permit information.
- Several Possible BIC implementations:
  - C-PCI
  - VME
  - PLC
- PLC (Programmable Logic Controller):
  - Modular Design: Power Source, CPU, DI/O, Ethernet, Profibus, etc…
  - Easily scalable and programmable
  - Robustness and Reliability
  - "Cheap" faced to other solutions as VME
  - Main Problem: Slow (Scan cycle 150ms)
    - Control: Millisecond response time
    - Monitoring: Millisecond granularity for time stamping
  - Solution: Use of the High Speed Boolean Processor FM352-5

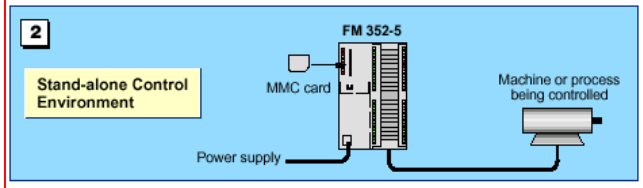


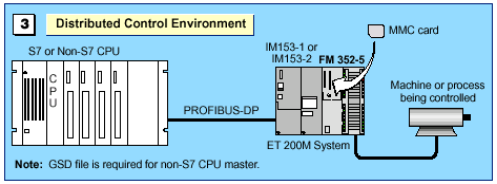
An Overview of the FM352-5 module

- High-speed Boolean processor that provides Independent control and extremely Fast control of a process within a larger control system.
- Scan Cycle = 1 µs.
- Up to 15 Digital Inputs: 12 of 24 VDC and 3 differential 5 VDC.
- Up to 8 Digital Outputs.
- Three Different Configurations:



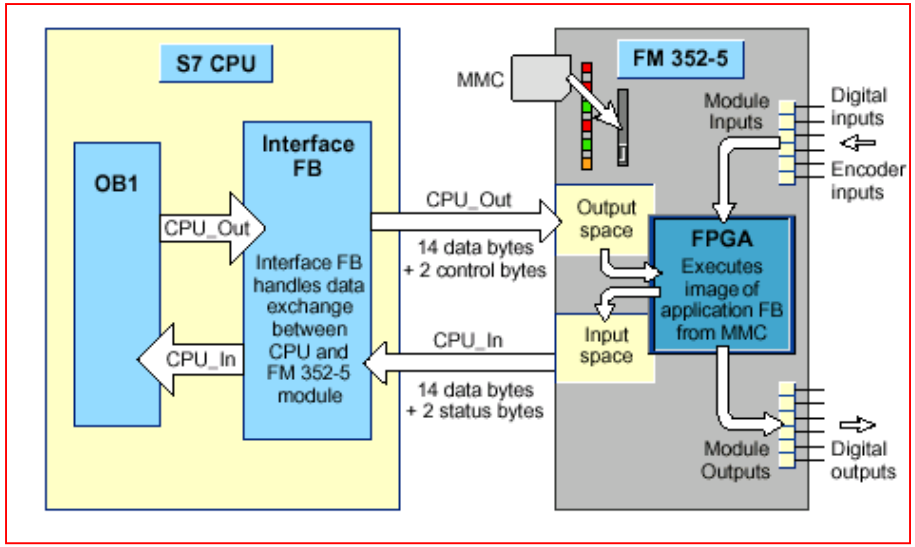






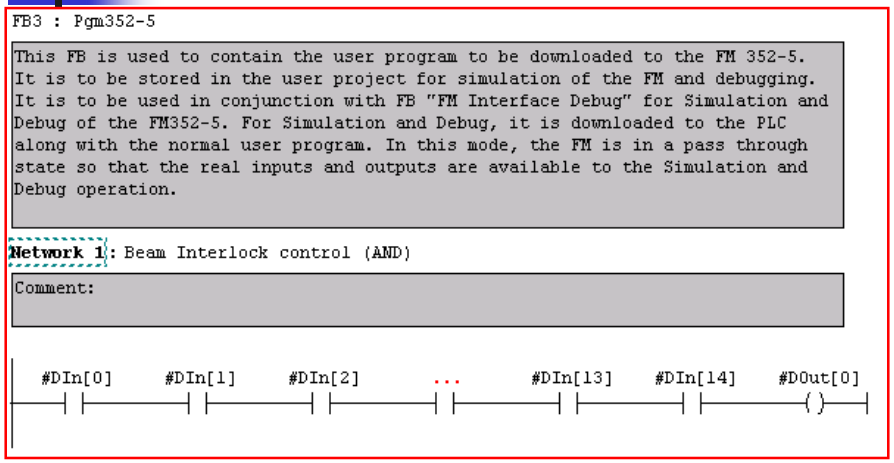
Programming and Operating

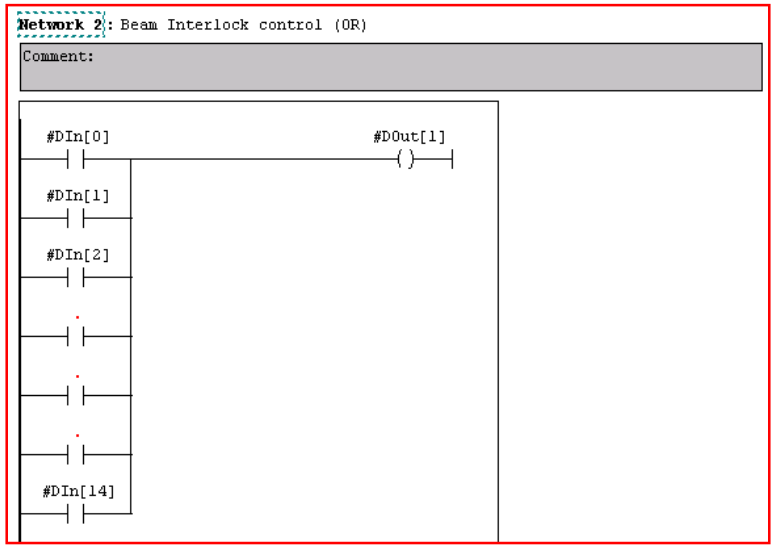
- Standard Siemens Programming environment known as STEP7
- Communication with the CPU (Input/Output) via 14 bytes pipe



- Reduced Set of Programming Primitives: Flip-Flops, Binary Logic, Timers, MPX, Counters, Shift Registers, Adders, Multipliers and Dividers
- Parallel execution of Programs using a Multi-phase Clocking

Control: Program and Response Time Analysis





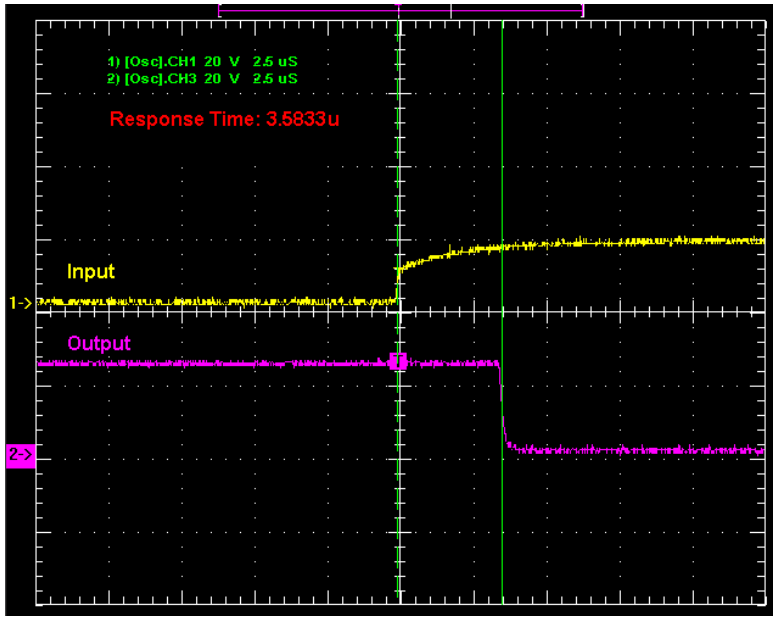
#DIn[0] = Beam Loss
#DIn[1] = Access
#DIn[2] = Vacuum
.
.
.
#DIn[14] = RF

#Dout[0]
v
#Dout[1]
} = ***Beam Permit***

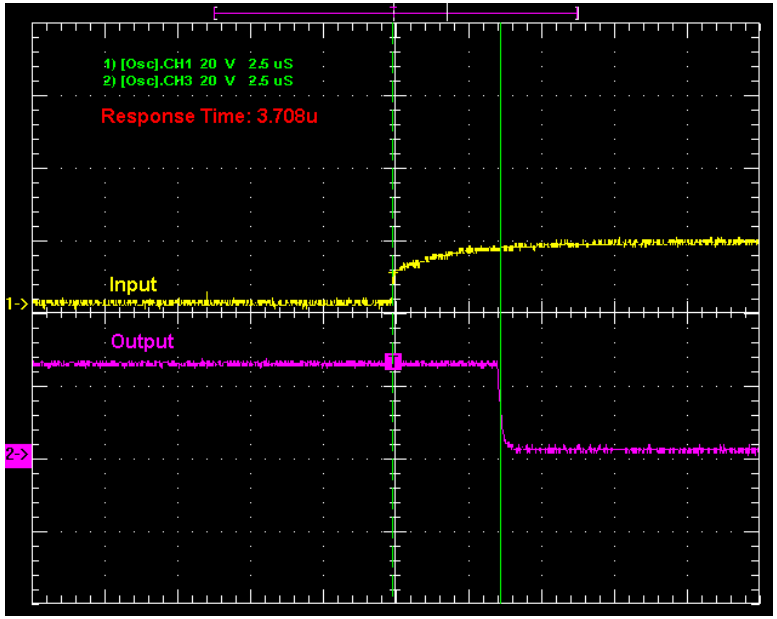
Control: Program and Response Time Analysis

- The Number of Inputs to an AND or to an OR gate does NOT affect the Response Time.

AND gate of 2 inputs



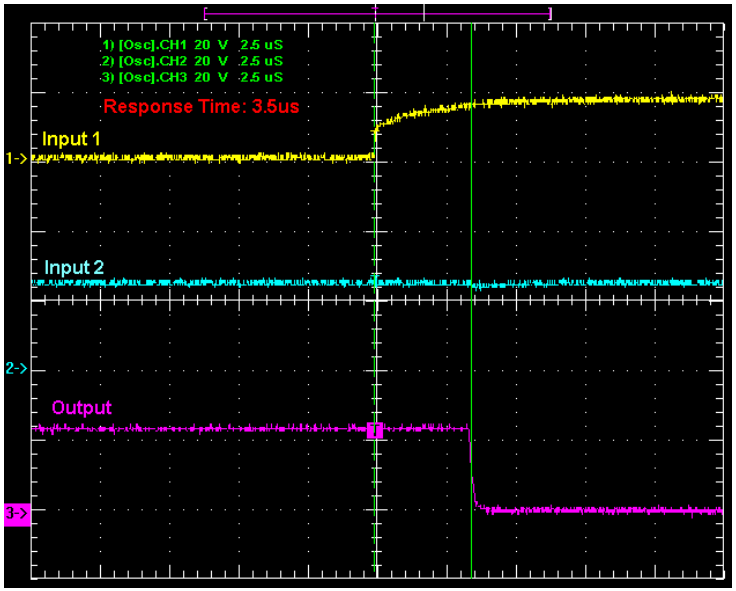
AND gate of 12 inputs



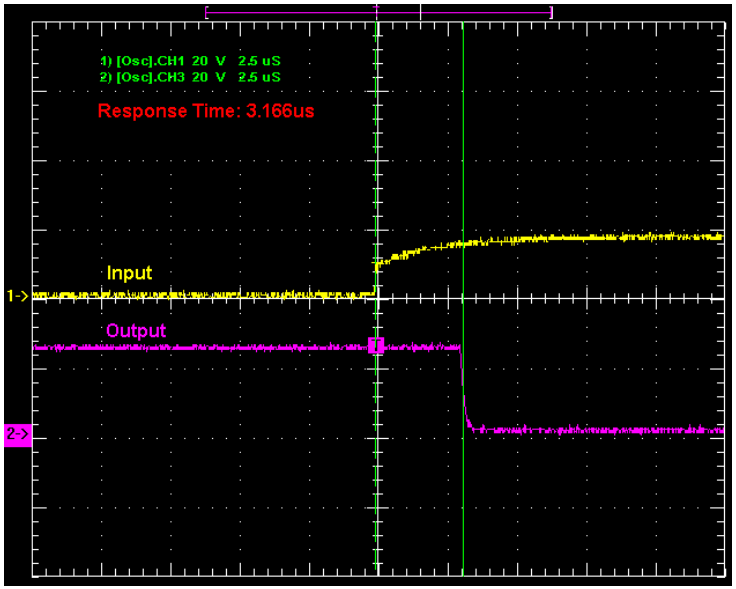
Control: Program and Response Time Analysis

- The Size of the program does NOT affect the Response Time due to it is executed in Parallel (FPGA) not sequentially

Complex Program + OR gate: 51% FPGA



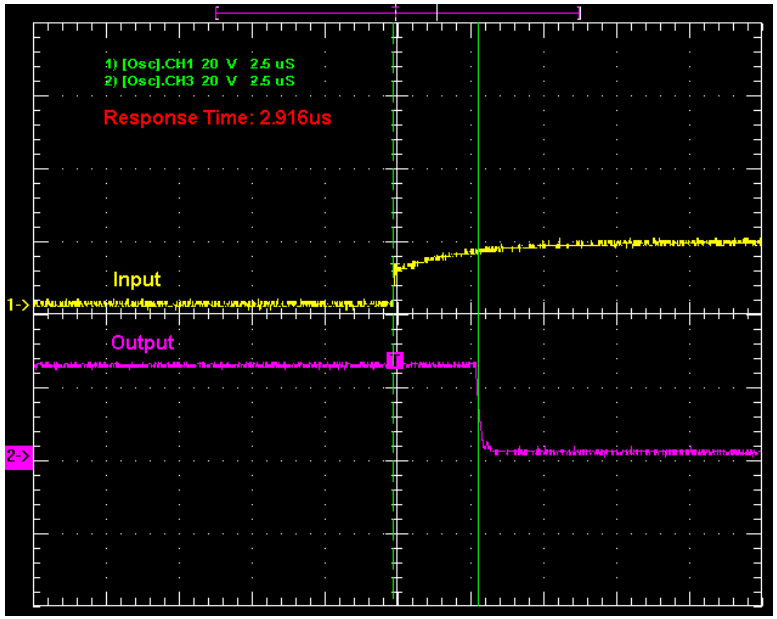
Simple Program (the output follows the input): 11% FPGA



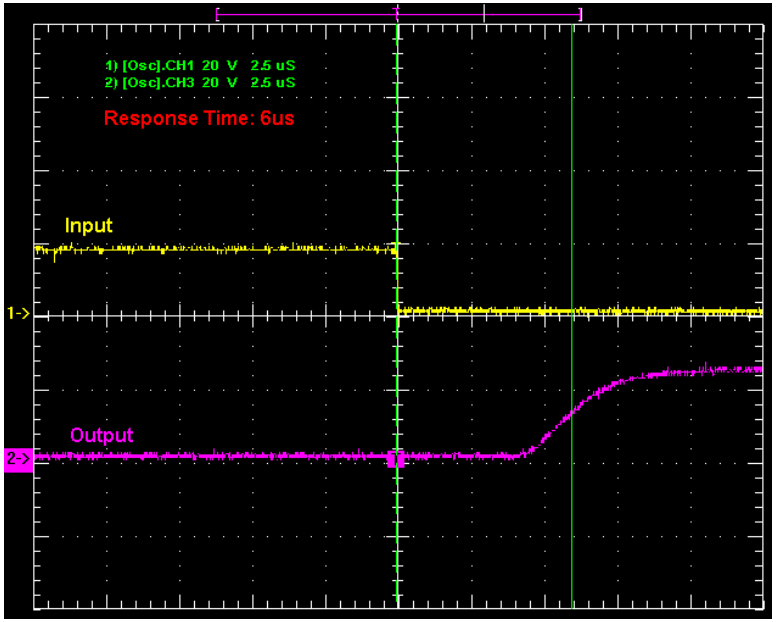
Control: Program and Response Time Analysis

- The Typical Response Time of an Output Activation is **3µs**
- The Typical Response Time of and Output Deactivation is **6µs**

Output Activation

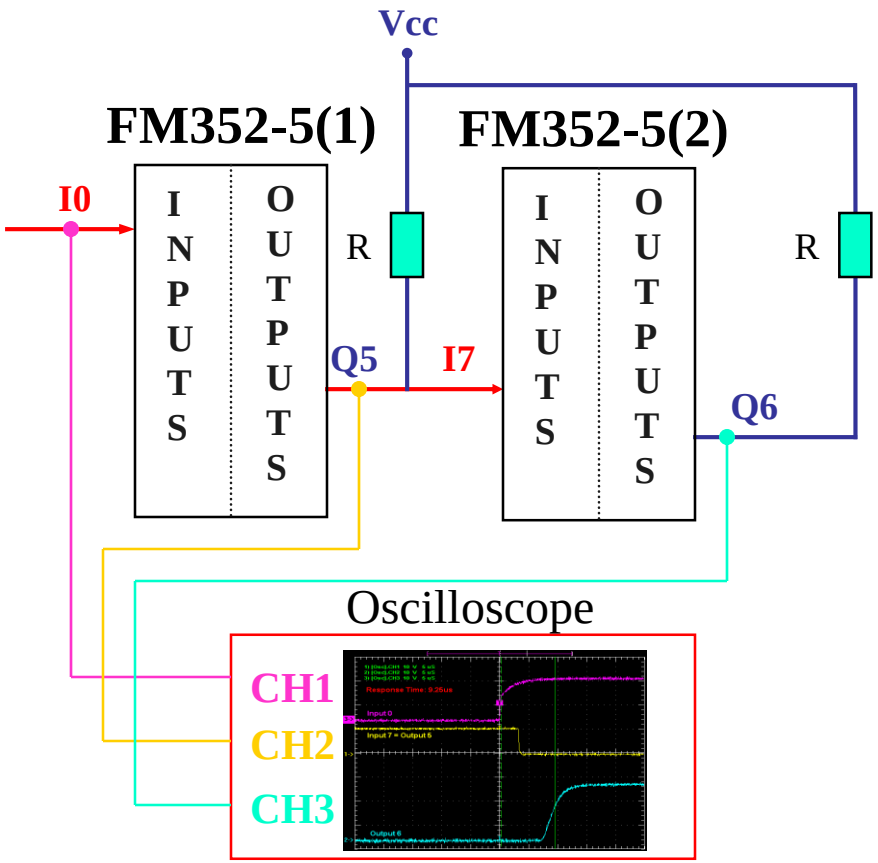


Output Deactivation

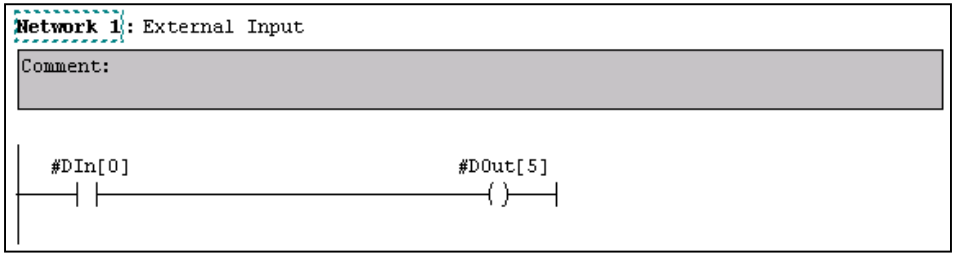


Control: Program and Response Time Analysis

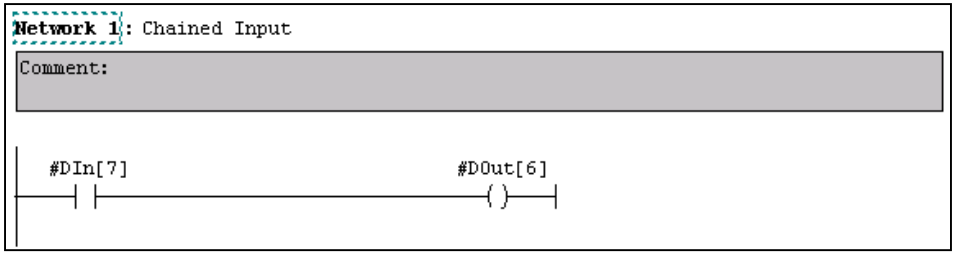
- Chained Modules Configuration and Program:



Control Program run by FM352-5(1)



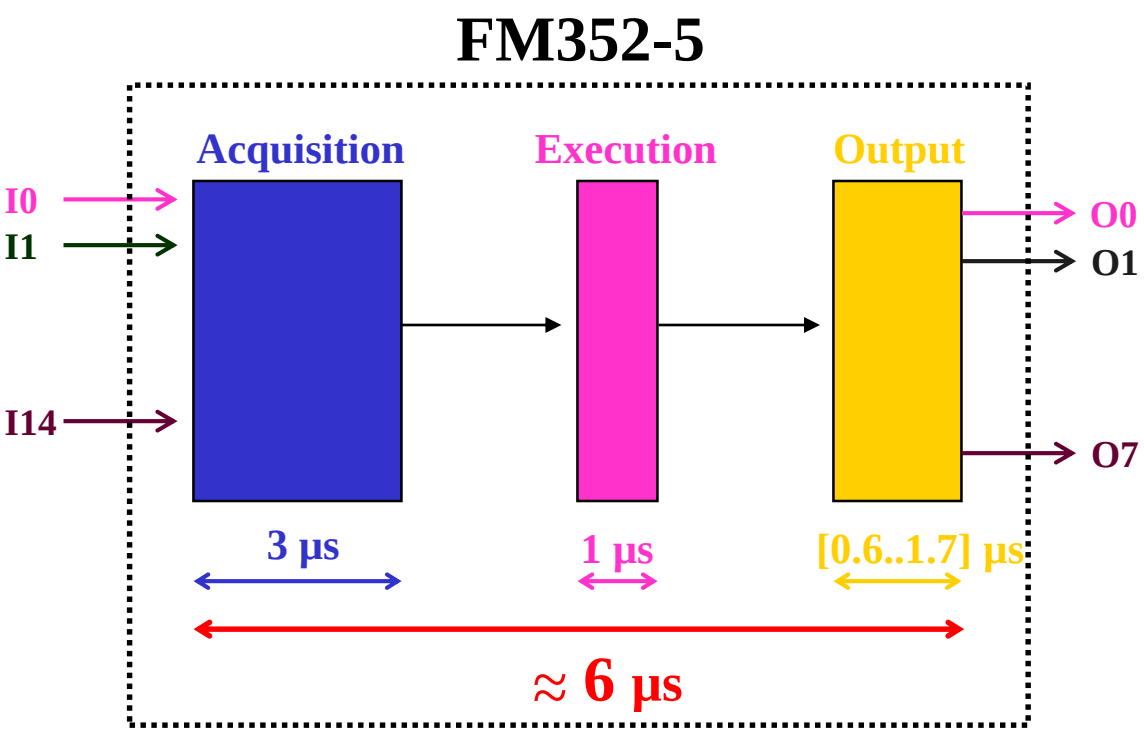
Control Program run by FM352-5(2)



- Response Time for Chained Modules of an Output Deactivation is ~ **9.25µs**
- Response Time for Chained Modules of an Output Activation is ~ **10.83µs**

Control: Program and Response Time Analysis

- If we Study the Technical Specifications of the FM352-5 module we see that the Response Time is **[2..6] µs**

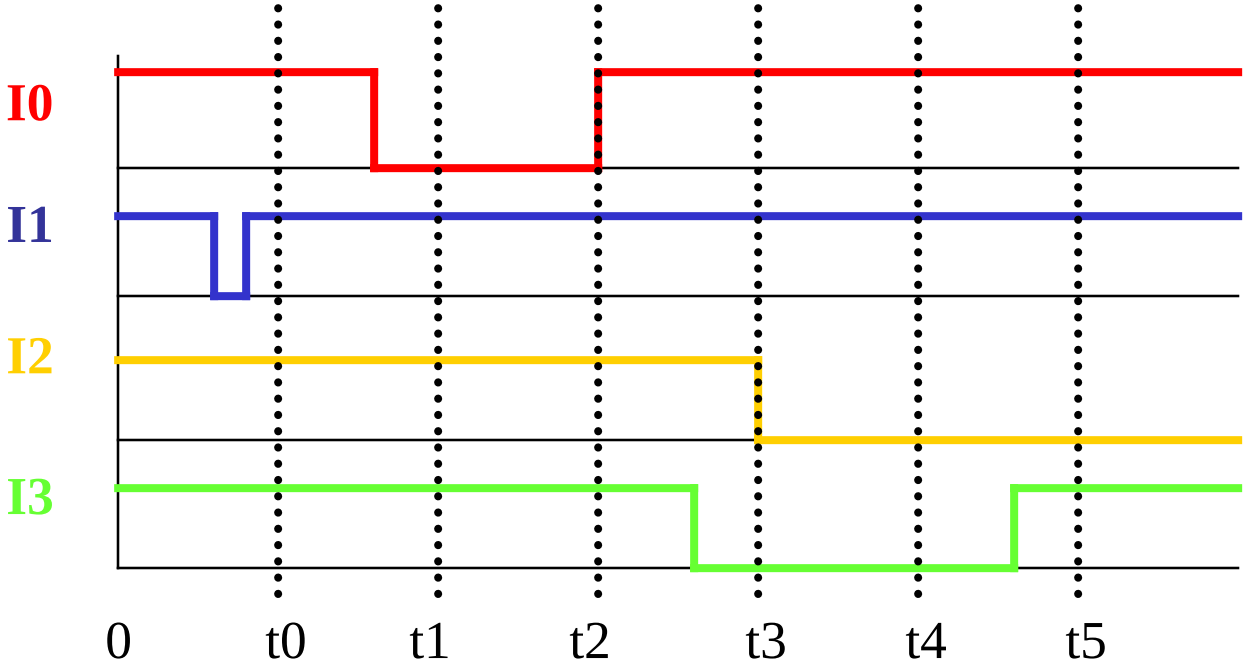


Control: Program and Response Time Analysis

- **Conclusions about process control using the FM352-5:**
  - We have a Knowledge of the environment **3µs** delayed.
  - We could Control the process with a Granularity of **6µs** in Single FM352-5 Configuration or **12µs** in Chained Configuration.
  - If we check the FPGA percentage of Occupation
    - A single logical gate of 2 Inputs (AND or OR): 11%
    - A single logical gate of 12 Inputs (AND or OR): 12 %
    - With an AND gate of 12 inputs and an OR gate of 12 Inputs: 12%
    - FPGA percentage of occupation computed through Time Slices (1200 maximum, 436 minimum for fixed resources - Intelligent Compiler Savings).

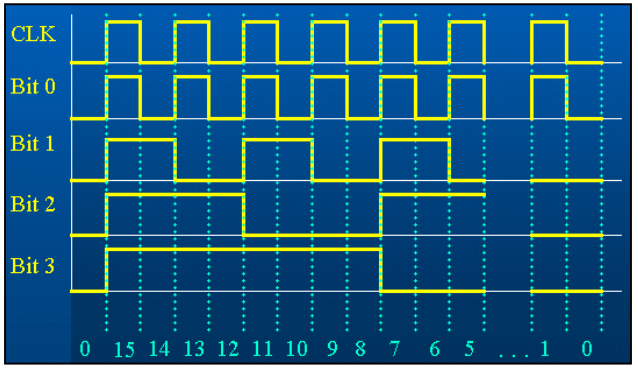
Monitoring: Requirements and Programming

- Target: *Continuous* monitoring *of the inputs performing a* ***Time Stamping*** *if any of these signals change.*



Monitoring: Requirements and Programming

- Several Solutions for Absolute Time Stamping.
- Programming Elements for **Time Interval Measurement**:
  - **Timers:** The time is measured in tenths of µs. We have precision of **10µs**.
  - **Counters:**
    - Internal Clock Generation: CP_GEN programming primitive allows a maximum frequency of 50 KHz (**20µs**)
    - External Clock Generation: The Maximum frequency allowed is 200kHz (**5µs**).
  - Counter **Using Frequency Divisors** 400KHz (**2.5 µs**):



Conclusions and Further Work

- The LHC Beam Interlock system must be **Safe** and **Real-Time**:
  - Robust and Reliable: PLC module
  - Deadlines of µseconds order (LHC Beam Turn = 88µs)
- The FM352-5 provides these features as a PLC module.
- We could consider the FM352-5 Boolean Processor as a Promising Monitoring and Control Device for the heart of the BIC.
- Further work: Evaluation of VME device faced to the PLC module.

Acknowledgements and References

- **Acknowledgments**: I like to thank the input of *Bruno Puccio* and *Rudiger Schmidt*.
- **References**:
  - F. Bordry, R.Denz, K-H.Mess, B.Puccio, F.Rodriguez-Mateos and R.Schmidt, *Machine protection for the LHC: Architecture of the Beam and the Powering Interlock systems*, LHC Project Report 521, 2001
  - Vicente Soriano, Manuel Zaera, Carlos Palau, Manuel Esteve, *Comunicaciones Industriales. Programacion de PLCs y PROFIBUS* (in Spanish), ISBN 84-699-3375-2, 2000.
  - Siemens, *FM352-5 High-Speed Boolean Processor. User Manual*, Edition 12/2001.

THANK YOU FOR YOUR ATTENTION !!!