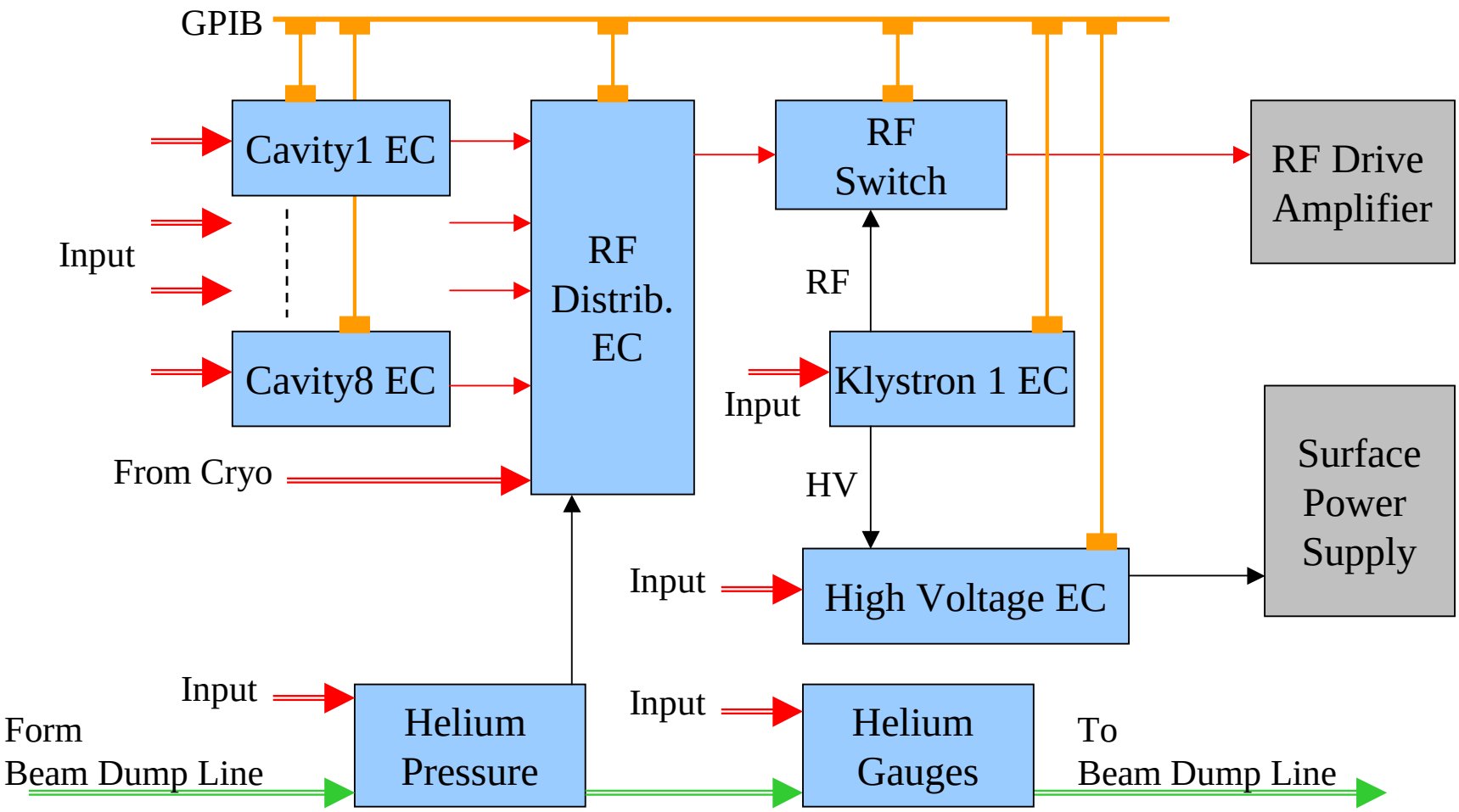
LEP2 and LHC Interlock System

- The Past
  - The “LEP2” System
    - Structure, Layout, Beam Dump, Hw, Sw, Diagnostic etc..
- The Present
  - The Evolution
    - Structure, Layout, Hw Modules, PLC, Sw, Tests etc..
- The Future
  - Final “LHC” version
    - Structure, Layout, PLC, Sw, Tests etc..
- Conclusions

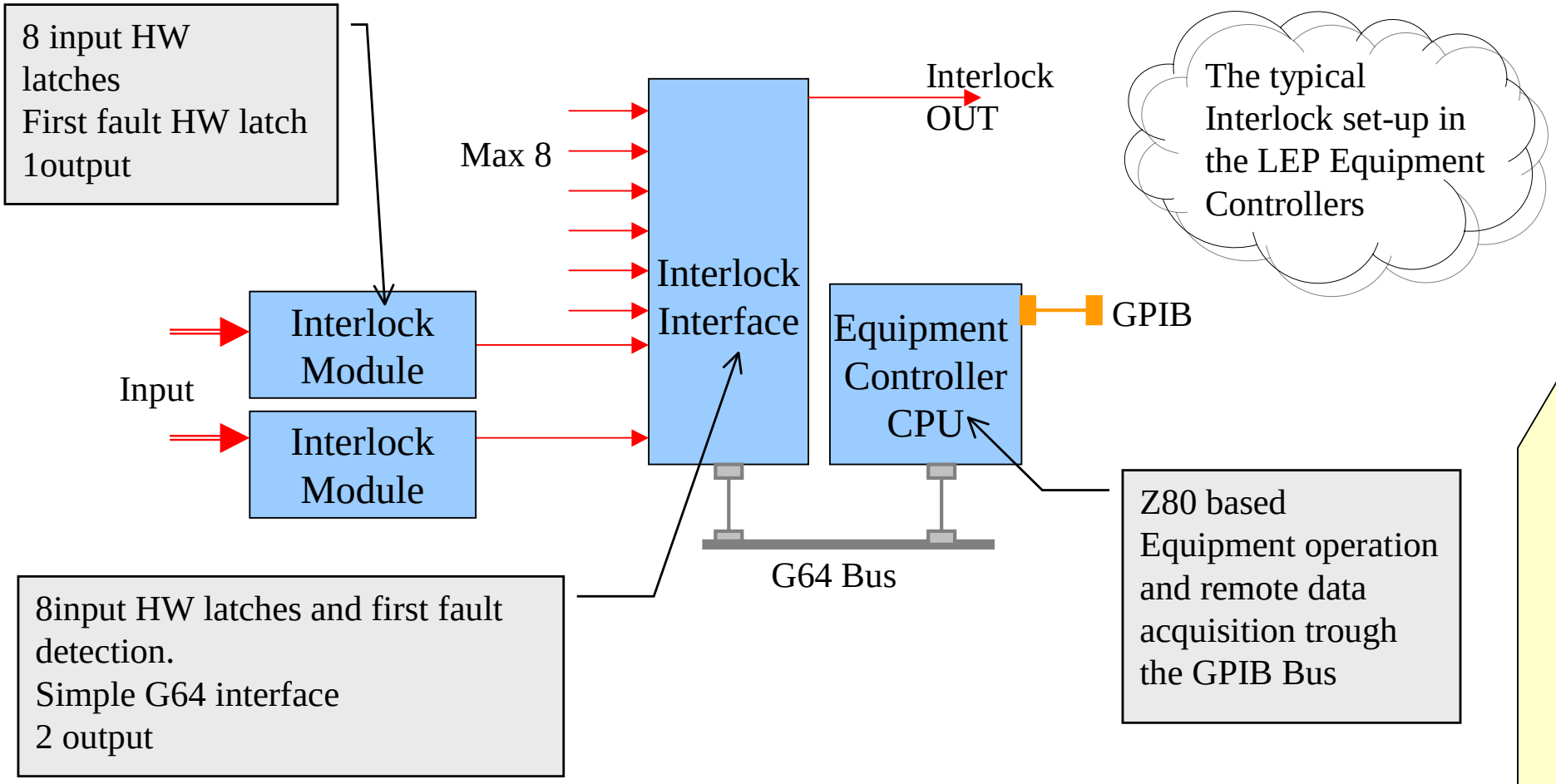
The “LEP” Interlock System

- LEP RF was 288 SC Cavities in 4 Points and a total of ~8000 interlocks RF and HV
- Full hardwired logic (TTL) implementation no software interlocks
- Interlock Interface&Module on the Cavity, Klystron and High Voltage Equipment Controller
- Helium Pressure and Gauges directly connected to the Beam Dump line (~570 relay connections)
- Communication with the control via G64 and GPIB Bus

The “LEP” ½ unit Interlock Structure



The “LEP” Interlock Hardware



The “LEP” Interlock Conclusion

GOOD

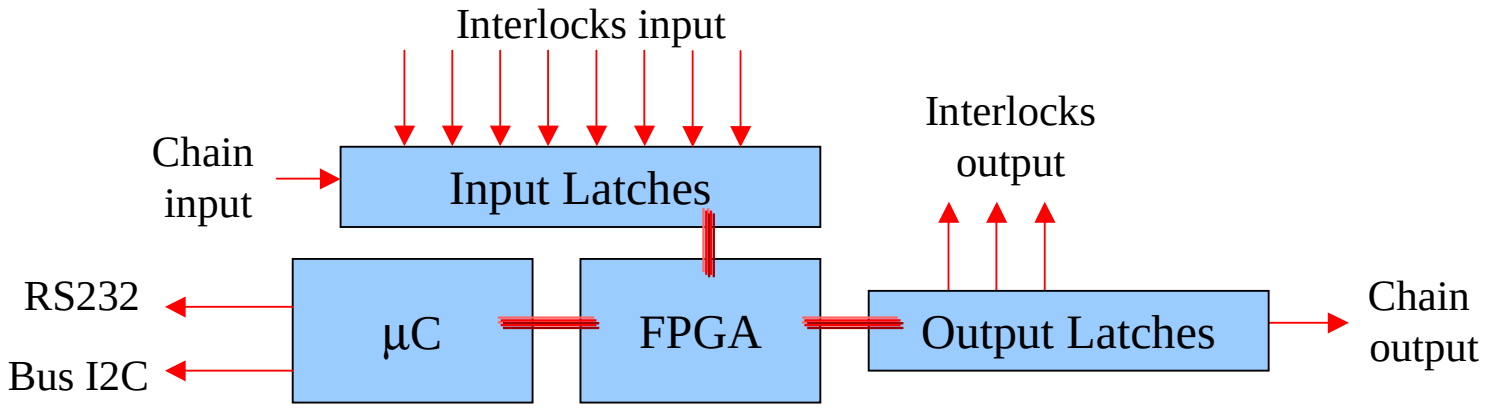
- TTL Logic was a reliable an simple solution *vs.* relay contact solution
- Modular system with local display (LEP was accessible)
- Full remote read-out
- Always a very reliable equipment protection during operation

LESS GOOD

- Unreliable and slow communication (GPIB) with unit controller
- Interlocks faults names coded in the EC software and sent to the unit controller in ASCII format, human readable strings, leading to high communication load
- Poor Beam Dump diagnostic and time stamping (new system added in 99)
- Full hardware solution … not enough flexibility
- Interlock information spread in different Equipment Controllers
- No information on Hw forced interlocks (specialists discipline needed !!)

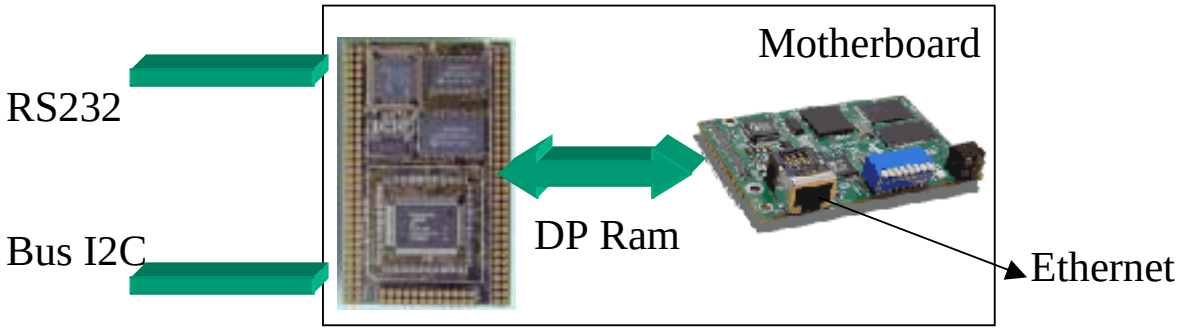
The Evolution …

- The Interlock Module Hardware
  - Keep a modular and TTL hardware approach (reaction time < 3µSec)
  - Redesign the diagnostic Hw with µC and FPGA for a gain in flexibility
  - Interlocks can now be software forced
  - I2C communication bus between modules and Interlock Controller (! ISP)
- The Interlock Module Software
  - First Fault, All Faults and Forced Faults are stored in the µC and sent to supervision
  - Remote µC program download via RS232⇔Ethernet interface

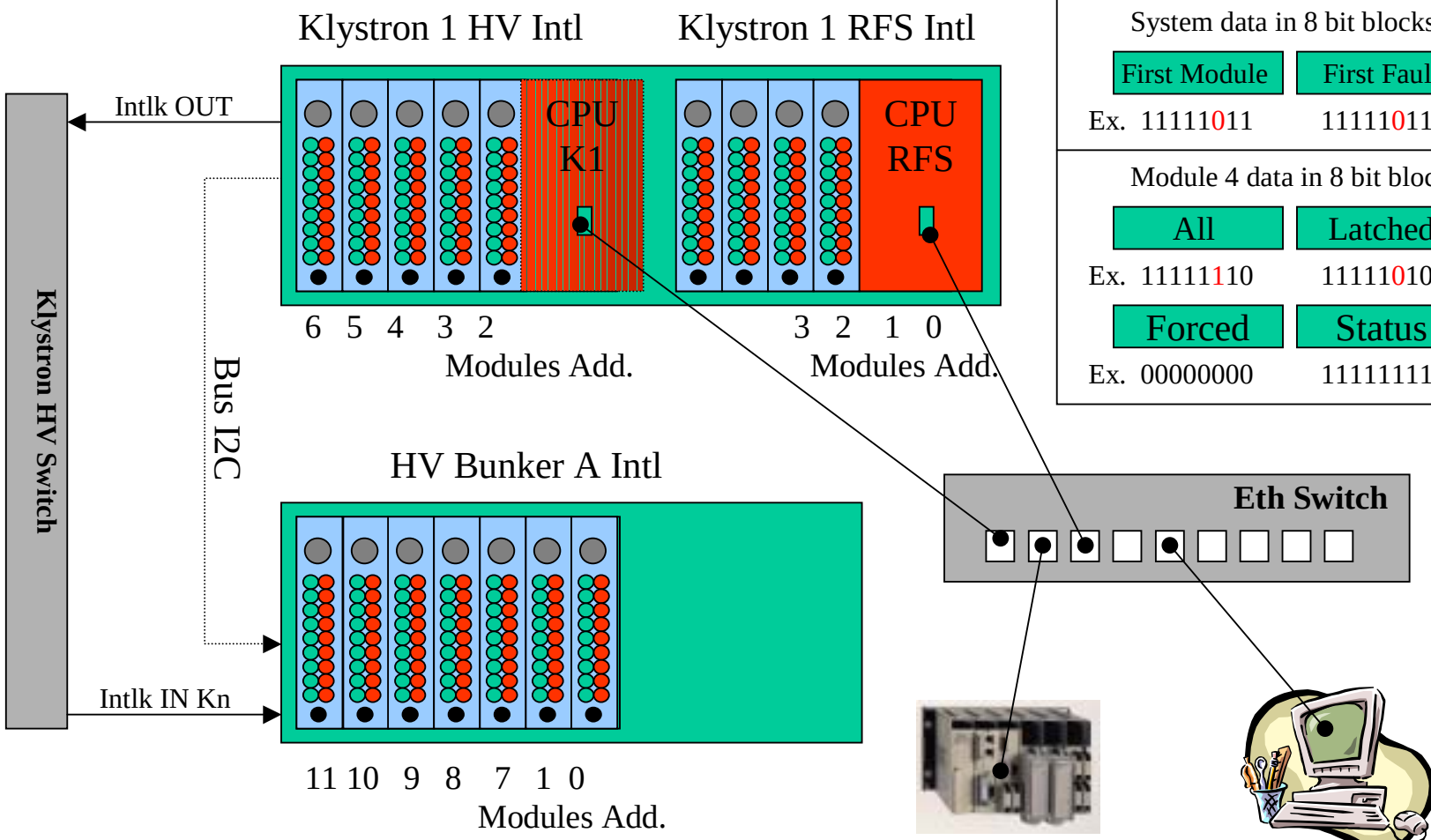


… The Evolution

- The Interlock Controller Hardware
  - Modular design (COTS mezzanines on custom motherboard)
  - One µC mezzanines (C51 based)
  - One communication mezzanines (HMS Anybus Modbus/TCP)
  - Hardware watchdog
- The Interlock Controller Software
  - First level of data formatting, Interlock code generation and system alarms
  - Ethernet communication with the supervision (PLC IoScan)
  - First Fault, All Faults and Forced Faults are stored in the µC and sent to supervision

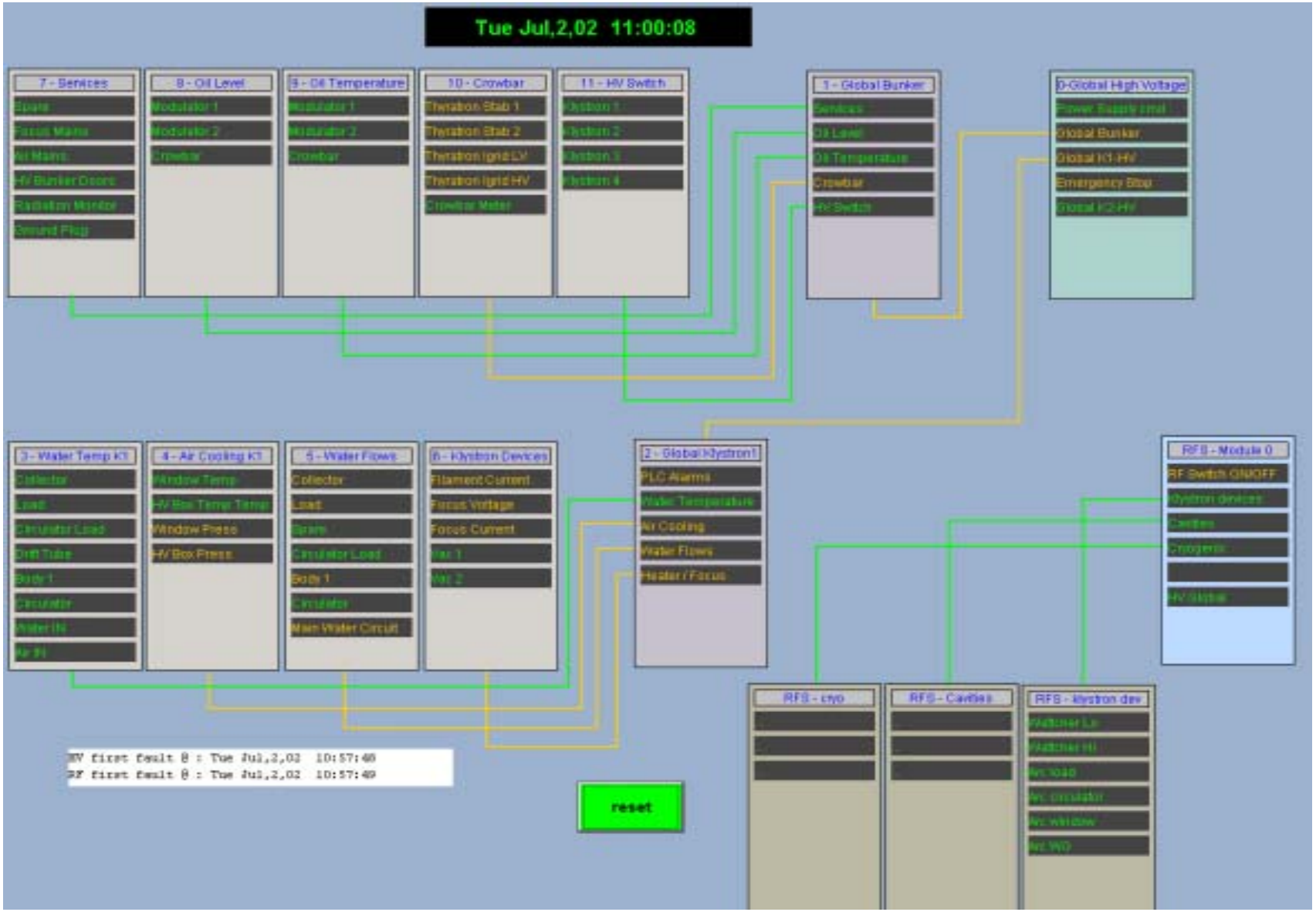


H112 Test Interlocks layout



Interlock code example	
System data in 8 bit blocks	
First Module	First Fault
Ex. 11111011	11111011
Module 4 data in 8 bit blocks	
All	Latched
Ex. 11111110	11111010
Forced	Status
Ex. 00000000	11111111

Interlock Screen

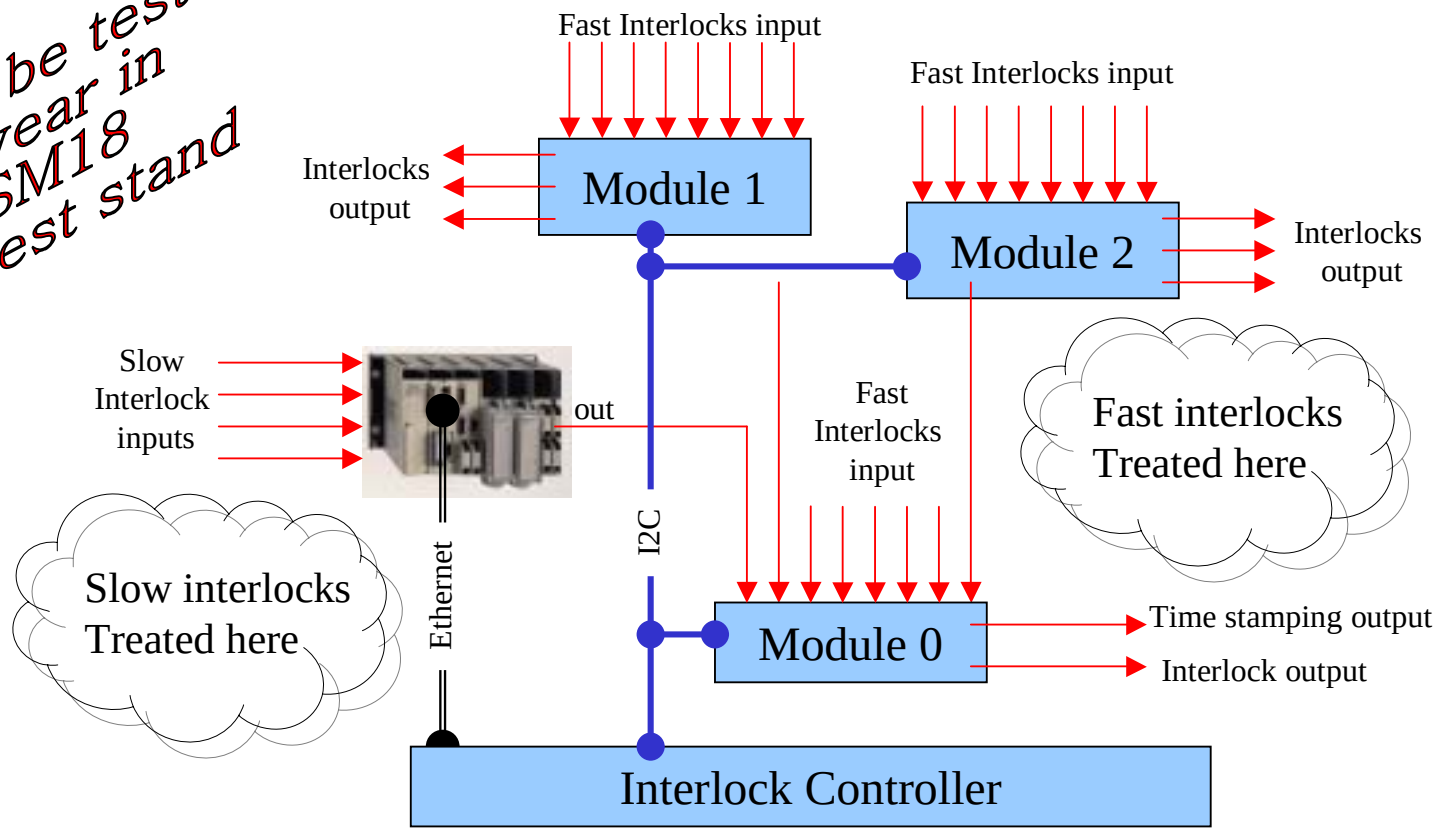


The proposed “LHC” interlock system

- The LHC RF will be 16 cavities/klystron Line and 4 HV bunkers with a total of ~1000 interlocks
- NEW Slow (~20mSec) interlocks will be treated by the PLC (Ex. Temperature, water flows)
- Only Fast (<3µSec) interlocks will be connected directly to the interlock system
- This will result in ~600 fast interlocks and ~400 slow interlocks so ~ 5 interlock Modules per Line
- NEW The PLC has a “sum of faults”output to the interlock system
- NEW A common time stamping system (GPS/IrigB) will be triggered by one dedicated interlock output
- NEW The PLC will read back the Interlock system status and provide a comprehensive code for the supervision (first fault, all faults, forced faults)
- Interface to the BIC system form Helium (later from HV and RF trips)

“LHC” interlock system diagram

This will be tested next year in the SM18 Cavity test stand



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