LHC Beam Loss Monitor

Design Considerations of Digital Parts.

LHC Machine Protection WG meeting
(28 May 2004)

LHC Beam Loss Monitor (TOC)

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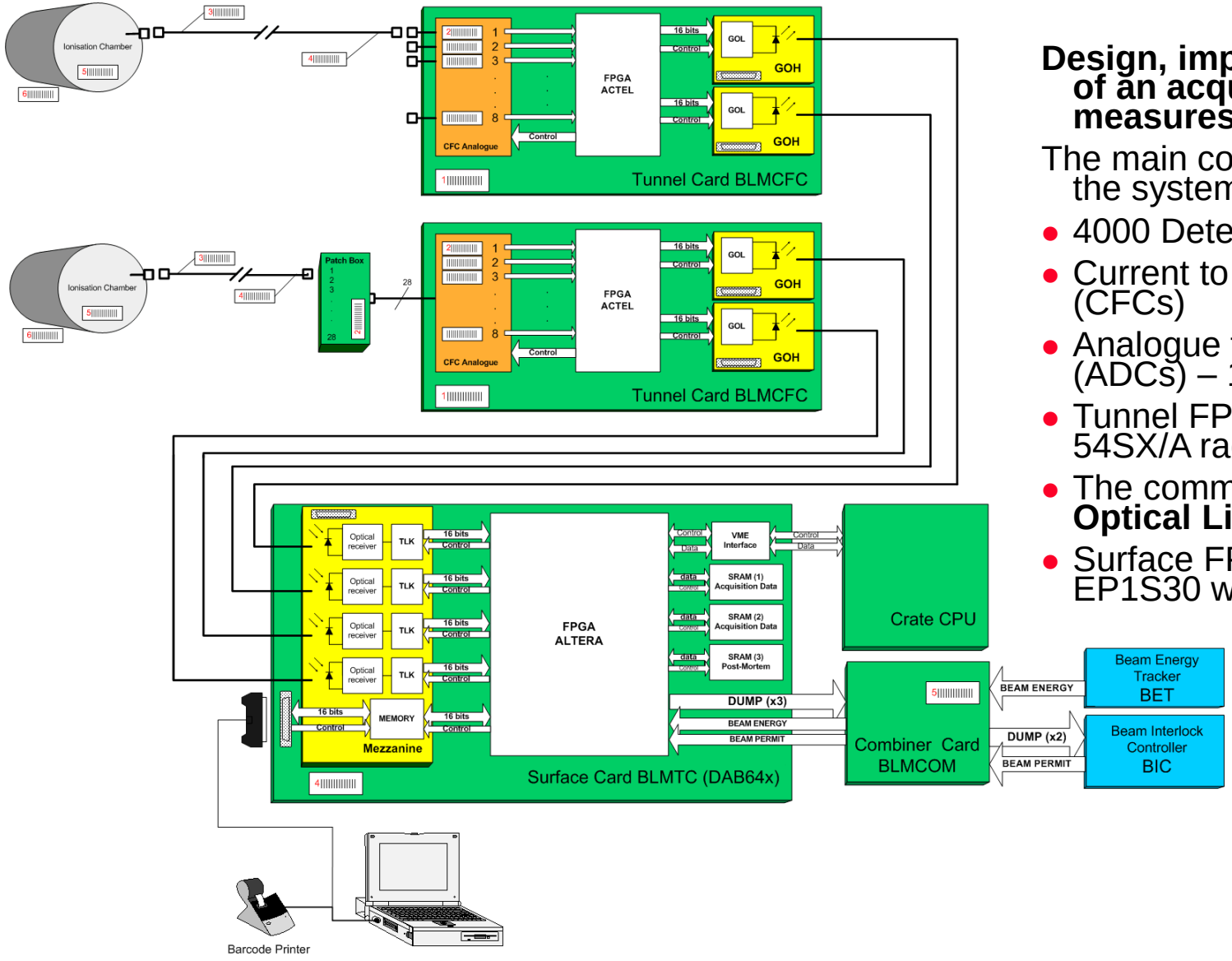
BLM Overview



Design, implementation and testing of an acquisition system that measures the particle loss rate.

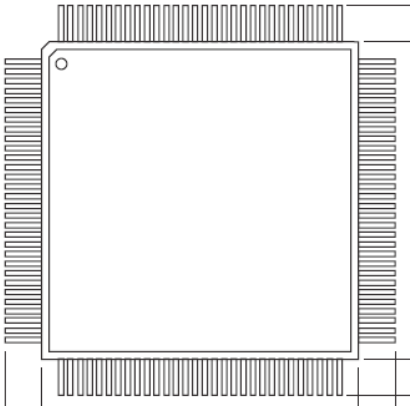
The main components that comprise the system are:

- 4000 Detectors in total
- Current to Frequency Converters (CFCs)
- Analogue to Digital Converters (ADCs) – 12 bits
- Tunnel FPGAs: **Actel**'s family 54SX/A radiation tolerant.
- The communication links - **Gigabit Optical Links** running at 800 Mbps.
- Surface FPGAs: **Altera**'s Stratix EP1S30 with 780 pin.

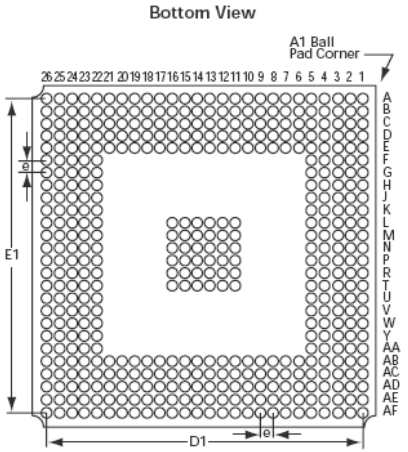
CFC Card Digital Part

Design criteria

- Radiation Tolerant Devices available:
  - Actel SX/A family ($40 for the 54SX32A)
  - Xilinx QPRO family (~20x more)
- Not very complicated digital part design but
  - Triple module redundancy (TMR)
  - Medium device
- Choose PQFP instead of BGA package
  - Will give simpler and cheaper PCB
  - Make use of socket

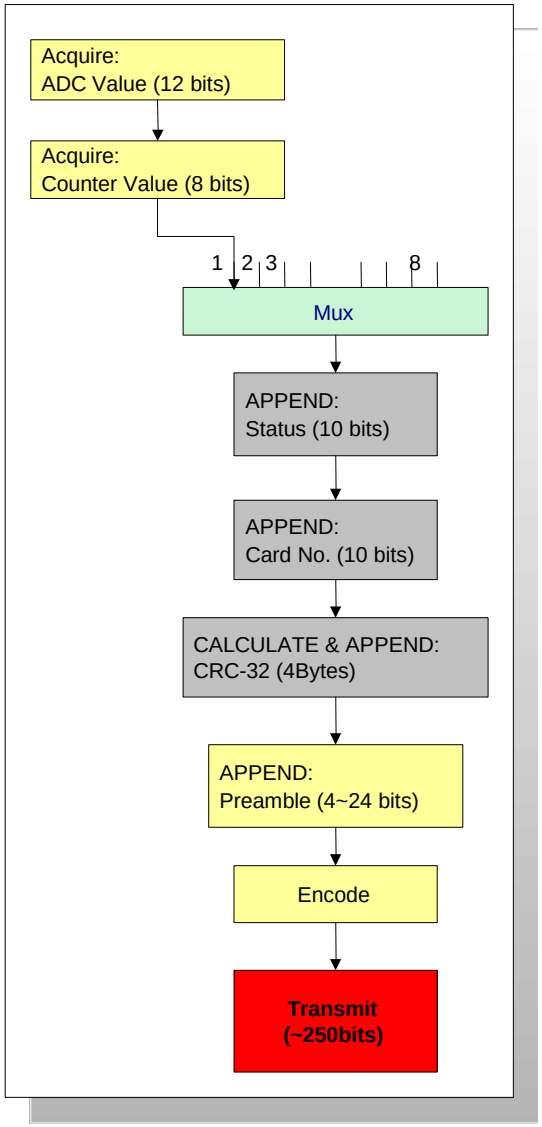


Plastic Quad Flat Pack



Ball Grid Array

Implementation of Tunnel FPGA



✓ Tunnel PCB arrangement

- 8x12bit ADC in parallel + control signals,
- 8 Counter inputs,
- Actel 54SX with 208 pins
- Connectors for GOH mezzanines.

✓ Production of CRC-32 error detection redundant information

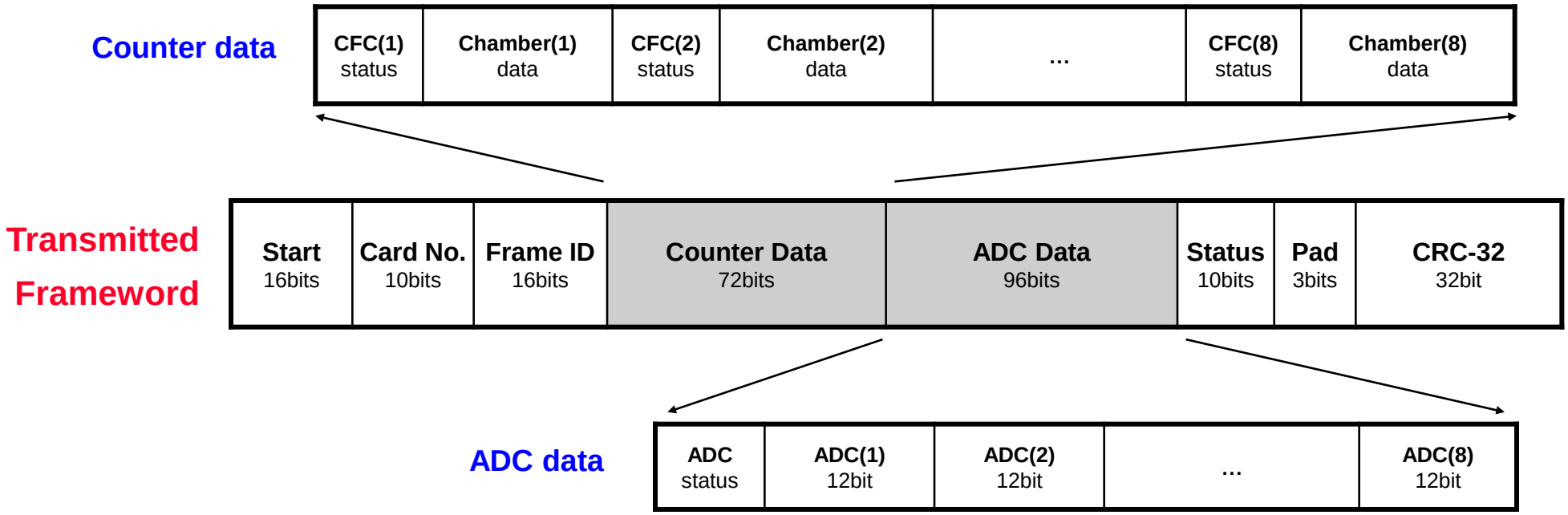
✗ To be done:

- Counters
- Registers for ADC data
- Multiplexing of all information

} Dependant on communication channel choice.

Frameword for Transmission

- **Formatting of the frameword for transmission (256 bits)**



- **Transmission of frameword every 40μs.**
  - **The data rate must be high enough to minimise the total latency of the system .**

Error-free Communication

The steps taken to ensure a reliable communication link:

- **Double (redundant) optical link**
- **CRC-32 error check algorithm**
  - **All single-bit errors.**
  - **All double-bit errors.**
  - **Any odd number of errors.**
  - **Any burst error with a length less than the length of CRC.**
  - **For longer bursts $Pr = 1.16415*10^{-10}$ probability of undetected error.**
    - **224 bits of data plus 32 bits of CRC remainder = 256 bits.**
- **8b/10b encoding**
  - **Clock data recovery (CDR) - guarantees transition density.**
  - **DC-balanced serial stream - ones and zeros are equal/DC is zero.**
  - **Error detection – four times more characters.**
  - **Special characters used for control – sync, frame.**
    - **256 bits of data are encoded in 320 bits = 64 extra bits.**

Communication Link Options

I. Use the Gigabit Optical Link (GOL) chip

- High-speed transmitter ASIC (at 800 or 1600 Mbps).
- Radiation tolerant layout (in 0.25 mm CMOS technology).

Also includes:

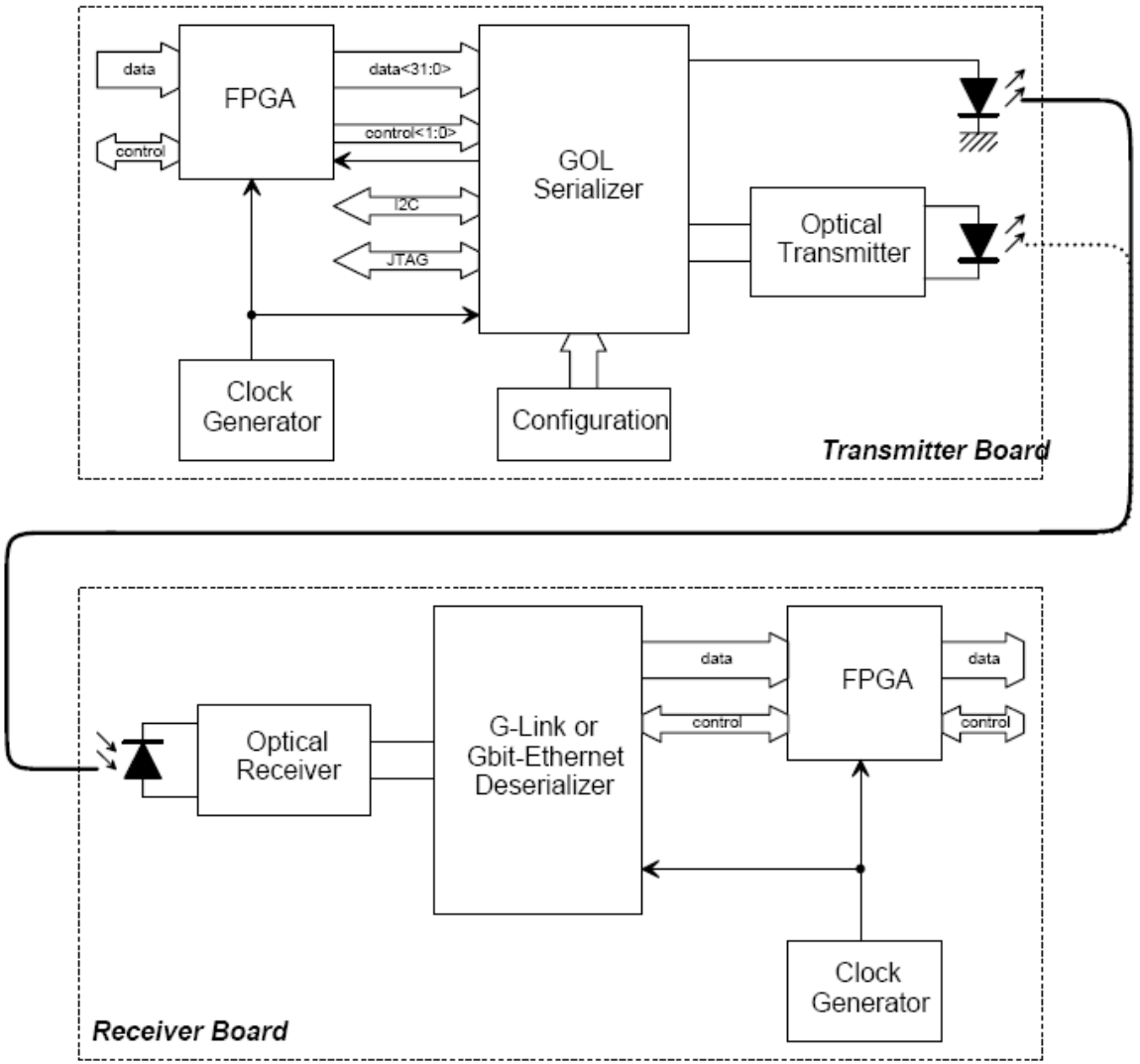
- Analogue parts needed to drive the laser.
- Algorithm running that corrects SEU.
- 8b/10b encoding.
- 16 or 32 bit input.
- Error reporting (SEU, loss of synchronisation,..)

More Advantages:

- **Very low cost** (50CHF for both ASIC & Laser or 200CHF as mezzanine).
- Already tested and functional.
- Independent system.
- Allows later improvement of design.

II. Build a custom communication link.

GOL Transmitter



Interfaces for registers:

- I2C
- JTAG

Drivers:

- Laser driver
- 50 Ω driver

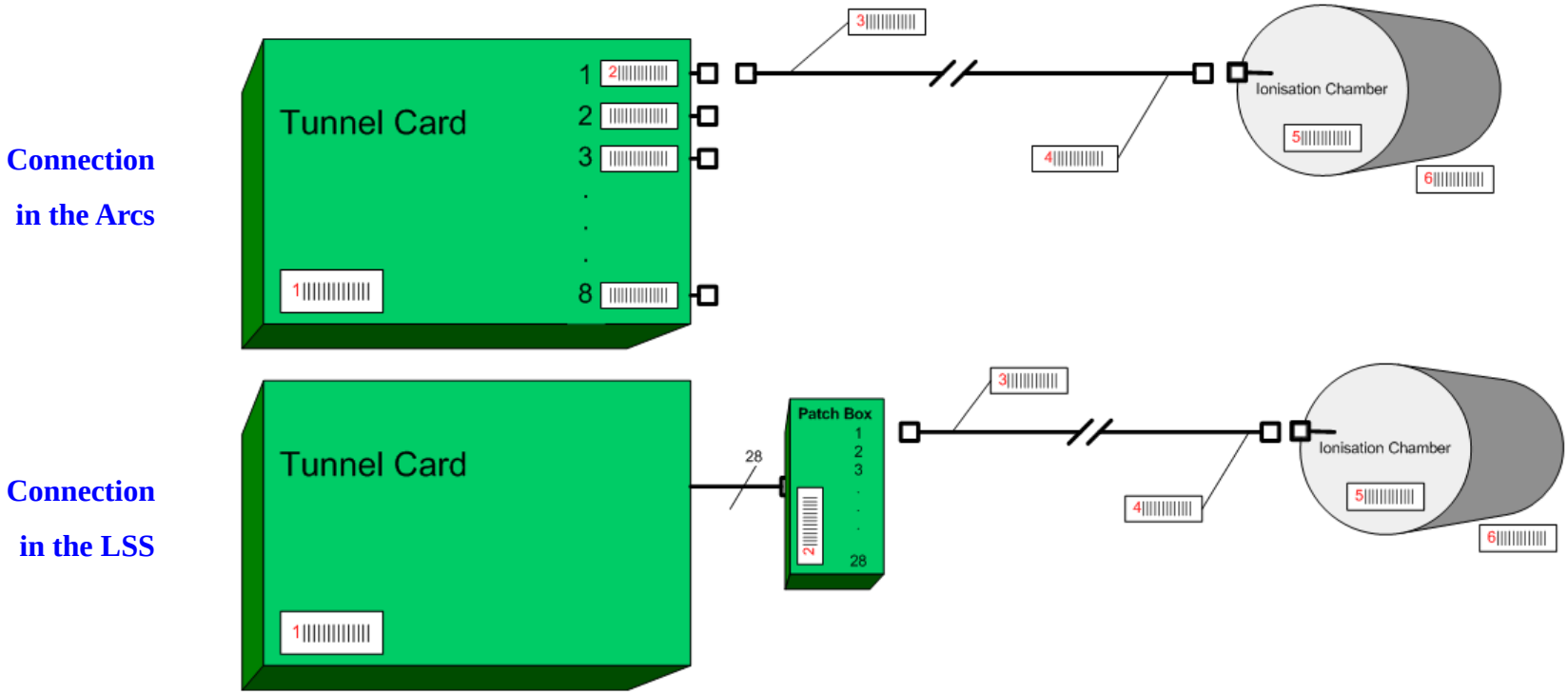
SEU: 60 MeV protons (Louvain):

- Fluence: $2.20*10^{12}$ p/cm^2
  (flux $3*10^8$ p/(cm^2 s) (3.14 KGy)
- No errors observed
- Limit cross section:< $4.5*10^{-13}$ cm^2

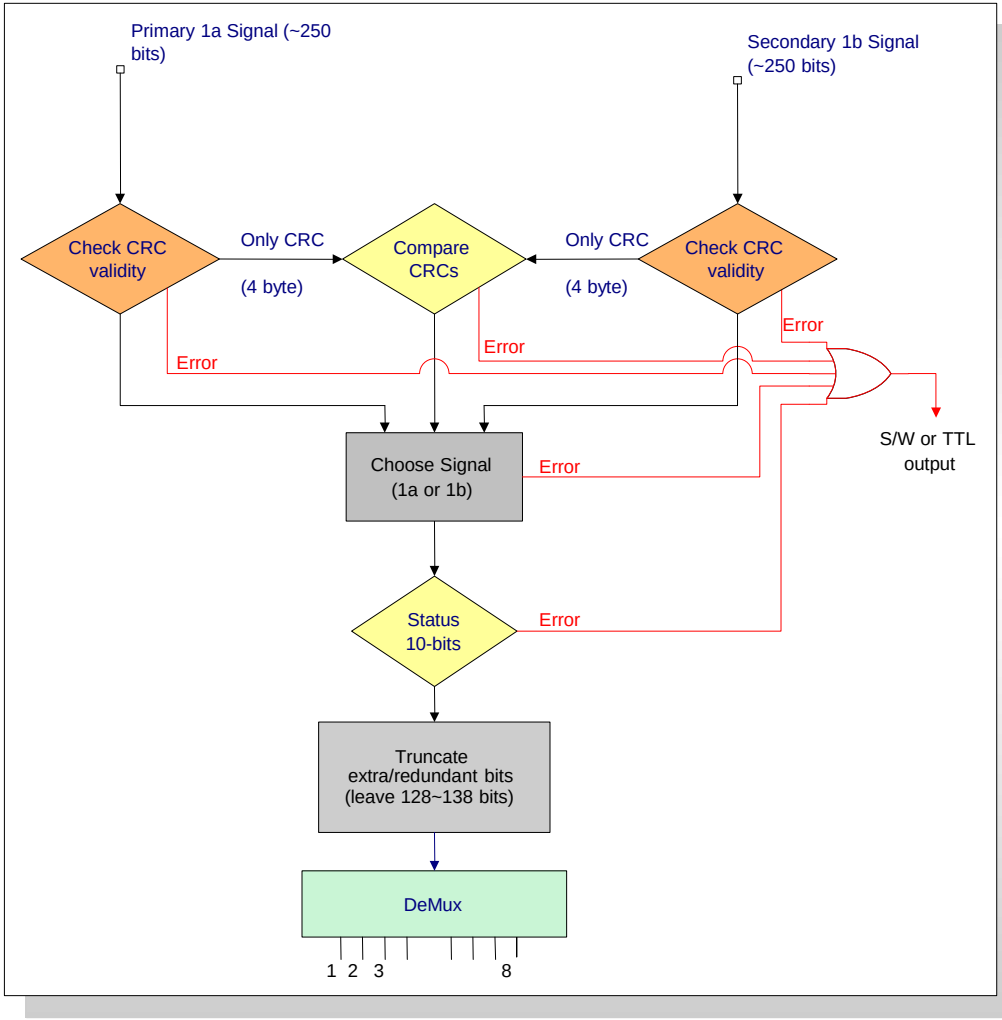
GOL web site (http://cern.ch/proj-gol)

Identification of cards

- **Identification of cards**
  - Barcode system for installation and indexing of cards, cables, detectors, position
  - Digital ID of cards on every transmission/check
  - Serial number for each frame transmitted



Transmission Check & Tunnel Status



The Surface FPGA receives:

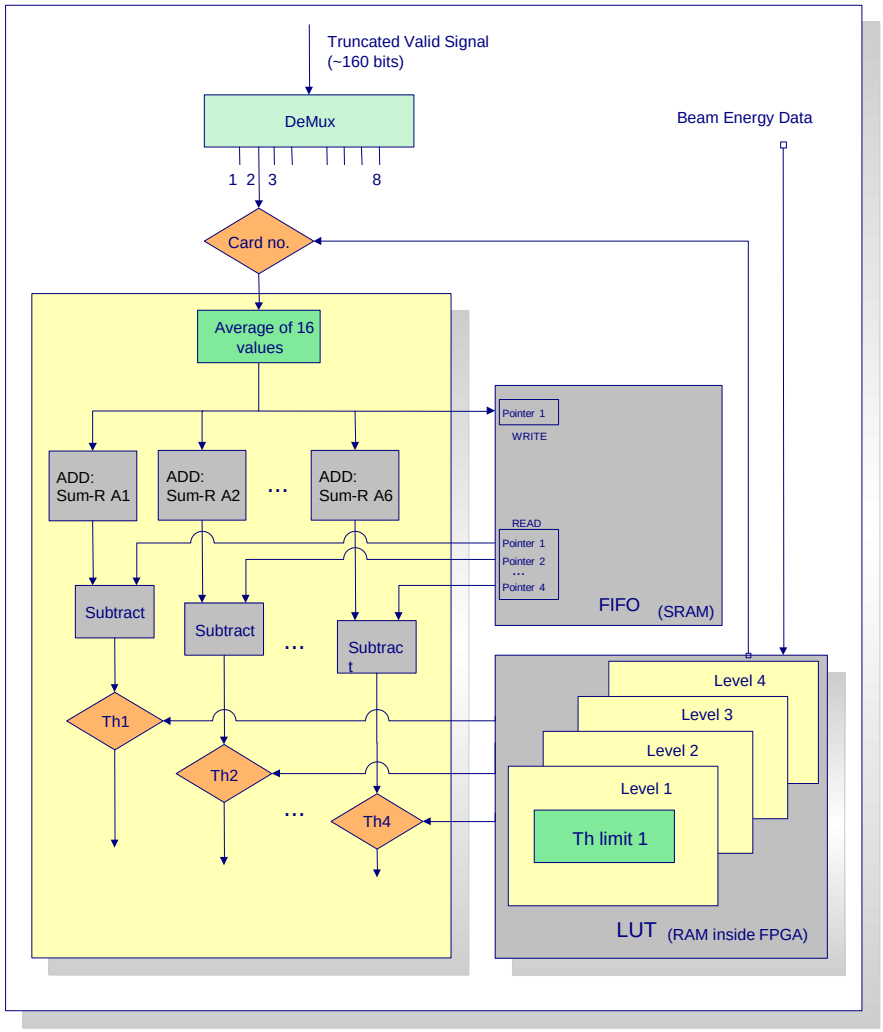
- ✗ **Double/redundant optical transmission**
  - **4 optical receivers on each card**
  - **If the GOL is used then the TLK chip from TI has direct compatibility.**
- ✓ **16 channels/detectors data**
  - **Receiver of 2 tunnel cards**
- ✓ **CRC-32**
  - **Error check / detection algorithm for each of the signals received.**
  - **Comparison of the pair of signals.**
- ✓ **Signal Select block**
  - **Logic that chooses signal to be used**
  - **Identifies problematic areas.**
- ✓ **Tunnel's Status Check block**

Signal Select Logic

CRC32 check		Comparison of 4Byte CRCs	Output	Remarks
A	B			
0	0	0	**Dump**	Both signals have error
0	0	1	**Dump**	S/W trigger (CRCgenerate or check wrong)
0	1	0	**Signal B**	S/W trigger (error at CRC detected)
0	1	1	**Signal B**	S/W trigger (error at data part)
1	0	0	**Signal A**	S/W trigger (error at CRC detected)
1	0	1	**Signal A**	S/W trigger (error at data part)
1	1	0	**Dump**	S/W trigger (one of the counters has error)
1	1	1	**Signal A**	**By default (both signals are correct)**
***Where 1:Correct, 0:Error**				

- **In cases when only one signal has errors the system continues by using the correct and issuing a S/W trigger.**
- **If the trigger shows to be repetitive it can give a hint of the problematic area.**

Running Sums



- ✓ **11+1 Running Sums per channel**
- ✓ **3 time regions**
  - **40µs-1ms**
    - run completely internally
  - **1ms-5ms**
    - run completely internally
  - **5ms-100s**
    - external SRAM to store the data
    - Uses averages to reduce data
- ✓ **4 Running sums per region**
- ✓ **Threshold Table**
- ✗ **SRAM Controller**
  - 16 writes and
  - 192 reads every 40µs only for the RS.

Quench Level Thresholds

Threshold values are dependant on

- **Beam Energy and**
- **Integration Time**

The system constantly transmits a value which corresponds to the particles seen over the integration time of 40μs.

- **Using this values the surface FPGA calculates and keeps 11 more running sums per detector.**
- **The max integration time needed to be observed is 100s.**
- **The rest are found by identifying the places where the approximation introduces the minimum fitting error.**

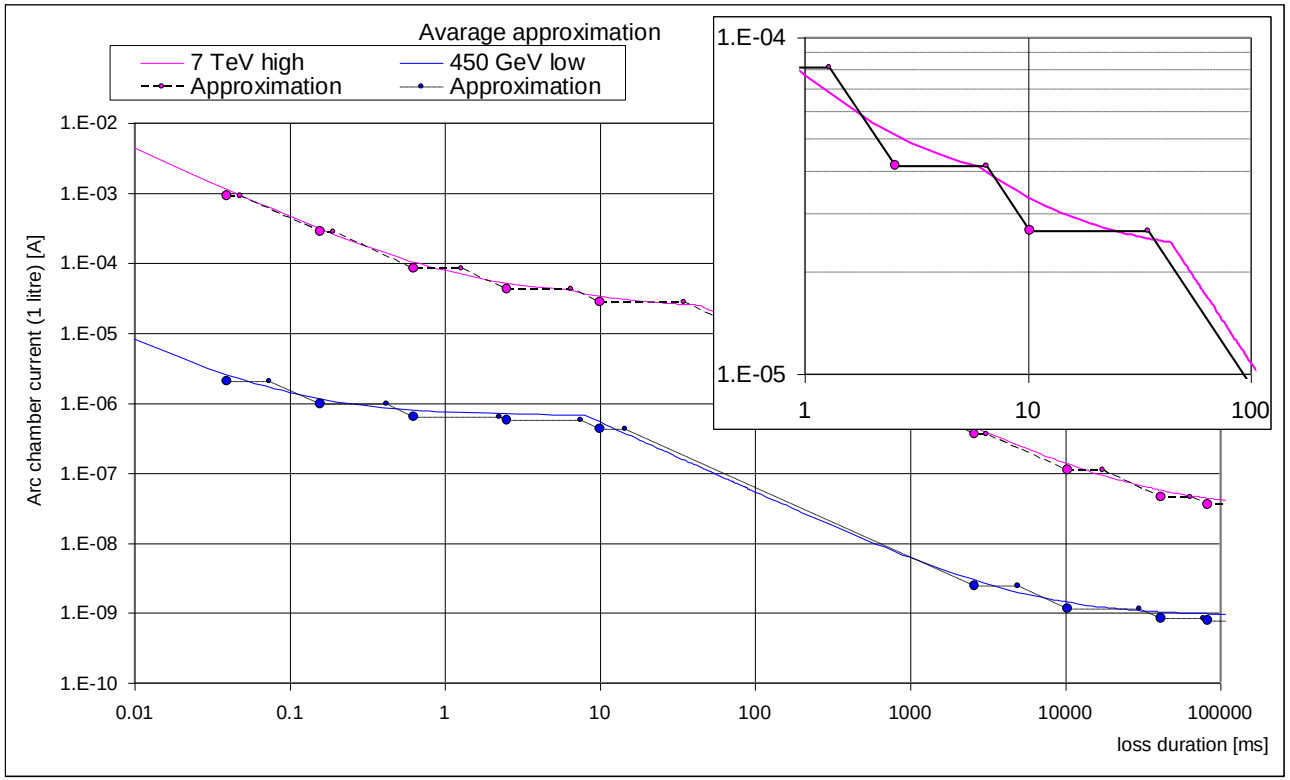
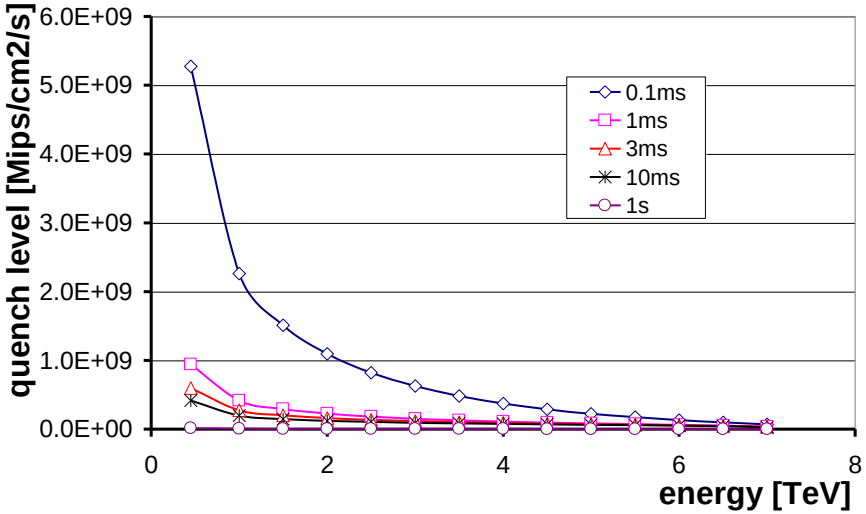


Figure and error calculations by G. Guaglio

Threshold Table

Threshold values are dependant on Beam Energy and the Integration Time

- **32 energy levels**
  - Received through the back-plane
  - from BET module (SIL-3)
  - as a Digital word



- **Unique 2D threshold table for each of 4000 detectors**
  - Stored in a RAM at the mezzanine card.
  - Beam permit will allow internal update
  - Can be used as a calibration and offset correction tool.

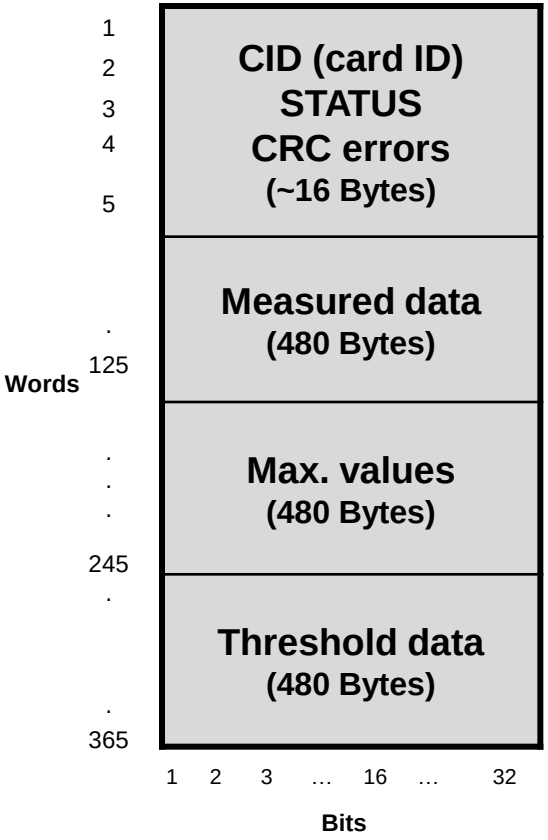
Calculations

- 11+1 *Time windows*
- 32 *Beam Energy Levels* (0 ~ 7 TeV)
- 16 Ionisation Chambers

6,144 *Th* & 2,048 *W* values
or 29 KB & 11 KB respectively per card

Logging Data Arrangement

These data have to be read with a rate of a second in order to be stored in a database as well as to give a graphical representation for the control room.



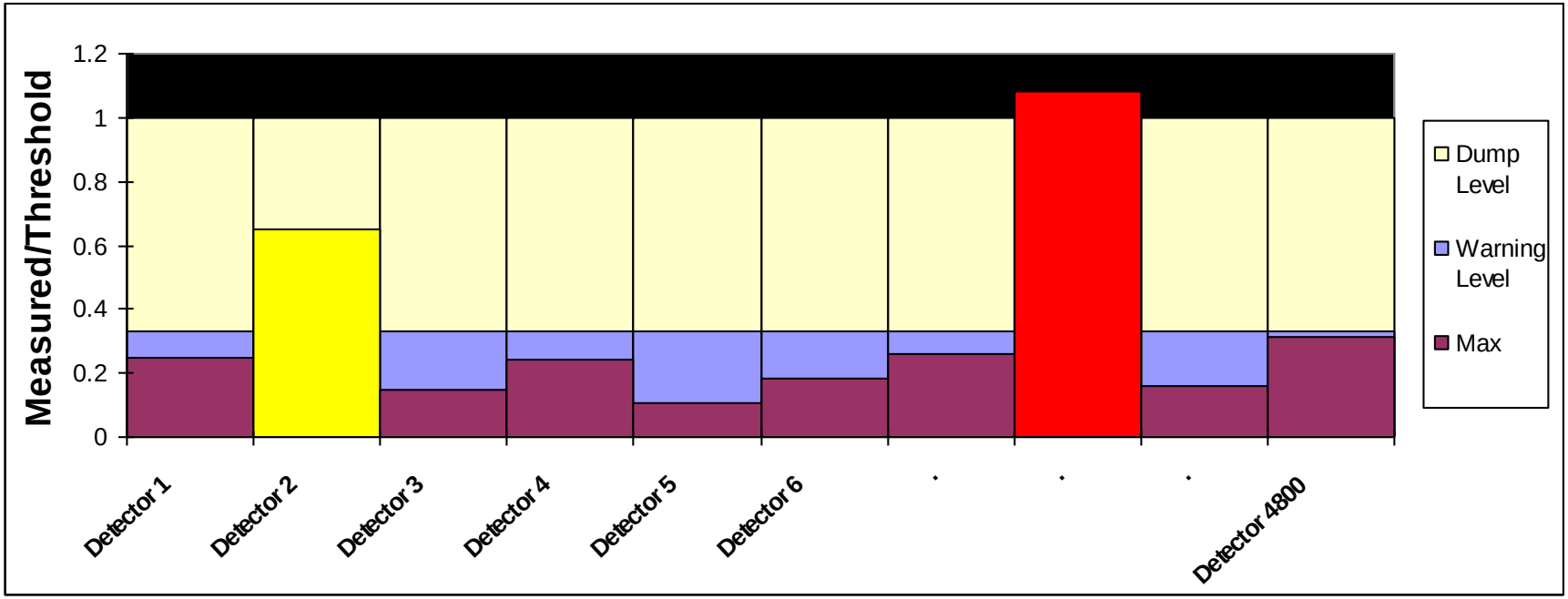
- The measured & calculated data. (480 Bytes)
- The max. values in the last second (480 Bytes)
- The used *Threshold* values. (480 Bytes)
- Additional info (card ID, status, errors) (~16 Bytes)

Total from each card ~ 2KB per second

- The card's *Threshold* table. (~ 29 KBytes)

Control Room Representation

The Control Room will be able to issue from logging data the Warning levels alerts and have a graphical representation which could look like:



The 12 values transmitted for each detector to the CPU will then have to be

- **normalised by their corresponding threshold value**
- **and from those the max value is displayed.**

Post Mortem Data Recording

- **Two circular buffers**
  - A. 2000 framewords (1000turns) of both signals received
  - B. Integrals of 10 ms (data useful for further analysis)
- **Double the above system and toggle between them using the stop PM recording trigger**
  - Never stop recording (i.e. avoid start input)
  - Test of PM will be possible anytime
  - Accidental/error-triggering proof
- **PM freeze from TTCrx through the backplane.**
- **Time-Stamp appended later by crate CPU.**
  - At PM freeze the CPU records the time and later when it reads the PM Data appends it to them.
- **Calculations:**

  1000 turns => 2000 acquisitions * ~250 bits frameword

  => ~ 60 KB/signal * 4 signals/card = 240 KB /card

  => 240KB/card * 16 cards/crate = 3.75 MB /crate

Summary

- Tunnel FPGA will be Actel's family SX/A with 208 pin sitting on a socket.
- Surface FPGA Altera's Stratix EP1S30 with 780 pin.
- All basic functions have been implemented.
- Test model of surface digital part is ready which uses:
  - Error checking of transmission.
  - Unique threshold table for each detector.
  - Averaging for longer running sums.

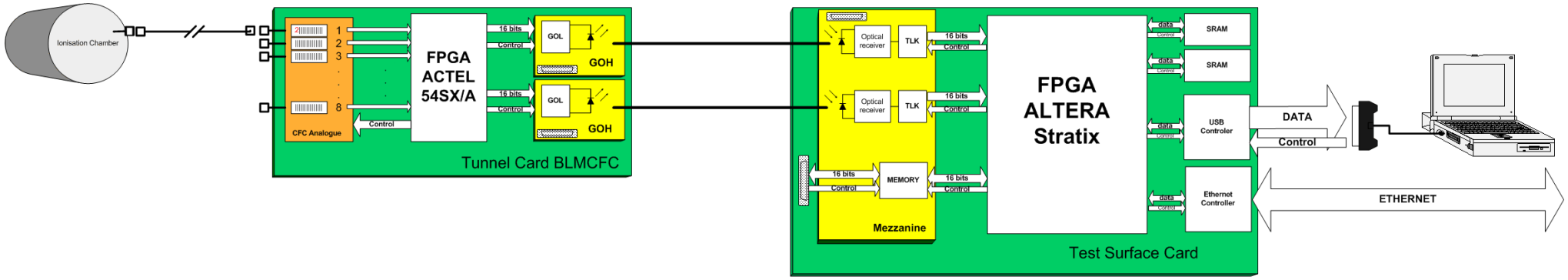
Next Steps

- Decide the communication link which will be used (will dictate the whole of the tunnel digital implementation and the rest of the surface part).
- Logging will be updated every second.
- PM will toggle between two buffers.

Other developments

Test acquisition card with PC link (Roman Leitner, Technical student)

- Tunnel system as it is.
- Same mezzanine with BLMTC.
- Propagate data via USB to a PC for further analysis and storage.



Tunnel ← → Surface

First use at DESY (Markus Stockner, PhD student)

- System test with circulating beam.