Status of CNGS hardware interlocking

- Introduction to the extraction interlock system
- Equipment interlocks :
  - Power converters & magnets
  - Target
  - Dumps
- Beam instrumentation interlocks
- Control issues
- Summary

Aim of this presentation

- Open issues.
- Identification of required links → cables - for B. Puccio

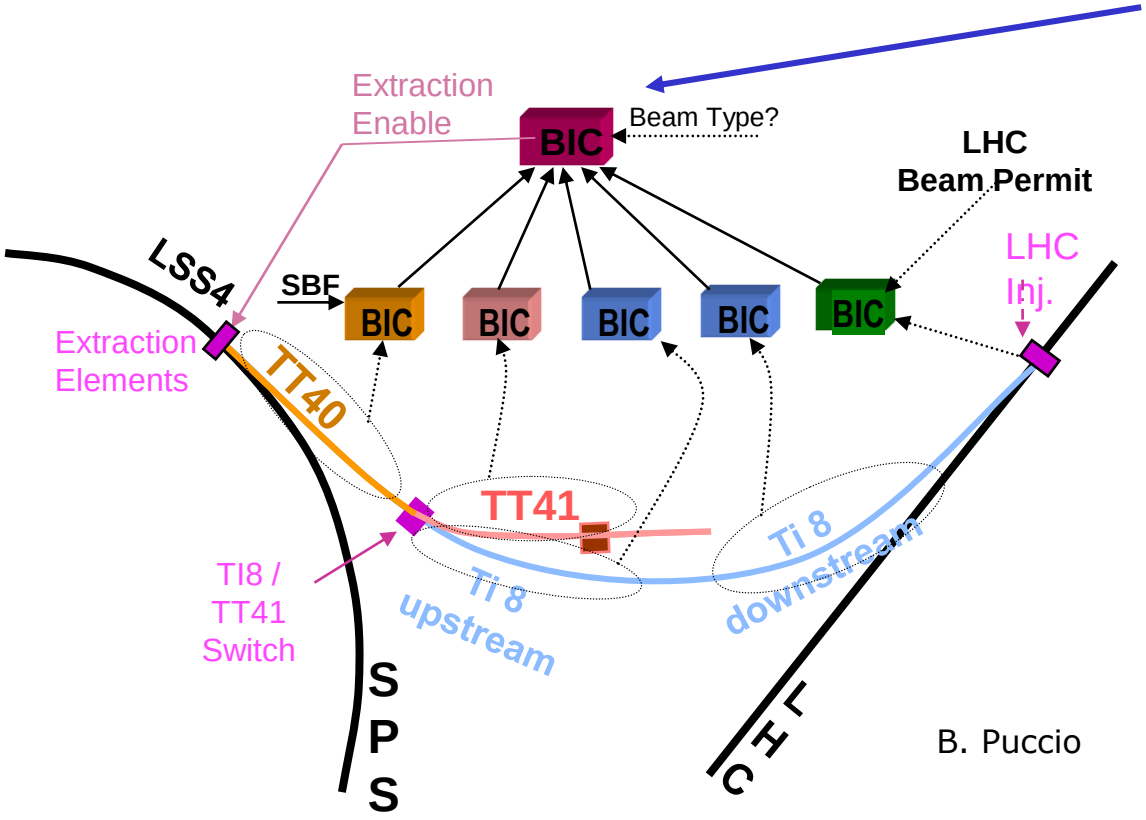
Beam Interlock Controller

The Beam Interlock Controller (BIC) is one of the core entities of the interlock system.

- The BIC module collects the *User-permit* (interlock) signals.
- Each BIC will have 16 inputs :
  - 7 **non-maskable** inputs. Always active
  - 7 **maskable inputs**, provided the SPS beam intensity is 'Safe' (< ~ 3 ×10^{12}). The 'Safe Beam Flag' is generated from the SPS BCT (implemetation still to be defined).
- A standard BIC provides one output corresponding to the logical *AND* of all inputs.
- Different BICs can be connected to each other by :
  - interlock loop (fiber optic link), used for the rings.
  - BIC output → BIC User-permit ('daisy-chain').
- BIC internal history buffer :
  - All transitions are logged and time-stamped (to the μs).
  - For the SPS, the start of the super-cycle is also recorded.
  - Possible extension : recording of the extraction pre-pulses → precise extraction time.

LSS4 extraction interlock architecture

- Architecture is sectorized to avoid (minimise) Xtalk between LHC and CNGS and allow flexible operation & setup.
- Each sector / zone controlled by one (or more) dedicated BIC.



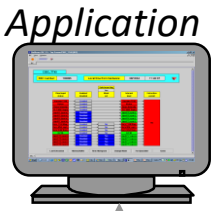
B. Puccio

A master module :

- receives the summary ouput signals from 'local' BICs.
- interfaces to the slow machine timing system (not yet defined!).
- performs the LHC / CNGS arbitration and sends **the extraction permit signal to the extraction kicker MKE in LSS4**.

Hardware for TT40/TI8 test

Courtesy
B. Puccio



Simplified layout of the installed material:

Control Network

VME crate with Lynx*OS*

PCs

BPM

BLM

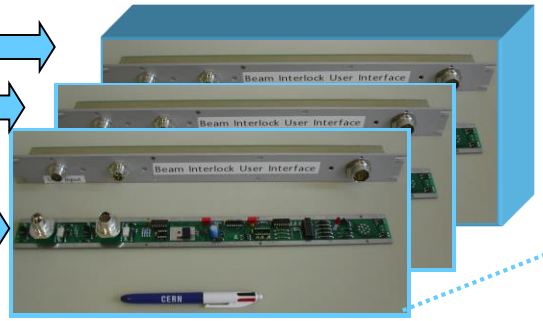
VAC

MKE

etc…

Extraction Enable

User Interface



User Interfaces

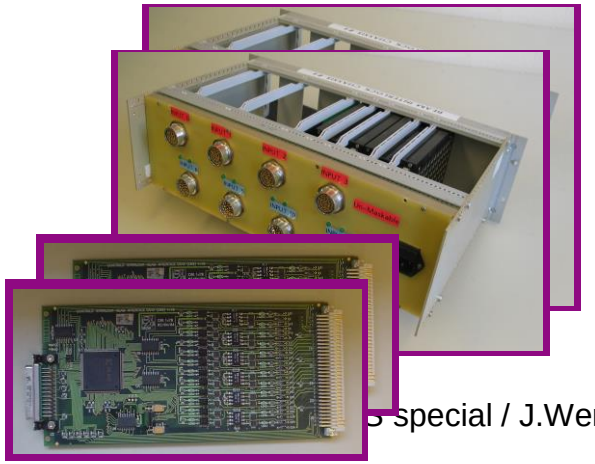
CPU + CTRP Modules

Patching modules

Core BIC modules

Optical module

to Extraction Kicker



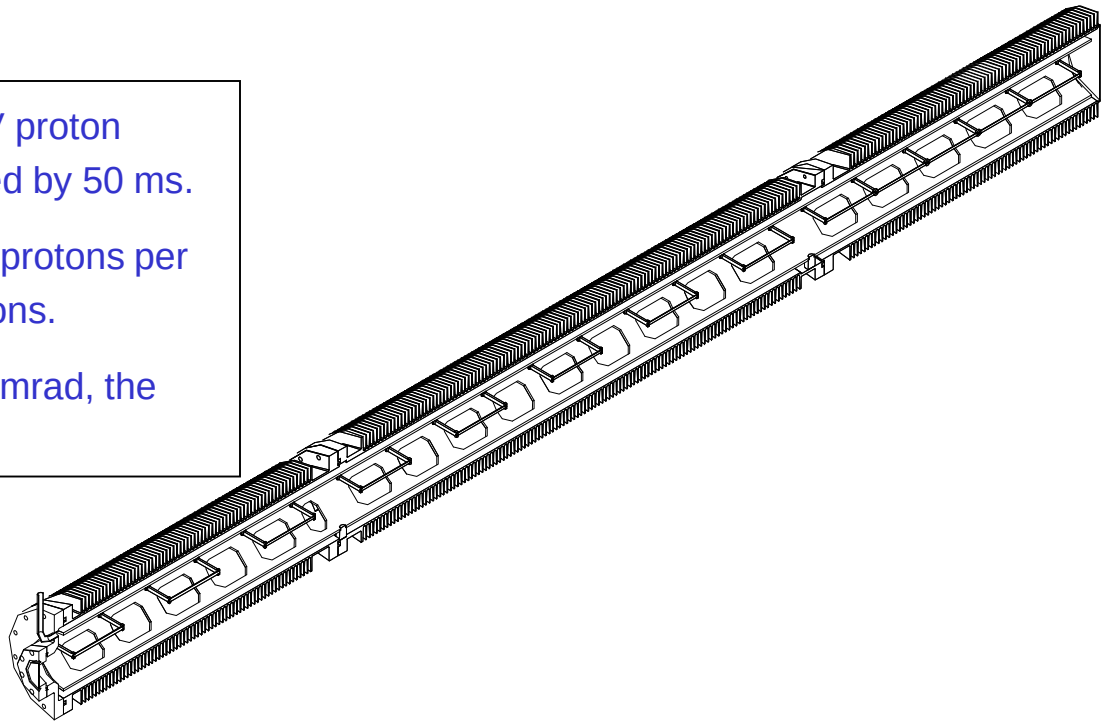
CNGS interlocking : aims

- Protection of the extraction channel and the transfer lines (TT40, TT41) – similar to the requirements for TI8 / LHC.
- Protection of the T40 target (and what is behind) :
  - At high intensity it is important to hit the target within 0.5 mm of the axis (target rod ∅ 4 & 5 mm) to avoid potential damage to the rods.

T40 intercepts a fast extracted 400 GeV proton beam with two 10.5 μs long spills spaced by 50 ms.

The nominal beam intensity is 4.8×10^{13} protons per cycle, the ultimate intensity 7×10^{13} protons.

The normalised emittance is ~ 12π mm mrad, the size is ~ 0.5 mm.



Interlocking issue

Interlocking of a fast extraction into a line is delicate :

- We must be sure *in advance* that all elements are at the right setting.
  - *Surveillance of critical HW settings → PCs !!!!!!*
  - *Interlocks are reset & re-evaluated for every cycle.*

- Beam instrumentation only gives *post-mortem information* !
  - *For CNGS we can however stop the second extraction.*
  - *We may latch (i.e. maintain) the interlock → blocks further extraction → manual reset.*

List of interlocked ‘elements’

Extraction channel & SPS ring :

- Beam position in extraction bump (M)
- Settings of orbit bumpers (M)
- Beam loss in extraction channel (M)

Interesting addition :

- Coarse energy interlock (CNGS,FT ↔ LHC)

Transfer line & target :

- Vacuum
- Extraction kicker
- TEDs & TBSEs
- CNGS decay tube shutter
- CNGS target assembly
- PCs (M)
- Magnets
- Horn
- Beam losses (M)
- Position at target, trajectory (M)
- Screen positions (M)
- Beam size ? (M)
- Hadron stop cooling

(M) = maskable

PC interlocking

Consequences on PC tolerances (dipoles) of **0.5 mm tolerance on the beam position at T40** :

Magnet	Location	Tolerance dB/B or kick	Time constant L/R (s)	Comment
MSE.418	Extr. / TT40	2×10^{-3}	0.022	
MBHA.4003	TT40	1×10^{-3}	2.61	
MBHC.4001	TT40	10^{-2}	1.01	changes angle
Main Bends	TT41	6×10^{-4}	1.03	
MBSG.4100	TT40/TT41	7×10^{-4}	1.05	switch to TT41/TI8
Hor. steering	TT40/TT41	10-12 μrad	≈ seconds	reaction time uncritical
Ver. steering	TT40/TT41	10-12 μrad	≈ seconds	reaction time uncritical

Much tighter than TI8 !

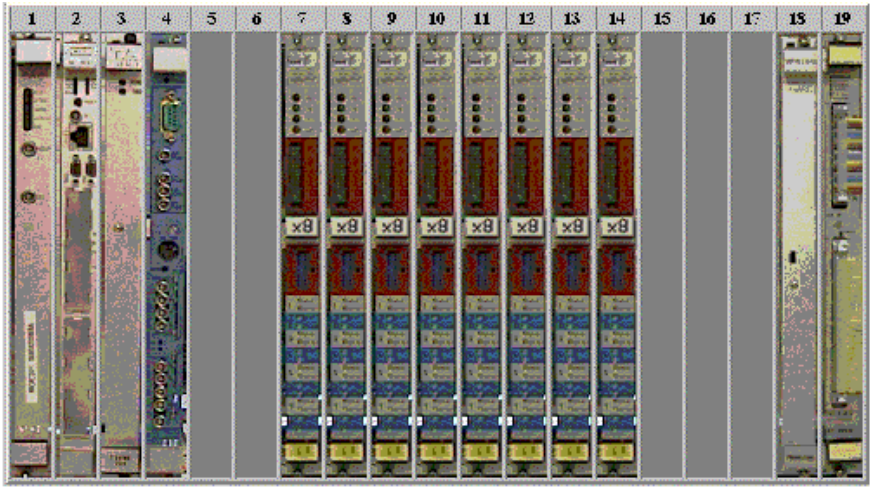
- For the dipole strings the tolerances are all at the 0.1% level – tough (time + ripple) !
- For orbit correctors one has to watch out during steering.
- Surveillance of

  wrong settings → *time un-critical !*

  failures → *time critical !*

PC surveillance - ROCS

The present PC surveillance is performed inside the ROCS system, a VME crate with PPC (lynxos), timing cards (TG8), ramp cards and ADC cards that controls a number of SPS PCs.



Interlock implementation:

- Timing interrupt (ms machine timing)
- Retrieve current measurement

  1 .. N ms-samples from continuous measurements: ***in 2004, 1 sample was finally used.***

- Average and compare if within tolerance with reference value for a predefined list of converters.

  OP tolerances in 2004 :

  - ***3 ×10^{-4}*** *on main dipoles and quadrupoles (3 converters).*
  - ***1-2 ×10^{-3}*** *on dipole strings, indiv. quadrupoles and bumpers (26 converters).*

- Generation of fast extraction permit (**FEI**) signal.

✓**Automatic removal of extraction permit after 1… 255 ms (was set to 20 ms in 2004).**

✓**Very efficient protection against wrong settings.**

! **Dead time (surveillance → extraction) : ~2-3 ms**

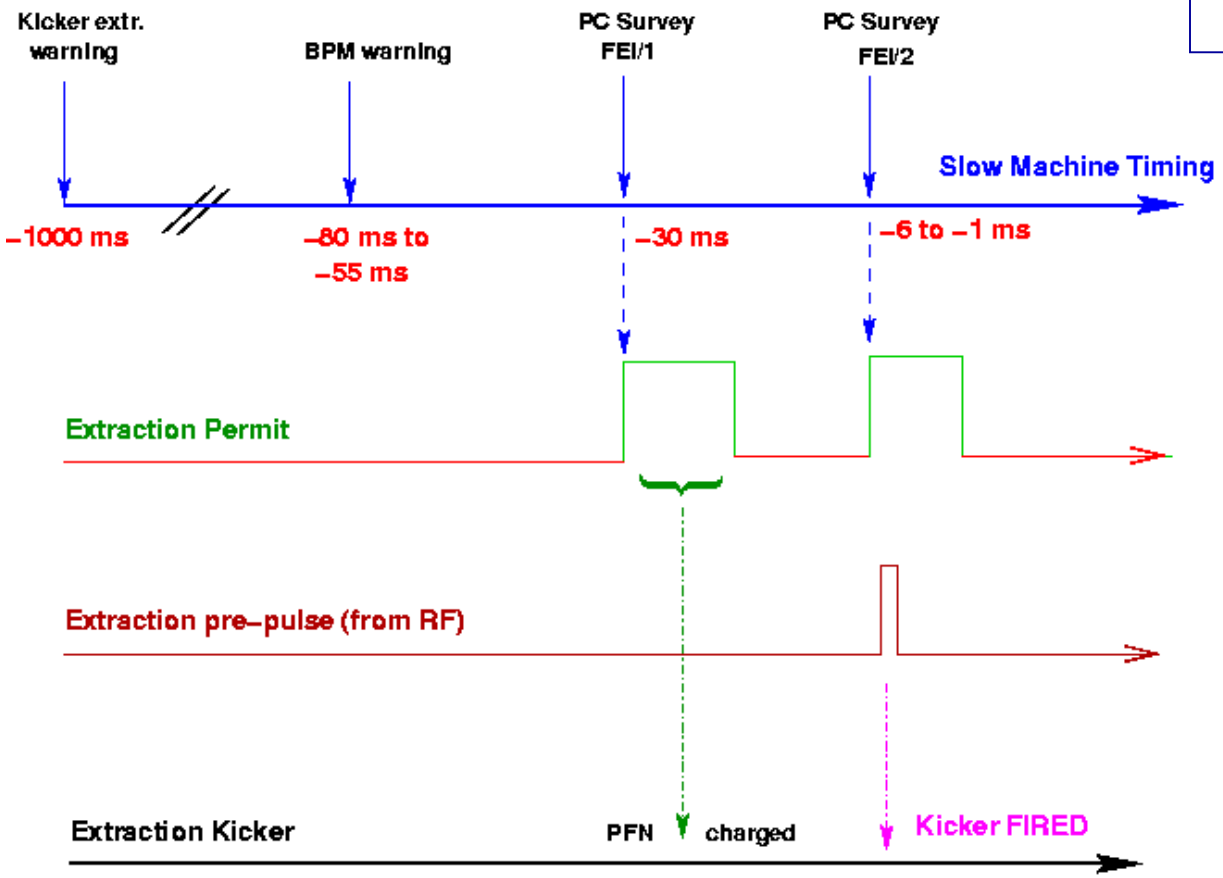
? **Operational issue : long term stability of ADCs, PCs, ripple ↔ achievable tolerances.**

Extraction & ROCs timing

The ROCs system gives 2 extraction permit signals :

- at t ≈ **extraction -25 ms** → PFN charging.
- at t ≈ **extraction -1 ms** → extraction trigger.

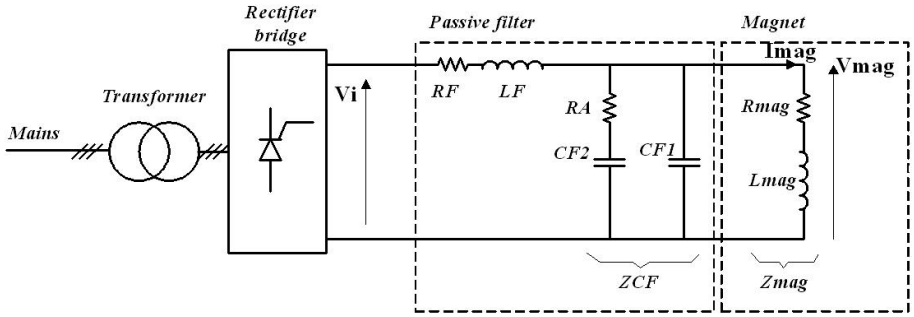
All interlock channels must give a "preliminary OK" at extraction – 25 ms for PFN charging.

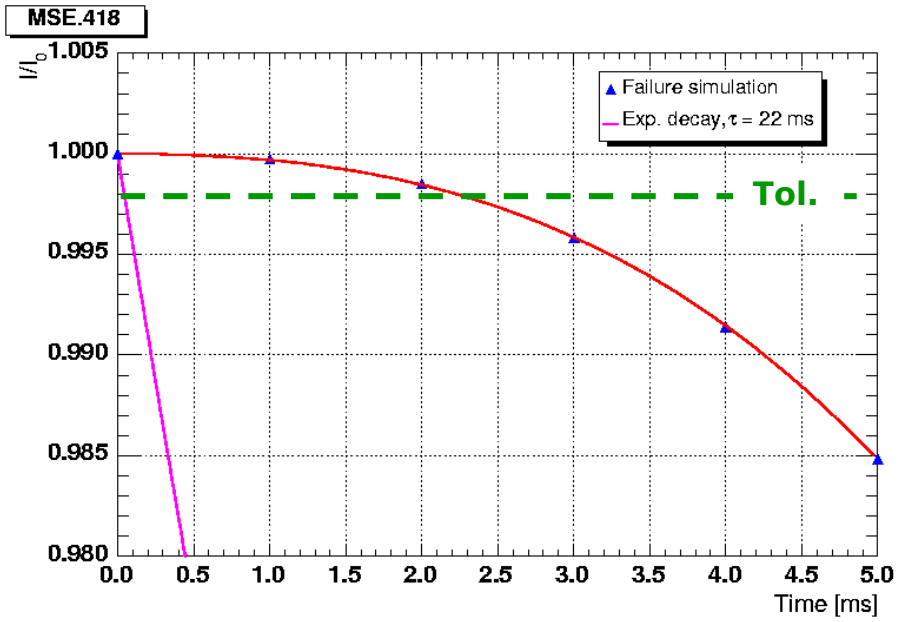


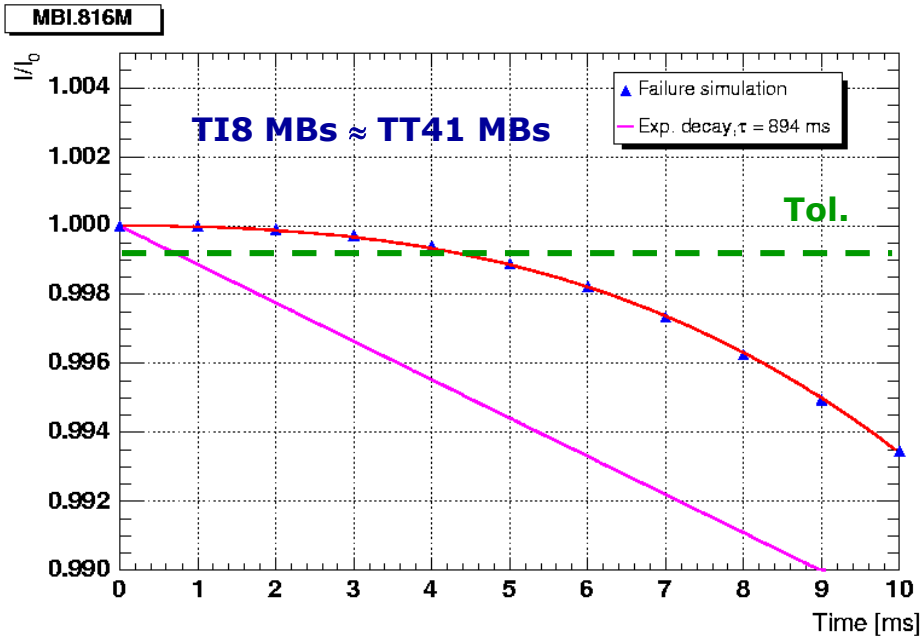
For CNGS this sequence is repeated twice (for each extr.)

PC failures – examples of simulations

The filter inside the PC has an important (and favourable) effect on the current decay just after the fault.

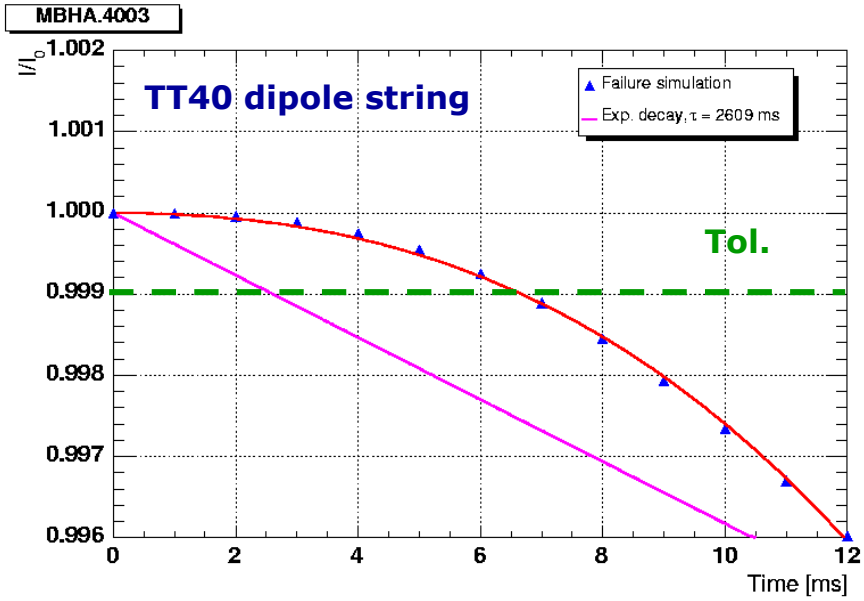


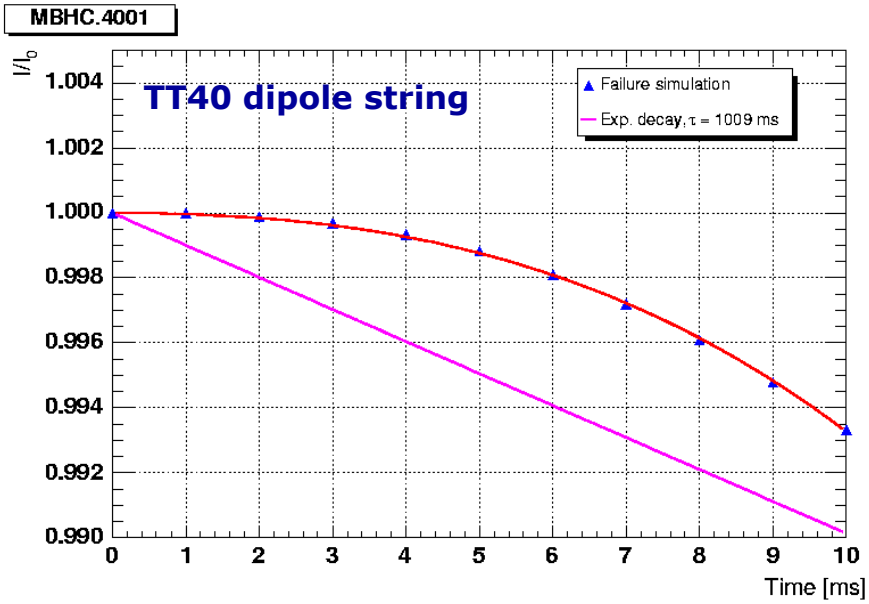


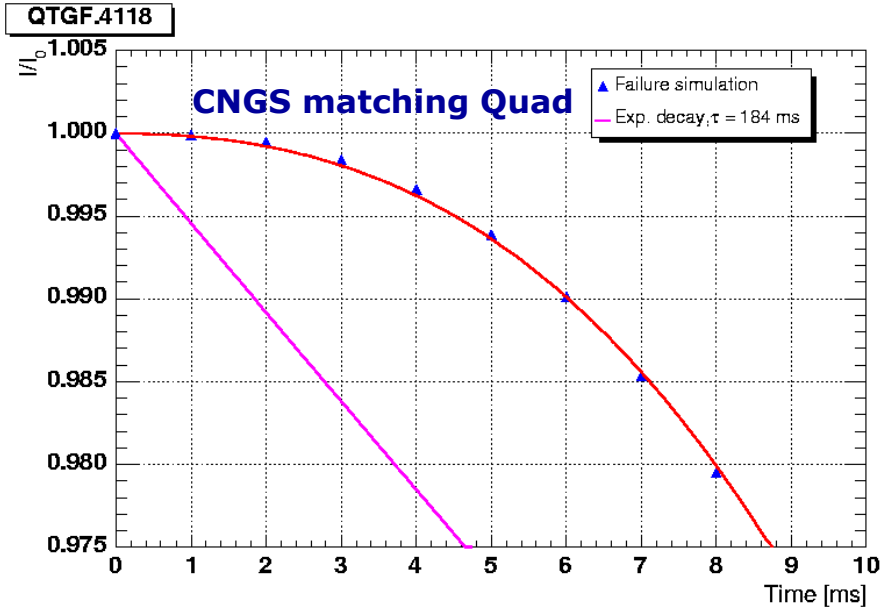


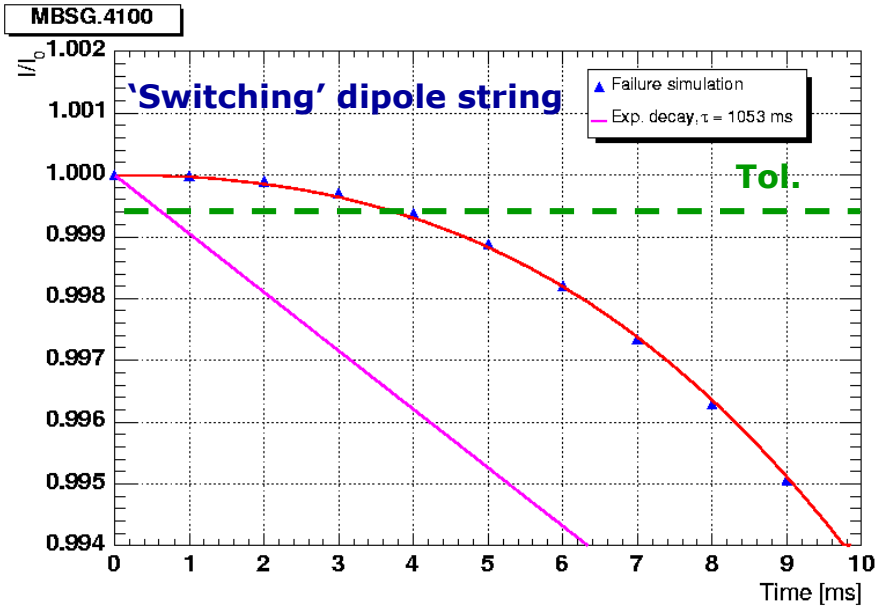
All simulations : courtesy C. De Almeida Martins (AB/PO)

PC failures – more examples









ROCS interlock performance

- The ROCS FEI provoque excellent protection against wrong trims/settings.
- From the simulations, despite the favourable effect of the filters, the FEI is not fast enough to provide full protection against PC failures.
- There are windows of a few milliseconds were a PC failure cannot be caught :
  - *MSE : in some cases the beam may only 'graze' the target.*
  - *Dipole strings : off-center impact ~ 1-2 mm or so.*

Can we do better for the critical circuits ?

➢ Direct interlock signal from the PC – would be excellent for internal faults.

➢ Fast detection of the decaying current by an external HW system.

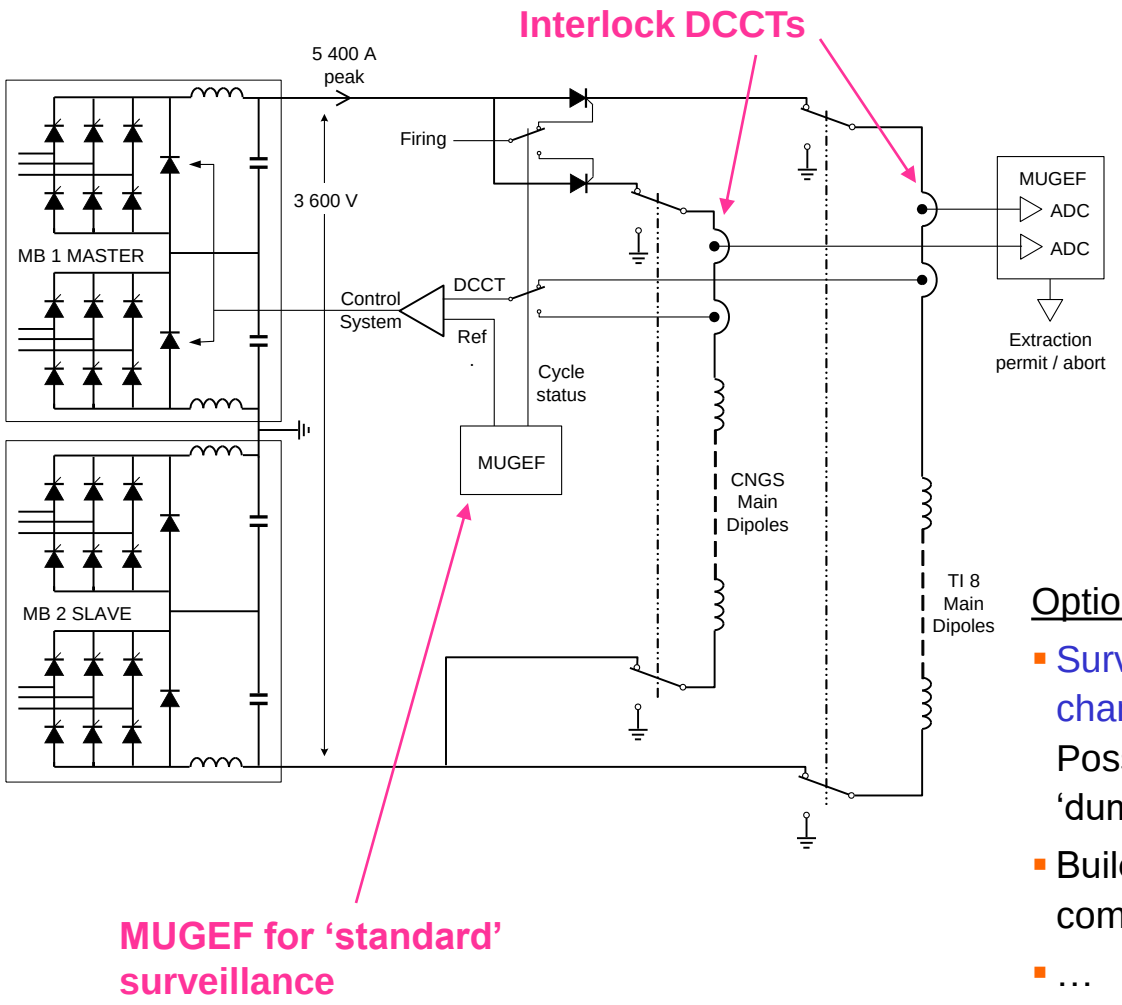
Both possibilities are being investigated….

Fast Current Decay Monitor

- The aim is to develop a system based on the detection of fast voltage changes that is able to reach detection limits on current changes of ~ 0.1% in 1 ms.
- Tests of a DESY system are ongoing… and seem very promising.
  - It seems one can react on current drops of ~ twice the PC ripple (low noise).

    → for the MSE which has the highest ripple (± 4 x 10^{-4}) → tolerance ~ 10^{-3}
- This system does not know the absolute current value, it is not a replacement for, but a complement to the ROCS interlock.
- When this system will be available, the following converters should be equipped:
  - *Extraction septum MSE.418*
  - *TT40 dipoles strings MBHA and MBHC.*
  - *The TT41/TI8 switch dipole string MBSG.*
  - *The TI8 and CNGS main dipole converters.*

Shared main dipole converter



- Former LEP main dipole converter, shared between CNGS/TI8.
- Electronic switching (2006 ?).
- 'Standard' surveillance of PC cannot resolve a switching error.
- **There is one DCCT in each branch that is 'reserved' for interlocking.**

Options for special DCCT surveillance :

- Survey each DCCT with a reserved MUGEF channel and use the standard surveillance. Possible, but PO does not really like such 'dummy' MUGEF PC channels.
- Build a 'low-tech' (no high accuracy needed !) comparator to check each DCCT against a ref.
- …

ROCS interlock list for CNGS/TI8 upstr.

Preliminary list ROCS FEI interlocks :

ROCS crate	PCs	BIC
m2sba4	orbit bumpers	TT40
m1sba4	TT40 circuits	TT40
	TI8 upstream circuits	TI8 upstream
	CNGS MB circuit	TT41
m1sbb4	septum MSE.418	TT40
	all TT41 circuits	TT41
	MBSG 'switch' magnet	TI8
m1sba4 ?	**MB - CNGS branch DCCT**	**TT14**
m1sba4 ?	**MB - TI8 branch DCCT**	**TI8**

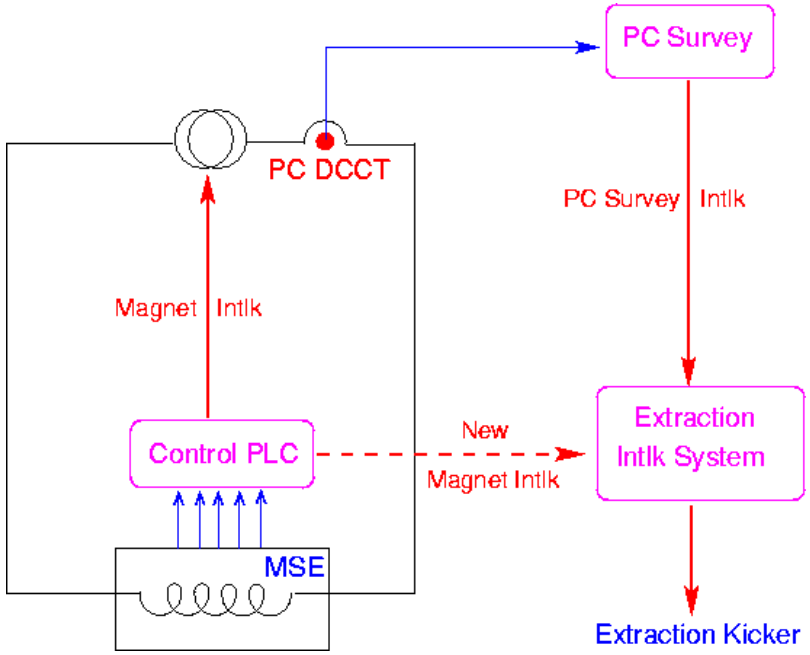
Prel. list FCDM / internal PC interlocks :

PCs	BIC
MSE.418	TT40
MBHA	TT40
MBHC	TT40
TI8 main dipoles	TI8 upstream
TT41 main dipoles	TT41
MBSG dipole	TT41

Special channels, to be confirmed !

Magnet interlocks

- MSE magnet surveillance :
  - ✓ Direct interlock signal from the PLC that surveys the septum to the TT40 BIC. This interlock is sent out 10 ms *BEFORE* the MSE PC is stopped.
  - ➢ The absence of this link was (one of) the reason why we made the hole in TT40.
- Warm Magnet Powering Interlock (WIC) system :
  - ➢ This PLC-based system surveys all the magnets (temperature…) of TT40, TT41 and TI8.
  - ✓ A direct link to the BIC system is used to stop the beam a few ms before any PC is stopped.



Magnetic horns

- Interlock if not ON – not maskable.
- Interlock signal is provided by PH/DT1 group.
- Expert masking of this interlock is required for the early setting up.
- So far – so good !

Target T40

ATB will provide two interlocks.

- Interlock No. 1 / non-maskable :
  - Target magazine rotation (no beam when magazine is moving!)
  - Target air-cooling system
  - Target cap shielding position interlock
- Interlock No. 2 / maskable :
  - Target table position.
  - No “target" position.
- Issues :

  ATB rack is in TSG4 – long long cable….

Safety elements : TBSE / Shutter

- Both the TBSE (personnel protection dump) and the shutter must be OUT of beam before beam operation starts.
- ATB will provide a signal that sets an interlock when the elements are not OUT.
- There will be one signal / element (2 TBSEs [TI8,TT41], 1 shutter).
- Issues :
  - *For the shutter the rack location is in TSG4 – long cable.*
  - *Same issue than for T40.*
  - *VME crate with a BIC + fiber link ? Or 3 long cables ?*

TED dumps / I

For each TED dump the following permit signals must be provided

1. ‘TED-in’ signal
   - *TRUE ONLY if TED is IN-BEAM.*
   - *FALSE in all other conditions (OUT, moving, intermediate…).*

   Used to mask interlocks arising from equipment **DOWSTREAM** of the TED.
2. ‘TED-not-moving’ signal
   - *TRUE if TED is IN-BEAM or OUT-BEAM.*
   - *FALSE in all other conditions (moving, intermediate).*

   Used to inhibit the beam in the region **UPSTREAM** of the TED.
3. ‘TED-out’ signal
   - *TRUE ONLY if TED is OUT-BEAM.*
   - *FALSE in all other cases.*

We need either 2. or 3., still under discussion, probably 3.

TED dumps / II

- For extraction, the TED may be IN or OUT, since both are SAFE positions.
- Software interlocks will be used to handle inconsistent TED positions by checking the consistency between
  - The **beam destination** (beam-to-TED, beam-to-target, beam-to-ring1…) as distributed by the timing system and set in the timing sequence

  and
  - The **actual TED position**

  as is already the case today. A SW interlock (that can be bypassed to allow fast checks…) is generated in case of inconsistency.

Hadron stop cooling

- The cooling circuit of the hadron stop must be interlocked by HW.
- This interlock is critical for safety, but is not time-critical ~ seconds.
- Issues :
  - The pumps are installed in the TI8 alcove TE80 near the downstream end of TI8, which complicates the cabling.

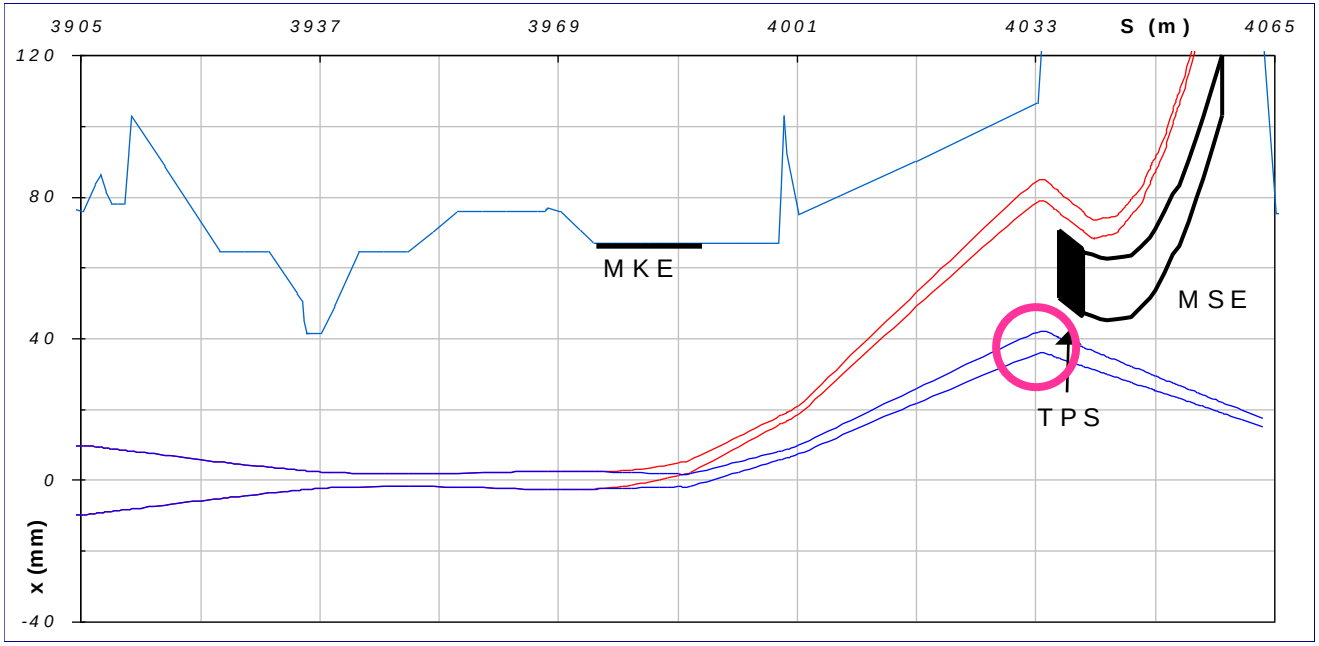
Beam diagnostics interlocks

- General principle :
  - ✓ All beam diagnostics interlocks are maskable for safe beams.
- Extraction channel interlocks :
  - The BLM interlock is connected to SPS ring beam dump system (we need to dump if there are losses on the circulating beam).
  - Intlk on beam position at extraction point is connected to the extraction interlock system.
- Transfer line interlocks :
  - Interlocks act only after an 'incident', for CNGS we can prevent the 2nd extraction.
  - Should interlocks be…
    - ***latched*** *(→ no more beam until there is a reset by an operator) ?*
    - ***reset for next cycle*** *(default) ?*
    - ***if latched, who is responsible for latching ?***
      - *SW interlock system ? Should in case foresee this option…*
      - *BIC system, user (BDI) ?*

Bumped beam position

- The beam position at the extraction point (monitor BPCE.418) is interlocked.
- The beam is not extracted if the position is not within ± 0.5 mm (LHC beam) of the reference.
- This interlock is not latched – checked before every extraction.
- Possible issues :
  - *Intensity dependence and stability of BPCE response (observed in 2004).*
  - *Tolerance of ±0.5 mm : also OK for CNGS ?*

  Should be since 0.5 mm at β = 100 m (BPCE.418) → < 0.2 mm at target.



Extraction / TL stability

- The TI8 tests revealed that the extraction + TT40 + TI8 are very stable :
  - *RMS stability << 0.2 mm for β=100 m (measurements dominated by BPM noise of 0.2 mm).*
  - *Dominated by MSE ripple of ± 4 ×10^{-4} (peak-to-peak).*
  - *Good start for CNGS…*

- Due to the sensitivity of the beam position at the target on corrector magnet kicks, steering will be delicate at high intensity and corrector strengths must be interlocked. This will complicate the steering (feedback or not) – need experience to define best strategy !

- Do we need interlocks on the overall trajectory in the line or do we rely on BLMs to tell us when we get too close to the aperture ?

Beam position at target

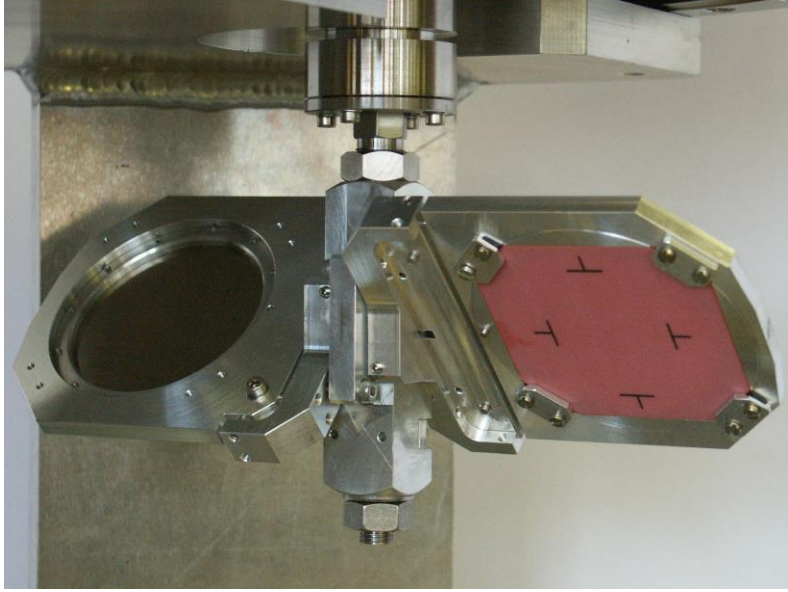
Interlock on beam position at T40 target :

- Tolerance ± 0.5 mm in both planes.
- To enhance the reliability → use all 3 BPMs in front of T40.
- Flexible configuration :
  - *accommodate changes based on OP experience.*
  - *foresee the possibility for voting (2 out 3 BPMs…)..*
- The ACQ system is being developed – interlock implementation is not a problem.

BLMs

- The BLMs of TT40, TT41 and TI8 upstream will be distributed over two VME crates (so far one) to allow a full segmentation by lines.
- THREE interlocks signals will be generated for TT40, TT41 and TI8-upstream.
- As long as there is no latching – no coupling problem :
  - *Interlock on the LHC beam is 'useless' since it comes too late.*
  - ✓ *Interlock on the first CNGS extraction prevents the second extraction.*
  - ✓ *No interference because interlocks are reset (in BLM system) at every cycle start.*
- With latched HW interlocks :
  - *Even with the 3 separate BLM signals, losses in TT40 will lead to coupling.*
- Issues :
  - *Is latching by SW interlock good (safe) enough ?*
  - *If not : who is responsible for latching ?*
    - *BIC ? → 1 additional BIC for each line (+ possibly additional VME crates).*
    - *BLM system ?*

Screens I : mechanics



A screen in the transfer lines is SAFE for :

- *OUT position.*
- *OTR (Ti/12 μm or C/100 μm) position.*

An interlock is generated if :

- *Screen is in AlO (thick screen) position.*
- *Screen is moving.*

The interlock will be maskable with Safe Beam Flag.

- The interlock is generated directly from the FPGA that controls the screen motor.
- One (or more, tbc) interlock signal will be given for each VME crate.
- The command to move the screens is always given in the period of the SPS cycle without beam : normally the beam should never intercept the frame of the screen !
- Issue :
  - *Two screens from upstream part of TI8 are mixed with TT40 screens in the same VME crate.*
  - *Is it worth splitting them off ? Do we leave them in one channel – very small probability of coupling LHC-CNGS…*

Screens II : size interlock

- To be avoided : too small beam sizes (for high intensity !).
- The implementation of an interlock is tricky → Ana's presentation.
- Sources of size reduction :
  - Emittance : excluded

    The emittance will not shrink 'by miracle', except if the intensity drops (~constant brilliance) – but that's no problem.
  - Optics : reduction of β
    - SPS ring : ~impossible since tunes are kept constant and are stable to << 0.01.
    - TL : since PCs are surveyed (including the quads), a reduction of β can come through
      - a wrong manipulation where a quad setting + tolerance are changed.
      - a problem on a magnet (inter-turn short)
      - an accidental change of β is likely to be asymmetric between H and V (i.e. one β grows, the other shrinks…) → should help ?

Extraction kicker & beam dump

- Only the extraction kicker system can know rapidly and for sure if the beam was kicked or not…. The interlock system does not have enough information.
- I propose that the extraction kicker generates beam dump signals (→ SPS beam dump) whenever the extraction is '*abnormal*' :
  - First CNGS batch not extracted :
    - → dump beam in SPS.
    - → empty PFNs with clipper or through the kicker magnets (in the beam-out segment) ?

    We loose a batch, but we are safer…
  - LHC beam not extracted and PFNs charged
    - → dump beam in SPS.
    - → empty PFNs through the kicker magnets in the 'beam-out' segment. No clipper.

    Gives a 'symmetric' handling of LSS4 (clipper switch) and LSS6 (no clipper).

Interlock settings

- The LHC and CNGS TL interlock system involves many threshold, reference and tolerance dependent interlocks.
  - *PCs : reference currents & tolerances.*
  - *BLMs : thresholds.*
  - *BPMs : reference positions & tolerances.*
- Presently those settings are not managed :
  - ‘*everyone’ can change values,*
  - *No history of changes.*
- Aim for 2006 :
  1. *priority : implement a trim system (+ history of changes) for interlock settings.*
  2. *priority : provide reasonable ‘protection’.*

Controls, OP, post-mortem

- With very high intensity, both for CNGS & LHC, we need diagnostics in case of problems.
- BDI data, PC currents and the complete interlock information are stored on the logging DB on a cycle-by-cycle basis.
- BDI data and BIS info may also be displayed on ‘fixed displays’ / applications.
- Logging and displaying all of this is good, but may not be sufficient !
- For example, for latched BDI interlocks, we must decide on how to proceed :
  - *try again with one extraction ? Maybe it was an erratic interlock…*
  - *switch back to low intensity and check everything (1 hour min ?).*
  - *…*

  → *need sufficient and easily accesible information !*

Interlock diagnostics

- Interlock from a static equipment (vacuum, dump, target…) :
  - *Fast diagnostics from the interlock system application.*
- Interlock from a 'dynamic' equipment – power converter :
  - *Rough diagnostics from the interlock system application.*
  - *Due to grouping of PCs into one signal, detailed info must be obtained from*
    - *the **logging system**.*
    - *the status information available within the ROCS crate (expert-ish !).*
- Latched interlock from BDI (position, BLMs) :
  - *Diagnostics with the intlk. system application.*
  - *Only **logging data** (since there is no more beam !!) can be used to understand what happened !*

Since we cannot always extract data manually from the DB (time !!), we need a tool :

- *to extract ALL relevant data for a selected cycle.*
- *to compare the data with a reference.*

~ ONLINE cycle-by-cycle Post-mortem

Summary : issues & questions

- Power converter interlocks :
  - To reduce the dead time of the present ROCS-based interlock system we need a new fast current decay monitor (FCDM) system and/or an internal PC interlock: 3 additional systems are needed for CNGS in addition to LHC requirements (main bends, MBSG, MBHA).
  - Shared converter for CNGS / TI8 dipoles : implementation to be defined.
  - In 2006 more experience concerning stability is needed to define tolerances on correctors.
- Beam diagnostics interlocks :
  - **To latch or not to latch by HW. Latching by SW interlock is always possible.**
  - Beam size interlock → A. Guerrero.
- Cabling :
  - **How do we cable/connect the signals from TSG4 and from TE80 (cooling) ?**
- Controls :
  - Interlock settings, post-mortem analysis.
  - The new SW interlock system will hopefully be 'usable' for summer 2006.
  - Lot's of work on that front.

Estimated cost for interlocking TT41

Item	Nbr	U.P. (in kCHF)	Total
VME system installed in BA4 (Power Supply, CPU module with Lynx*OS* included)	**1**	**15**	**15**
Beam Interlock Controller (Core module + Monitoring card + SBF interface + Patching card)	**2**	**6**	**12**
Connection with equipment systems (User Interface unit with ~200m of cupper cable)	**13**	**3**	**39**
Long connection with system in TSG4 (User Interface unit with 800m of cupper cable)	**3**	**9**	**27**
Very long connection with system in SR8 (Special Interface unit using fibre optics)	**1**	**10**	**10**

Total: 103 kCHF

#	Interlock Name	Comments
1	TT41 vacuum valves	
2	TT41 PCs & magnets	ROCS surveillance for TT41 PCs (MB +Q +Correctors)
3	Magnetic Horns	including cooling water
4	Warm Magnets Interlock	WIC gives 3 separate signals (TT40, **TT41** & TI8)
5	Screens	
6	TBSE TT41 (as TBSE410113)	Signal TBSE is IN or moving (=unsafe) or OUT (safe)
7	TT41/TI8 position of main bends	possibly special ROCS ?
8	TT41 beam losses (latched signal)	
9	Beam Position (latched signal)	
10	MB current monitoring	ROCS surveillance of shared MB ROCS
11	FCDM in TT41 (1of2)	Fast Current Decay Monitoring / MBSG
12	FCDM in TT41 (2of2)	Fast Current Decay Monitoring / Main bends
13?	Beam Size?	Sw Interlock or Hw Interlock?
14	ή Target T40 (1of2)	Non Maskable signal from PLC managing Target's interlocks
15	ή Target T40 (2of2)	Maskable signal from PLC managing Target's interlocks
16	Shutter	Unsafe if not OUT position. (cooling water signal included?)
17	Hadron stop cooling -	Pumping system installed in SR8

in TGS4

in SR8