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the **Large Hadron Collider** project

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Functional Specification

INTERLOCKING BETWEEN SPS, CNGS, LHC TRANSFER LINES AND LHC INJECTION

Abstract

This document specifies the detailed beam interlocking requirements of the SPS to LHC transfer lines, the CNGS transfer line and the LHC injection systems. The required operating modes and associated interlock conditions are described and a possible interlock architecture outlined. The document specifies the general performance requirements, the interlock conditions for the various elements and the acceptance tests, commissioning steps and maintenance requirements.

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Interlock requirements defined with VK, RS, JW

Conceptual aspects already discussed with BP; proposal for architecture….

Many useful comments incorporated (visible in EDMS comment collector if anyone is interested).

Here present main features, plus some unresolved issues

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Main features

- Based on previous work on extractions, transfer lines and injections (RS, JW, et al.)
- Added dedicated LHC injection BIC
- Added concept of Injection Permit
- Complex logic remains in SPS extraction BIC only
  - OR logical conditions
  - Timing and cycle awareness
  - Safe beam and beam presence conditioning
- Require LHC beam permit to inject any beam
- Require LHC beam presence for high intensity

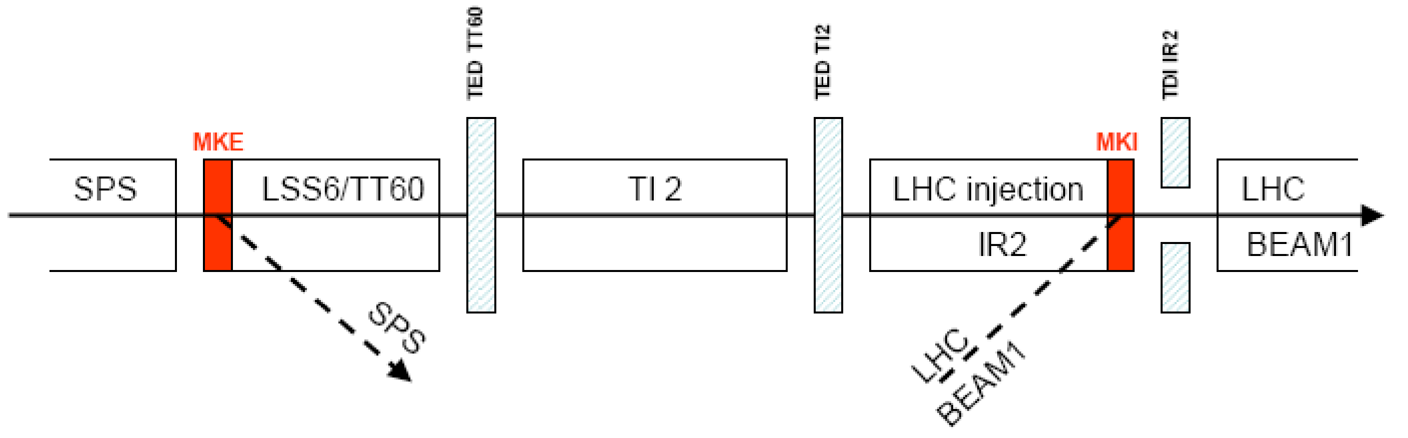
Specification includes:

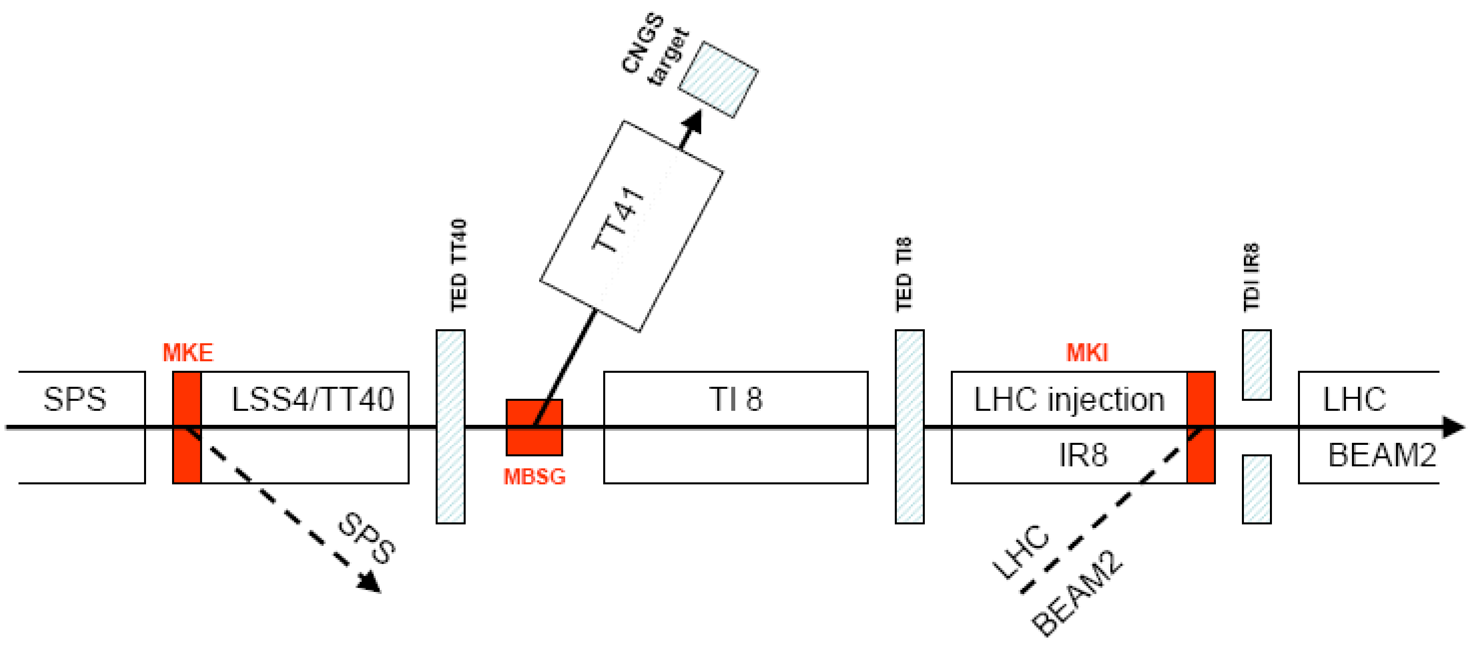
- Concepts
  - Operational modes
  - Truth tables
- Proposed architecture
  - Number and type of BICs
  - Signal exchange
    - From equipment to BICs
    - Interchange between BICs
    - SLP to BICs
- Interlock classes
  - Types of input and approximate numbers
  - Tolerances

Interlocks classes

- ROCs surveillance (all PCs)
- PC fast sum fault (new: ~10 PCs)
- FMCCM (new: ~10 PCs)
- CNGS target
- Screen positions
- Protection devices (TEDs, TCDIs, TDIs, ...)
- Extraction / injection equipment (kickers, septa)
- Beam instrumentation (BLMs, BPMs, BCTs)
- Vacuum valves
- LHC experiments
- Software channels

Segmented system





Based on truth tables for different allowed 'modes'

Inputs	User permits			Dumps					SPS/LHC					Output	
	1	2	3	4	5	6	7	8	9	10	11	12	13	1	2
Mode	LSS6 extraction/TT60 user permits	TI 2 upstream and downstream user permits	LHC IR2 injection user permits	TED upstream 'IN beam'	TED upstream 'OUT of beam'	TED downstream 'IN beam'	TED downstream 'OUT of beam'	TDI / TCLI in 'PROTECT' position	LHC beam permit	LHC beam presence flag	LHC safe beam flag	SPS safe beam flag	LHC beam type (timing signal)	SPS LSS6 extraction permit	LHC IR2 injection permit
1. Beam to LSS6/TT60 TED	1	x	x	1	0	x	x	x	x	x	x	x	x	1	0
2. Beam to TI 2 TED	1	1	x	0	1	1	0	x	x	x	x	x	1	1	0
3. Low intensity beam to LHC	1	1	1	0	1	0	1	x	1	x	x	1	1	1	1
4. High intensity beam to LHC	1	1	1	0	1	0	1	1	1	1	0	x	1	1	1

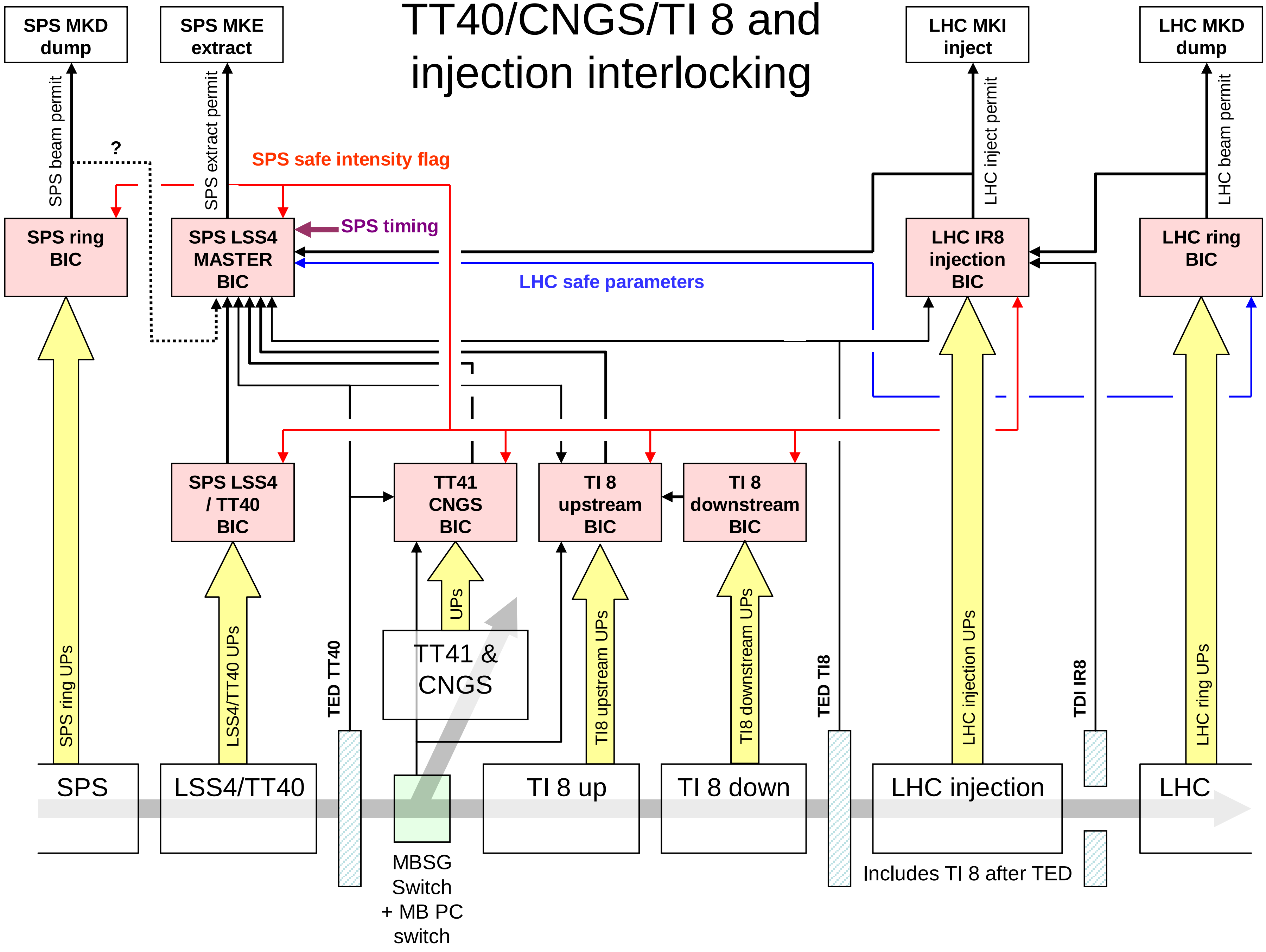
LSS6/TT60/TI 2/IR injection

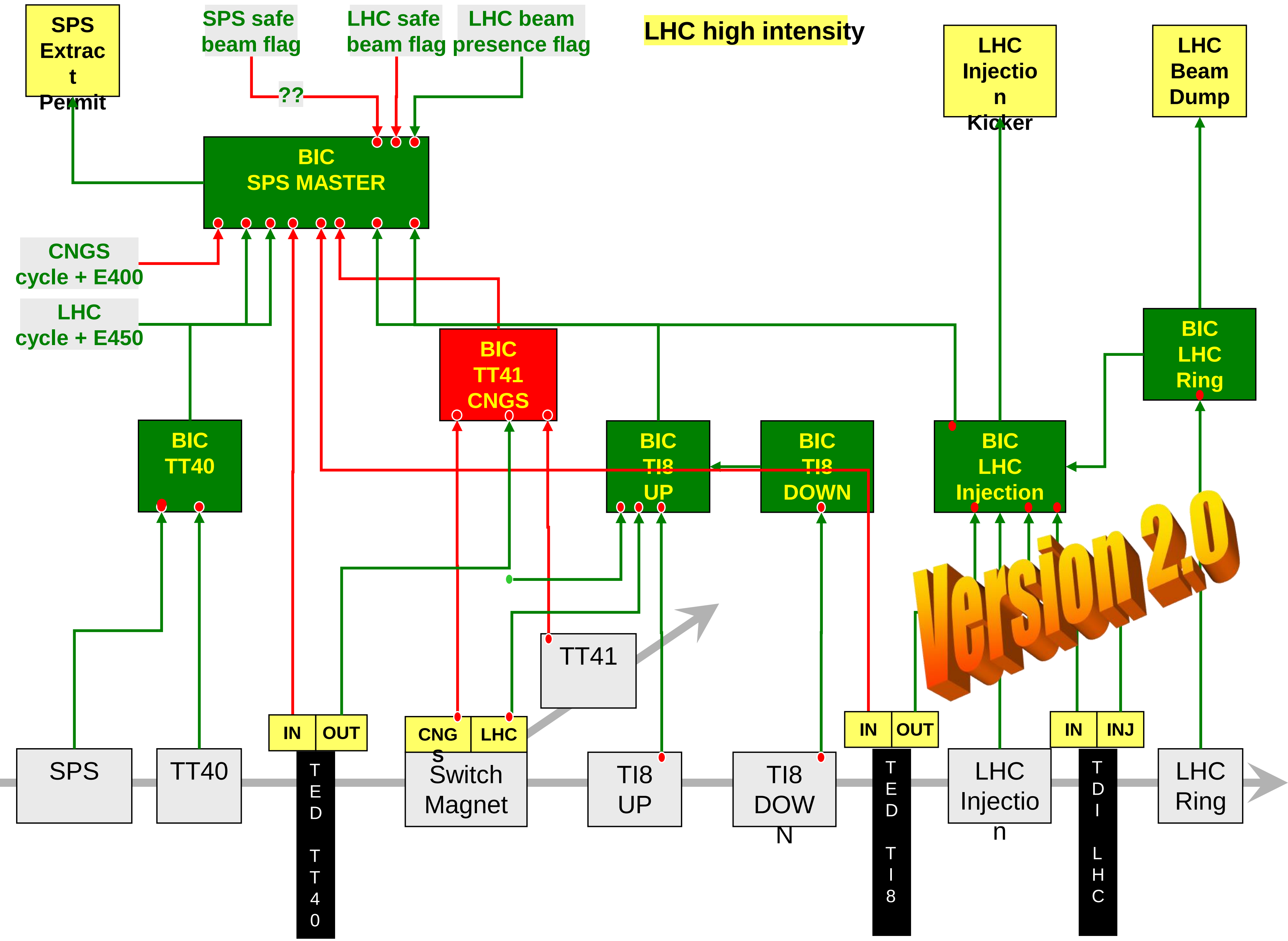
Based on truth tables for different allowed 'modes'

Inputs	User permits				Dumps					SPS/LHC						Output	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	1	2
Mode	LSS4 extraction/TT40 user permits	TT41/CNGS user permit	TI 8 upstream and downstream user permit	LHC IR8 injection user permits	TED upstream 'IN beam'	TED upstream 'OUT of beam'	TED downstream 'IN beam'	TED downstream 'OUT of beam'	TDI / TCLI in 'PROTECT' position	LHC beam permit	LHC beam presence flag	LHC safe beam flag	SPS safe beam flag	LHC beam type (timing signal)	CNGS beam type (timing signal)	SPS LSS4 extraction permit	LHC IR8 injection permit
1. Beam to LSS4/TT40 TED	1	x	x	x	1	0	x	x	x	x	x	x	x	x	x	1	0
2. Beam to TI 8 TED	1	0	1	x	0	1	1	0	x	x	x	x	x	1	0	1	0
3. Low intensity beam to LHC	1	0	1	1	0	1	0	1	x	1	x	x	1	1	0	1	1
4. High intensity beam to LHC	1	0	1	1	0	1	0	1	1	1	1	0	x	1	0	1	1
5. Beam to CNGS	1	1	0	x	0	1	x	x	x	x	x	x	x	0	1	1	0

LSS4/TT40/TT41/TI 8/IR 8injection

TT40/CNGS/TI 8 and injection interlocking





SPS Extract Permit
SPS safe beam flag
??
LHC safe beam flag
LHC beam presence flag
LHC high intensity
LHC Injection Kicker
LHC Beam Dump
BIC SPS MASTER
CNGS cycle + E400
LHC cycle + E450
BIC TT41 CNGS
BIC LHC Ring
BIC TT40
BIC TI8 UP
BIC TI8 DOWN
BIC LHC Injection
Version 2.0
TT41
IN
OUT
CNGS
LHC
IN
OUT
IN
INJ
SPS
TT40
TED TT40
Switch Magnet
TI8 UP
TI8 DOWN
TED TI8
LHC Injection
TDI LHC
LHC Ring

Tolerances for warm magnets – ROCS surveillance

Family name	Description	# Circuits	Imax A	tolerance ΔI/Imax
MBB	TT60 dipole	1	7500	0.001
MBG	TT41 main dipole	1	5400	0.001
MBHA	TT40 dipole	1	1100	0.001
MBHC	TT40 dipole	1	1000	0.001
MBI	TI 2 / TI 8 main dipole	2	5400	0.001
MBIAH	TI 8 dipole	1	1000	0.001
MBIAV	TI 2 / TI 8 dipole	4	1000	0.001
MBIBH	TI 2 dipole	1	800	0.001
MBIBV	TI 8 dipole	1	800	0.001
MBSG	TI 8 / CNGS switch	1	4400	0.001
MCIAV/H	TI 2 / TI 8 corrector	88	3	0.1
MCIBH	TI 8 dipole	1	400	0.001
MDAV/MDLH/MDLV	TT60 corrector	4	300	0.1
MDGV/MDGH	TT41 corrector	12	3	0.1
MDSV/MDSH	TT40 / TT41 / TT60 dipole	6	400	0.001
MPSH/MPLH	SPS H extraction bumper	8	400	0.001
MPSV/MPLV	SPS V extraction bumper	8	120	0.001
MQI	TI 2 / TI 8 main quadrupole	34	600	0.001
MSI	LHC injection septum	2	1000	0.001
MST	SPS extraction septum	1	7500	0.001
MSE	SPS extraction septum	2	24000	0.001
QTG	TT41 main quadrupole	8	500	0.001
QTL/QTM/QTR/QTS	TT40 / TT41 / TT60 quadrupole	16	500	0.001

FMCM – PC sum fault

Family name	Description	# Circuits	# PC 'Σ fault'	# FMCCM	ΔI/Imax	Δt ms
MBB	TT60 dipole	1	1	1	0.001	1
MBG	TT41 main dipole	1	1	1	0.001	1
MBHA	TT40 dipole	1	1	1	0.001	1
MBHC	TT40 dipole	1	1	1	0.001	1
MBI	TI 2 / TI 8 main dipole	2	2	2	0.001	1
MBIAH	TI 8 dipole	1	1	1	0.001	1
MBIBH	TI 2 dipole	1	1	1	0.001	1
MBSG	TI 8 / CNGS switch	1	1	1	0.001	1
MSI	LHC injection septum	2	2	2	0.001	1
MST/MSE	SPS extraction septum	3	3	3	0.001	0.05

Testing procedures: outline

7.7 LHC SUPERCONDUCTING MAGNETS AND OTHER SYSTEMS

The superconducting DC magnets in the injection regions will be surveyed by the LHC PIC and BIS. This, together with the LHC beam presence condition, is deemed adequate for protection of the LHC at injection.

8. TESTING, COMMISSIONING AND MAINTENANCE

For the interlock system, with the complex multi-cycling aspects and numerous user inputs, a critical process will be the system commissioning. System tests must be performed for every SPS super-cycle before it is used for regular operation, both with and without beam.

The logic relies on the LHC beam permit as an input; this signal cannot be forced or simulated, and so special testing procedures must be developed in conjunction with the tests of the LHC BIS. Testing of the input from the SPS timing system will also need to be made, to verify that the mode dependency works correctly.

8.1 TESTING WITHOUT BEAM

After the interlock system has been installed and the hardware commissioning is completed, a series of acceptance tests without beam can be performed. A detailed test programme must be formalised in advance, including the test procedures, details and acceptance criteria. This test program should be constituted such that every critical element and every critical path in the decision logic is at least tested once. Critical questions must be addressed concerning how to test the system when the LHC Beam Permit is one of the inputs, when the timing is an input channel, and when all possible combinations of the "Master" BIC must be checked. The tests without beam should include:

- Application software functionality and acceptance tests;
- Logging and post-mortem functionality and acceptance tests;
- Individual BIC logic outputs (matrices) for possible input combinations, to fully test the OR logic needed in the special extraction BIC;
- Failsafe behaviour at different levels, by unplugging connectors, supplies etc.;
- User permit masking and unmasking with Safe Beam flag;
- Signal exchange between BICs;
- Signal exchange between user inputs and BICs;
- SPS safe beam flag and LHC beam presence flag signal transmission;
- Extraction/injection permit signal exchange between BICs and MKE/MKI;
- Individual user permit signal generation;
- Individual user permit settings management;
- Software channels;
- Cycle-dependent individual user permit reference settings;
- Extraction/injection permit synchronisation with SPS timing system;
- Full tests of all user permit signals which do not rely on the beam;
- Full system tests to check the effects of each user permit and input;
- Full system tests with a multicycling (interleaved beam) configuration;
- Full system tests for switching between FT, CNGS, LHC and interleaved beam;
- Full system tests to check synchronisation aspects and signal latency;
- Switching between different pre-defined modes for setting-up and filling (including bump polarity changes).

8.2 TESTING WITH BEAM

When beam is available, a series of additional tests with beam are required at an early stage of each step in the commissioning process. The detailed test requirements must be formalised in advance, taking into account the beam intensity steps, and including the test procedures, details and acceptance criteria. The tests with beam should include:

- Application software functionality for beam-related parts;
- Logging and post-mortem functionality for beam-related parts;
- EMC related tests;
- Acceptance tests of SPS Safe Beam system (generation, thresholds, ...);
- Individual user permit signal generation for beam related parts;
- Cycle-dependent individual user permit reference settings for beam related parts;
- Extraction/injection permit synchronisation with extracted / injected beam;
- System response to kicker failure modes;
- Full tests of all user permit signals which rely on the beam;
- Full system tests with multicycling (interleaved beam) configuration;
- Full system tests for switching between FT, CNGS, LHC and interleaved beam;
- Full system tests to check synchronisation aspects and signal latency;
- Functionality with injection sequencer for LHC filling;
- Calibration with beam of reference settings.

8.3 FUNCTIONALITY NEEDED FOR LHC BEAM COMMISSIONING PHASES

For the sector test planned at the start of LHC commissioning in late 2006, the full interlock system functionality should be available. This will prevent any danger associated with trying to 'stage' such a critical machine protection system. In any case a sub-set of the system is needed for the sector test, to ensure that only Safe Beam can be injected into the LHC.

8.4 MAINTENANCE POLICY

The lifetime of the system is estimated at 20 years. A maintenance policy must be developed taking into account expected component lifetimes and failure modes, and also as a result of the BIS dependability studies. Failures that do not result in a loss of functionality (for example of the monitoring part of the system) must be detected and lead to the execution of a maintenance procedure. The maintenance must be performed before any beam operation can be allowed, in order to come back to the required SIL level. In addition, regular preventive maintenance of the most critical components may be required, and should be defined and implemented in the overall policy.

9. OTHER INTERLOCKING

9.1 SOFTWARE INTERLOCKING CHANNELS

The present SPS software interlocking system must be upgraded for the LHC era and extended to the transfer lines. The software interlocking for the LHC will be an important aspect of the machine protection. Presently no specification exists of the detailed requirements or implementation for either machine, nor for the lines. It is expected that the software interlocking for the extraction, transfer lines and injection will use the solution

Main implications

- **Hardware**
  - 2 more BICs (1 per injection)
  - Downstream TED status to extraction BIC - cables
  - LHC SLP signals to SPS extraction BIC – cables
  - 2 HW position signals from TDI (retracted, protect)
- **Operation**
  - LHC beam permit always required for beam past downstream TED, irrespective of MKI and TDI state
    - no dedicated setting up mode – need safe beam mask
    - Cannot set up injection during LHC down time
- **Safety**
  - SPS Safe Beam Flag has to be safe (no redundancy in interlocks when setting up TDI)
    - SIL level estimate needed – being addressed in MPWG

Remaining issues/concerns

- MKE/MKI resonant charging + extraction permit
  - Double gate used presently for MKE
  - Not adapted to MKI – another approach?
- Details of segmentation in injection regions
- Finalise extraction kicker fault cases and actions
  - Missing, erratic, link to SPS dump, …
- SPS safe beam flag generation and reliability;
- Safe setting management for references and tolerances in the equipment front-ends;
  - SSM concept and scope…
  - Multi-cycling aspects of references in some front-ends (BPCE, MKE, …);
- Adaptation and extension of existing software interlock system (SSIS);
- Reference values and tolerance windows for corrector magnet settings.
- …