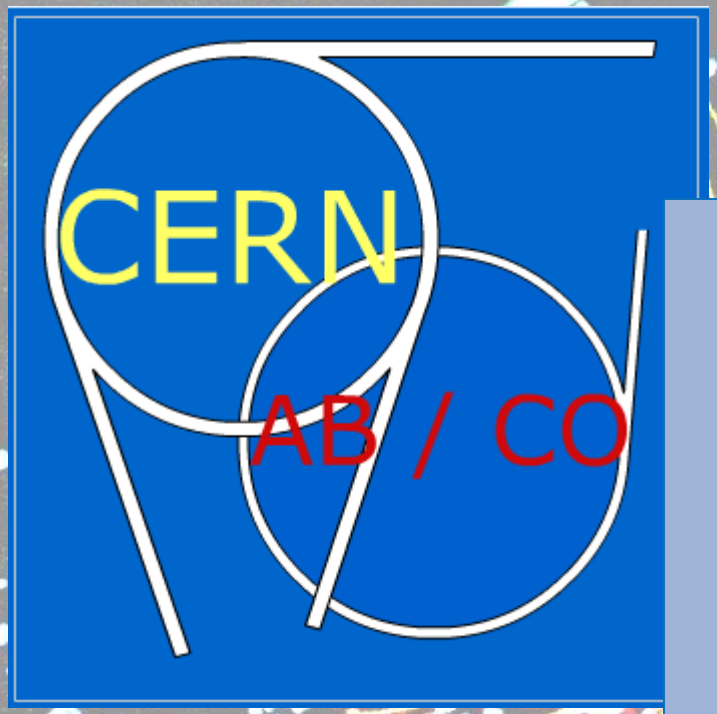

Commissioning and Testing the LHC Beam Interlock System

MPWG – 2nd September 2005

Testing and Commissioning

1. System Overview
   - Beam Permit Loops
   - Beam Interlock Controllers
   - User Interfaces
2. Testing and Commissioning Methods
   - Overview
   - Phase I Testing – Stand Alone Controller Level
   - Phase II Testing – Full Controller Level
   - Phase III Testing – System Level
   - Phase IV Testing – Machine Level
3. Summing Up
   - Open Questions

System Overview

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Beam Permit Loops

Beam Interlock Controllers (BIC)

16 BICs
- Two at each Insertion Point

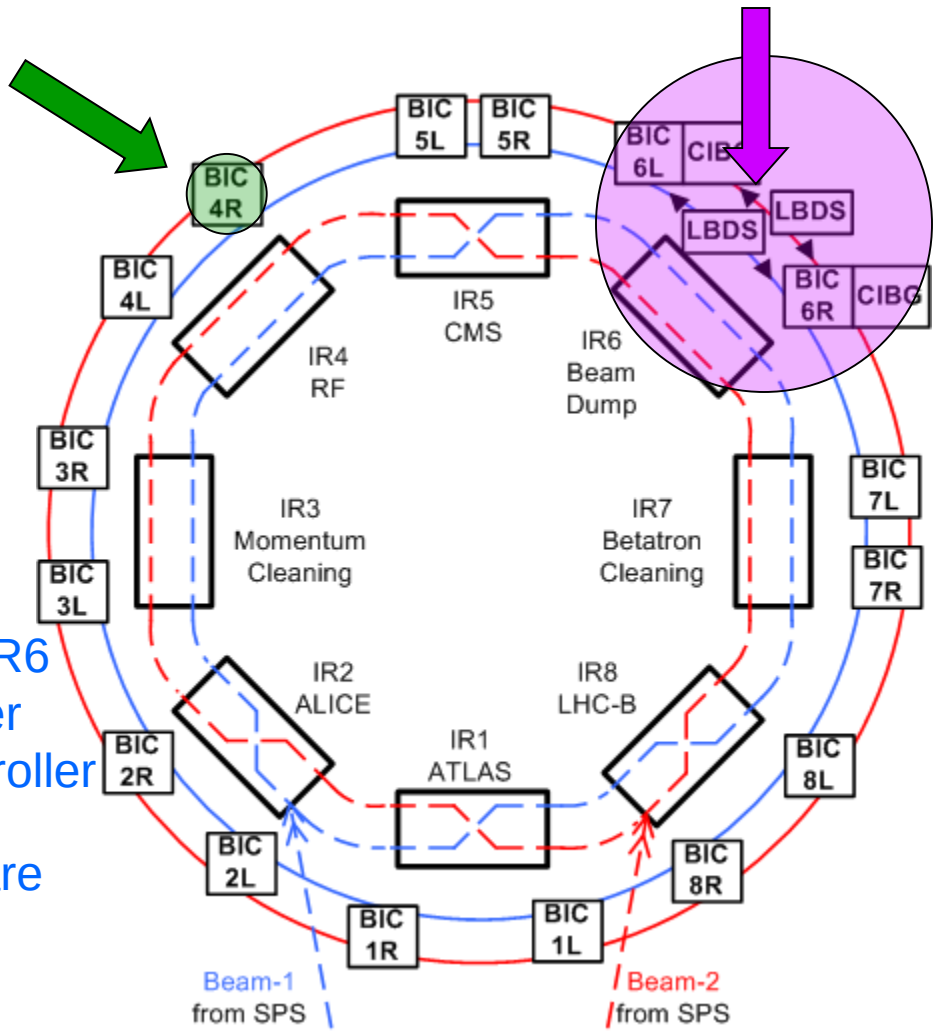
Up to 20 User Systems per BIC
6 x Beam-1
8 x Both-Beam
6 x Beam-2

4 fibre-optic channels from Point 6
1 clockwise &
1 anticlockwise for **each** Beam

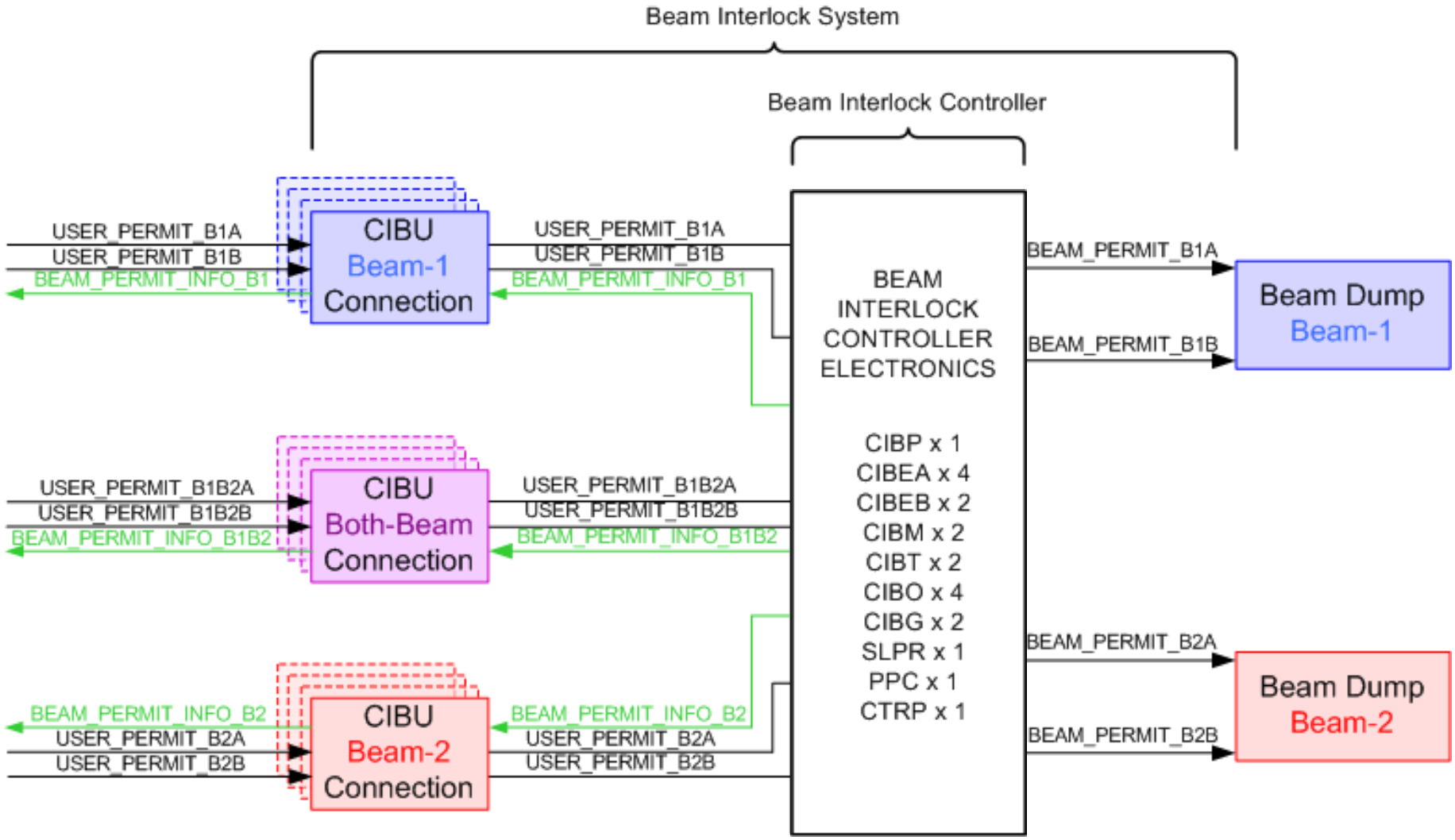
10MHz Square wave generated at IR6
-Signal can be cut by any Controller
-Signal can be monitored by any Controller

When any of the four 10MHz signals are absent at IP6, BEAM DUMP!

Beam-1 / Beam-2 are Independent!



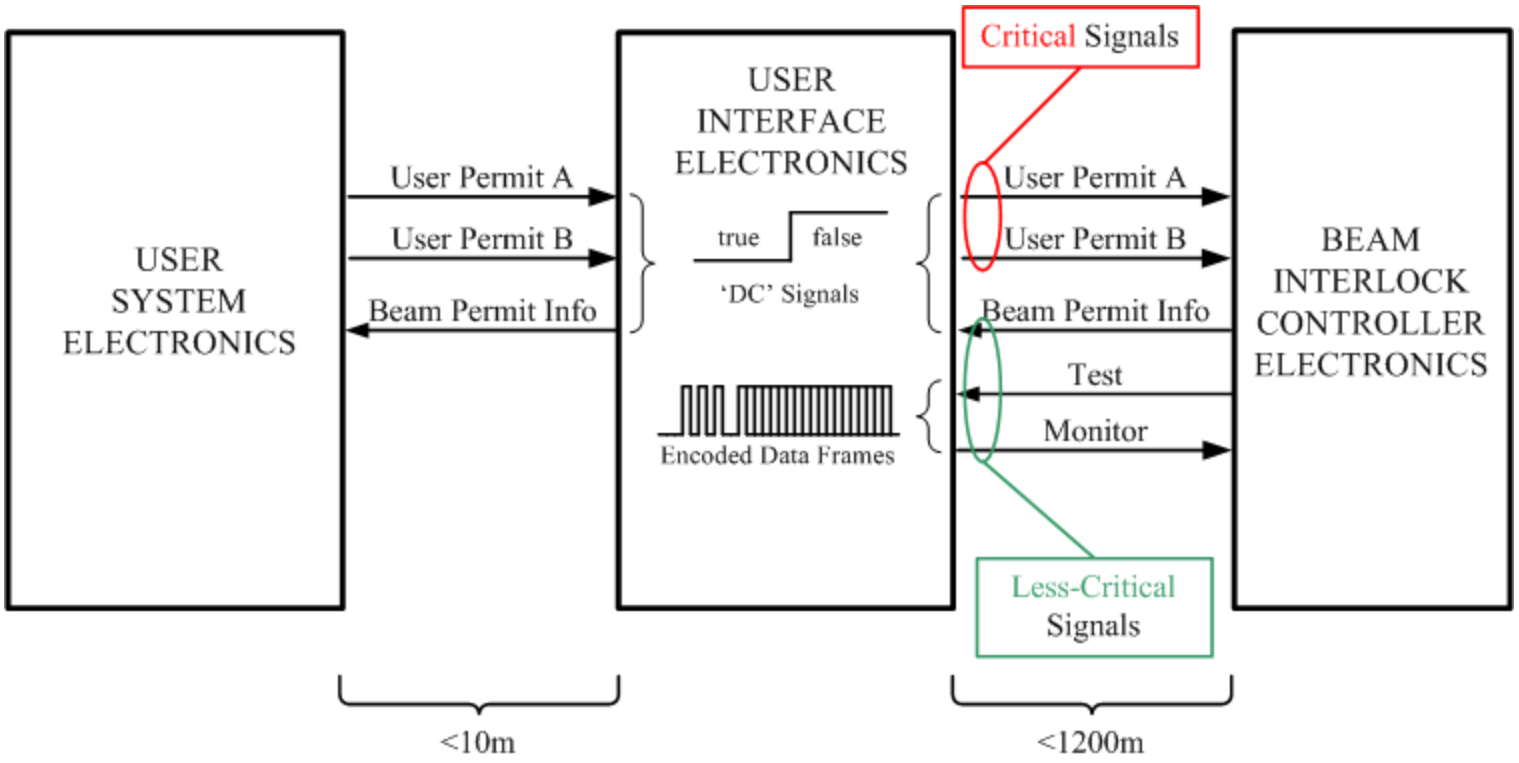
Beam Interlock Controllers



Based on VME – Has a *few* sub-components

all needs to be completely tested!!

User Interfaces



All links designed to be almost 100% testable from end to end of BIS
Using Built-In Test Mode
BUT we need to test the cable to the User System to cover 100% of the system

Methods

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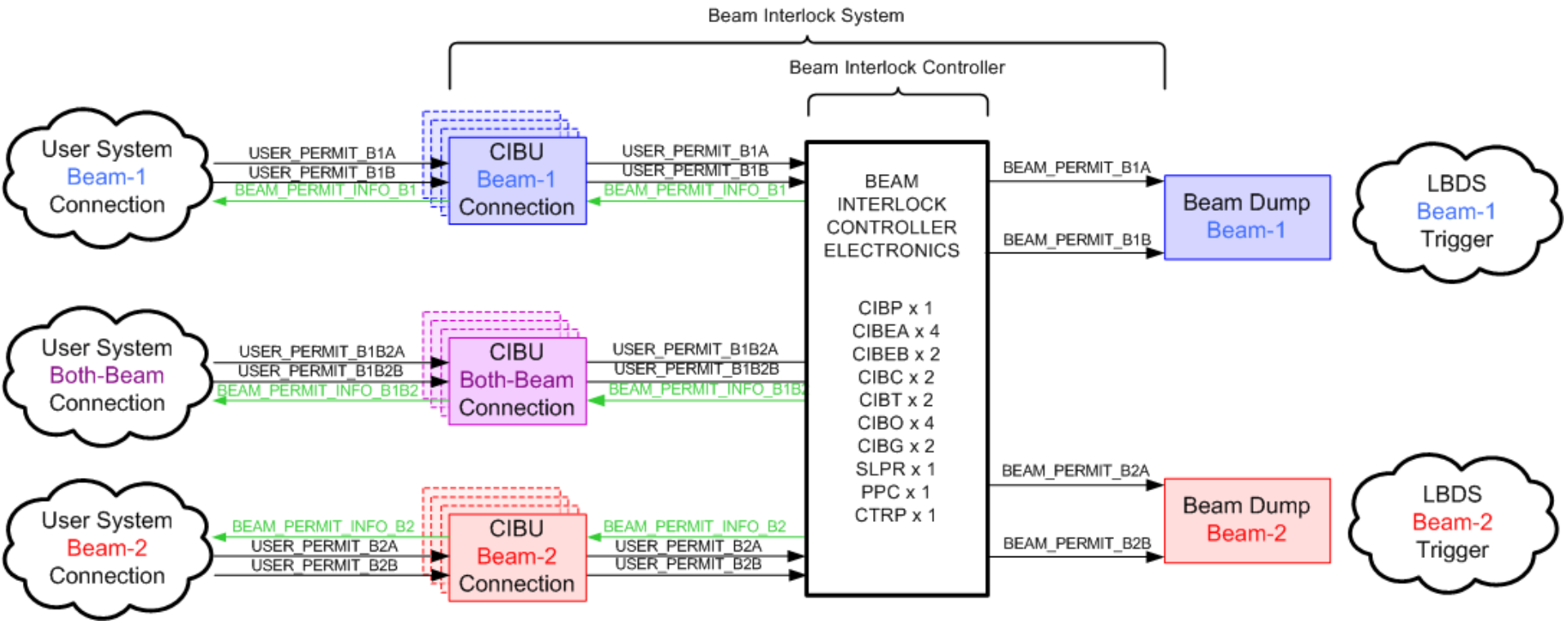
Testing and Commissioning Overview

Need to verify the integrity of the complete Beam Interlock System
Both In Lab & In LHC
Both With & Without User Systems

Using ideas from Felix (see MPWG #46)
Stealing Markus' PIC Test and Commissioning Documentation for a Basis

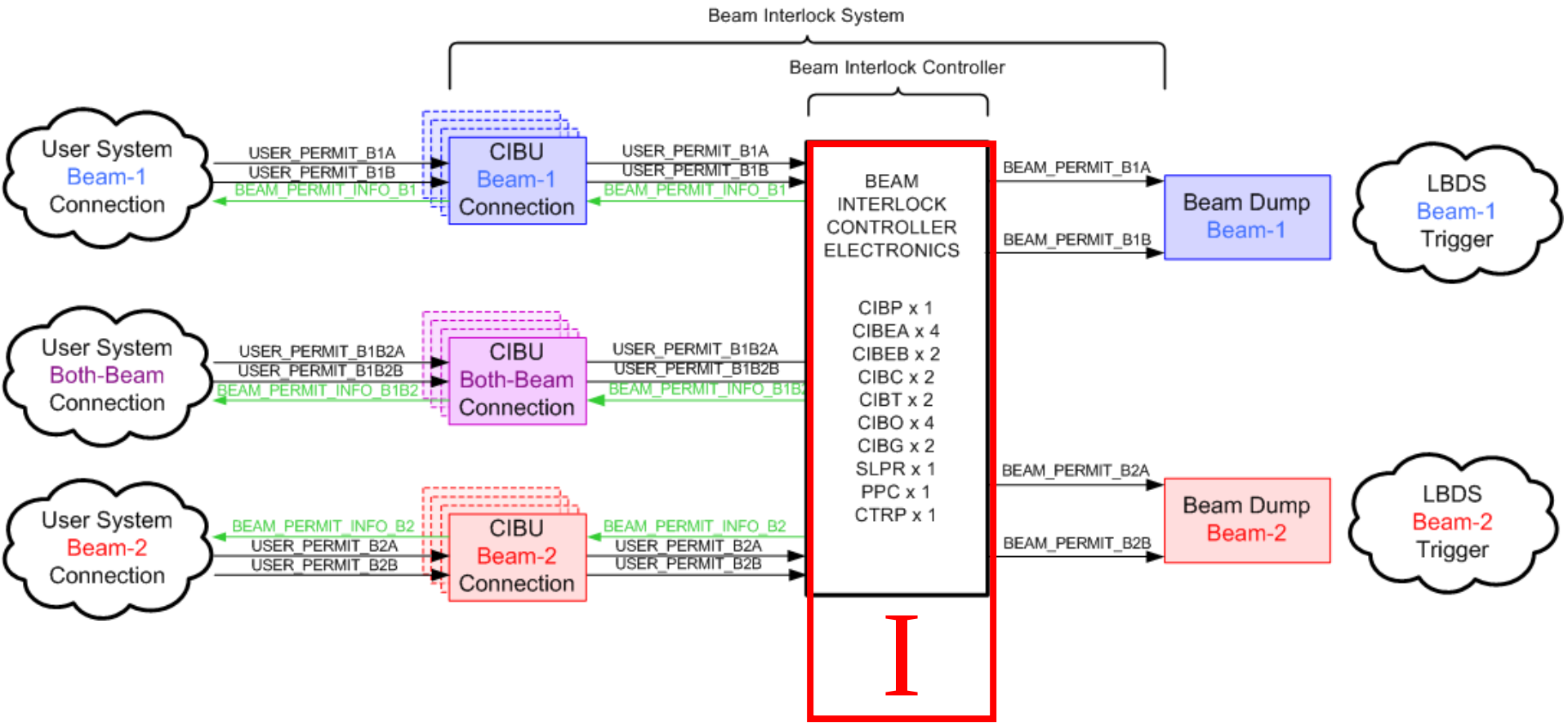
Documentation
-Describes Individual System Tests
-Describes Commissioning
-Gives basis for Pass / Fail Criteria
-Lists failure diagnosis for likely failures
-Serves as a guide for writing the Test Software

Phases Overview



The Testing and Commissioning has been split into phases
Incrementally tests the system, allowing milestones to be set for testing
Provides clear boundaries of who is involved, and where the test is carried out.

Phase I

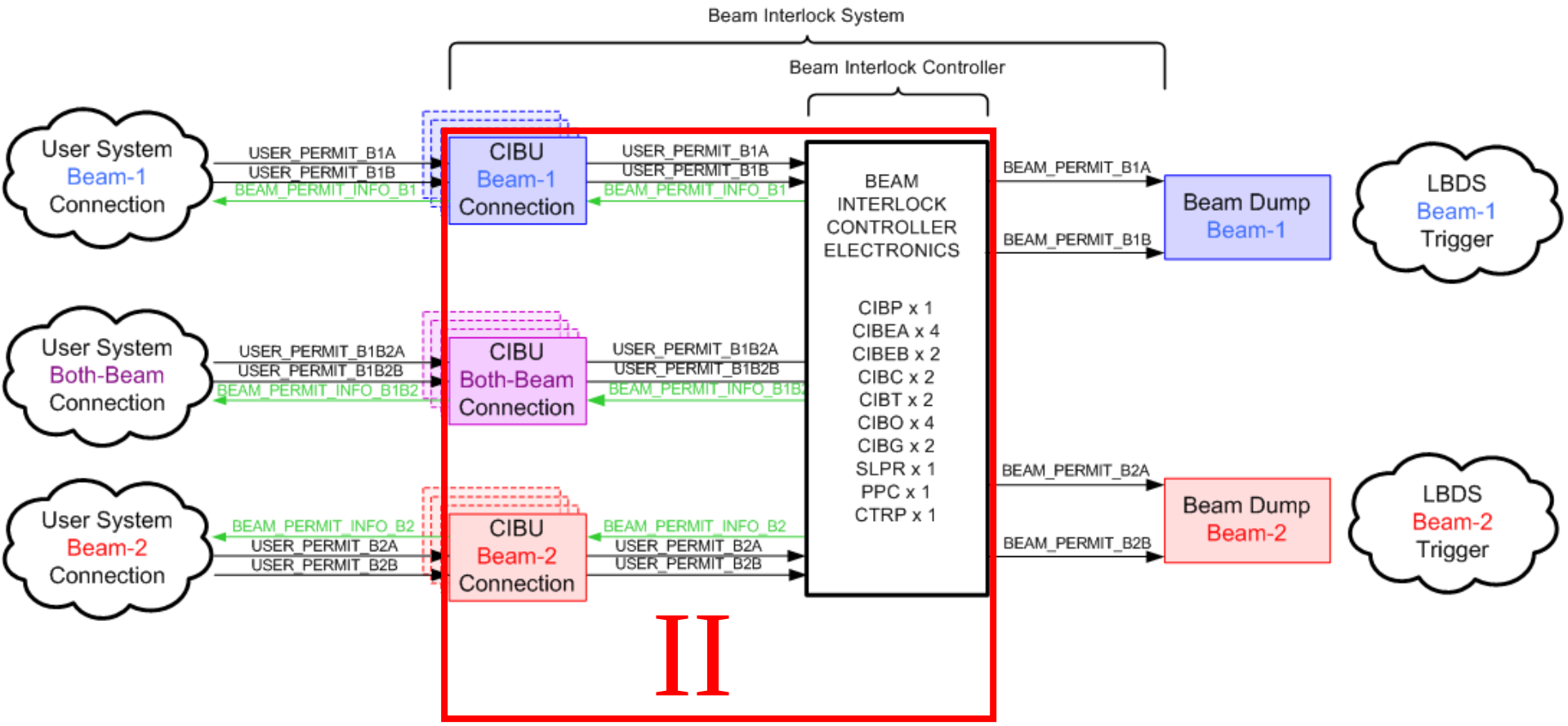


Stand Alone Controller Test

Who? Machine Interlocks Team

Where? Lab / LHC

Phase II

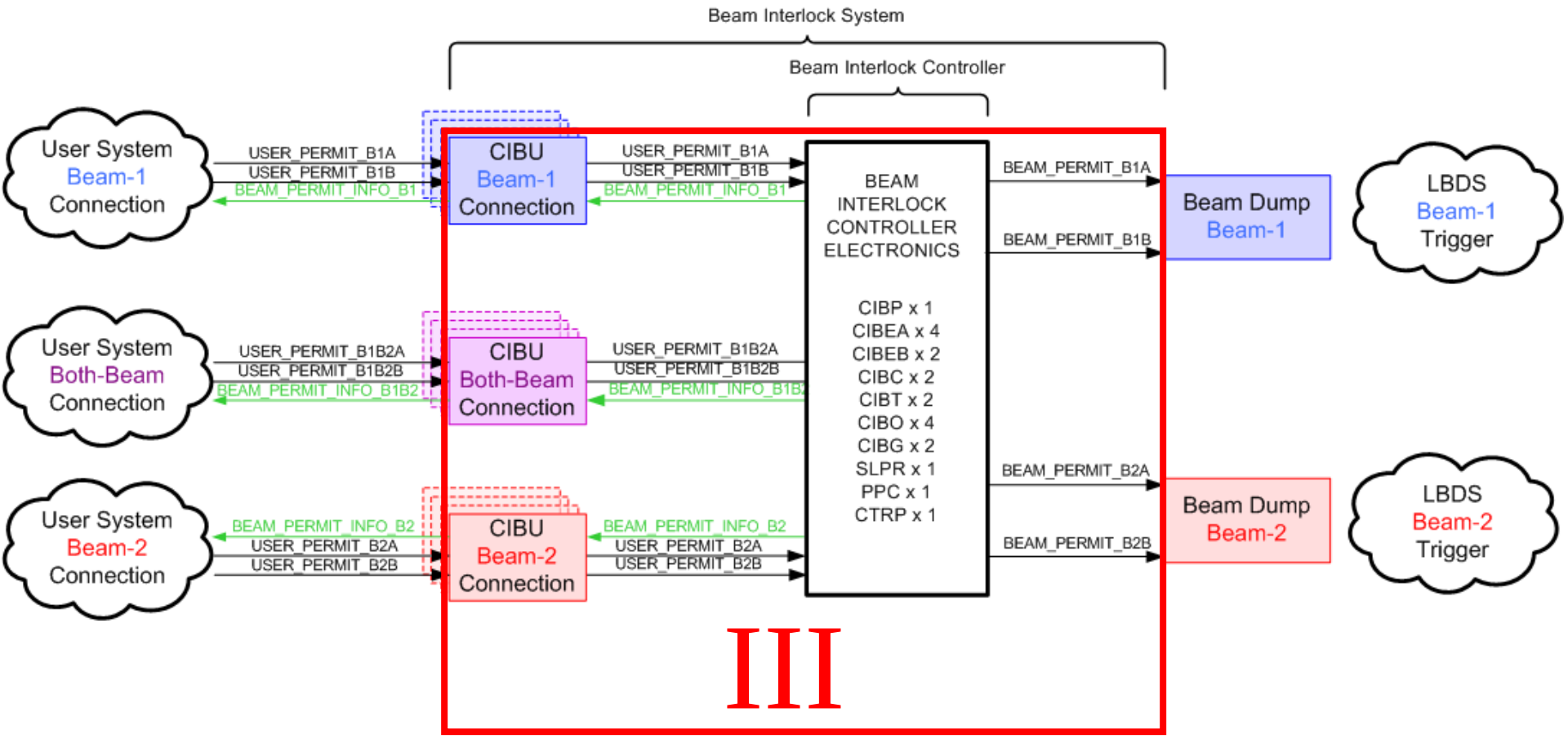


Controller & Interface Test

Who? Machine Interlocks Team

Where? Lab / LHC

Phase III



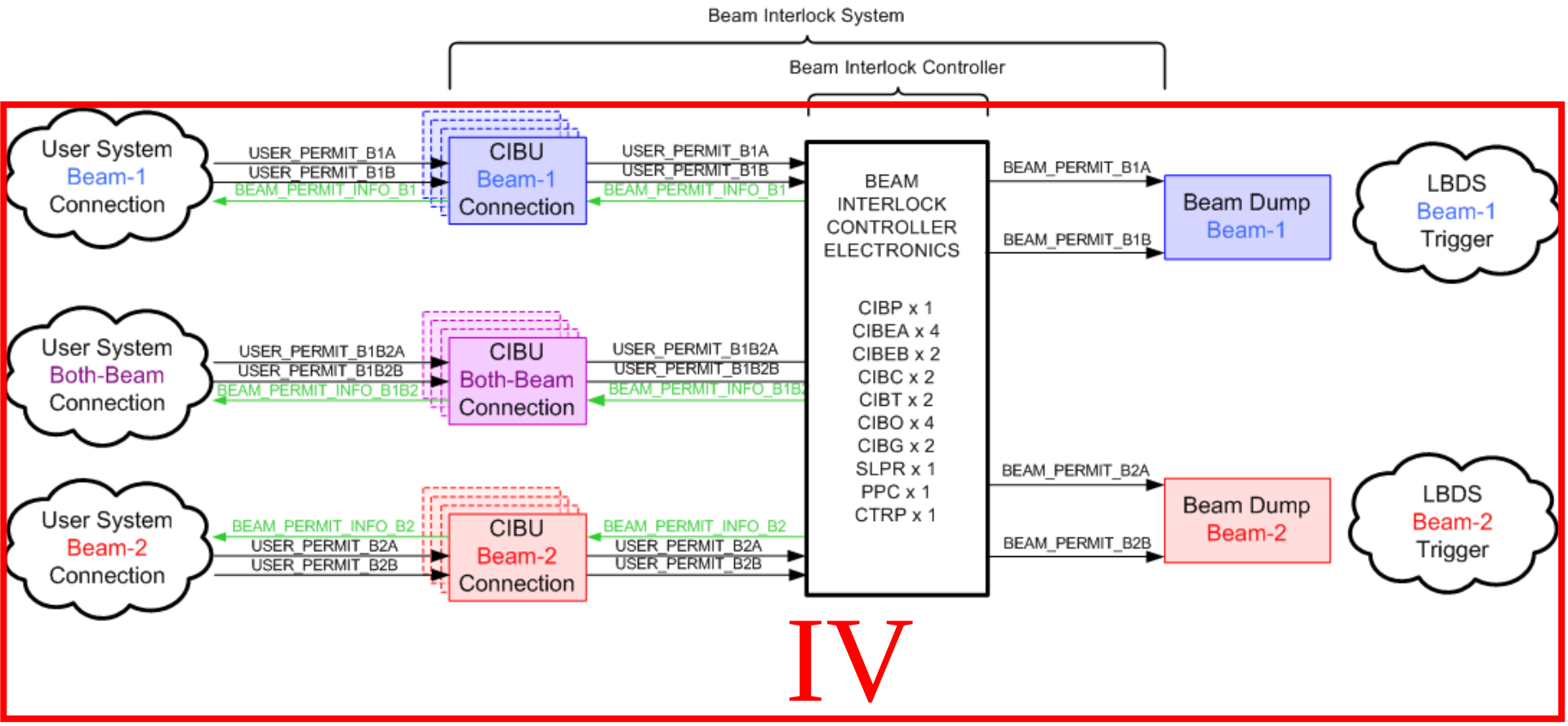
Beam Interlock System Test

Who? Machine Interlocks Team

Where? Lab / LHC

(Lab max 3 BICs)

Phase IV



Beam Interlock System Commissioning

Who? Machine Interlocks Team & LHC User Systems & LBDS

Where? LHC

Phases Summary

Phase I tests the Beam Interlock Controller in a stand-alone mode.

Phase II tests the Beam Interlock Controller including the User Interfaces, it ensures that the communications are coherent, and operating to specification.

Phase III tests the whole Beam Interlock System, including the Beam Permit Loops. It gives a time value for the propagation of each User System signal from a BIC to the LBDS. These results can be used in conjunction with the History Buffer to provide accurate Post-Mortem information from the BIS.

Phase IV is the final commissioning step required for LHC operation; it tests all the User System Inputs to the User Interfaces, and verifies the correct breaking of the permit loop as well as the detection of this by the LBDS.

For ***Phase IV*** a high level sequencer would be ideally used to switch User Permits *false* at the User System level.

(as currently implemented for the PIC/QPS/PC arrangement)

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Open Questions & Comments

1. Phases I, II and III can be carried out Independently, we don't need User Systems to be ready!
2. BUT… For the Permit Loop testing (phase III) the LBDS Frequency Detector must be
   a) Ready, installed, and powered OR
   b) Replaced by a dummy module OR
   c) Bridged completely
3. Can User Systems set User Permit A AND/OR B to true?
   - This is against the rules laid out in the Beam Interlock Specification
   - But this would speed up commissioning
   - Without this, we'll not be able to test the link User System to User Interface until the User System is really ready for beam.

Open Questions & Comments

4. Can User Systems and LBDS work with this Sequencer idea?
   - The ideal would be a push button on demand complete system integrity check before every run
   - Carried out by this sequencer!

FIN

Typical Method (Phase III)

7.4 EXECUTION METHOD

The test is presented in a list format, as previously described.

START OF TEST III

1. Ensure BICs have all competed Phase II testing
2. Ensure the 'Clean Up after Testing' has been completed for each BIC
3. Verify
   a. All internal status signals & History Buffers correspond to hardware (all BICs)
4. Set Software Permit A to *true* for all BICs
5. Set User Permit A to *true* for all BICs (via User Interface Test Mode)
6. Set Generator A to *true*
7. Verify
   a. Permit Loop A is formed
   b. All internal status signals & History Buffers correspond to hardware (all BICs)
   c. Frequencies of Permit Loop A are 10MHz (within tolerances)
8. Set User Permit A of first User Interface to *false*
9. Verify
   a. Permit Loop A is broken completely
   b. All internal status signals & History Buffers correspond to hardware (all BICs)
   c. Latch A is *true* for all BICs
   d. Frequencies of Permit Loop A are 0MHz (within tolerances)
   e. Event reconstructor correctly determines source of Beam Dump
10. Record Event Timings
11. Set Latch A to *false* for all BICs
12. Repeat 4, 5, 6, 7, 8, 9, 10 and 11 for all User Interfaces and Software Interlocks
13. Repeat 4, 5, 6, 7, 8, 9, 10, 11 and 12 for B signals

END OF TEST III

7.5 CLEAN-UP AFTER TESTING

Once the tests are complete the following must be carried out

1. Record all Cabling
2. Record the Timings Point to Point
3. Record that IST of BIS is completed with timing specifications for each User Interface link to LBDS