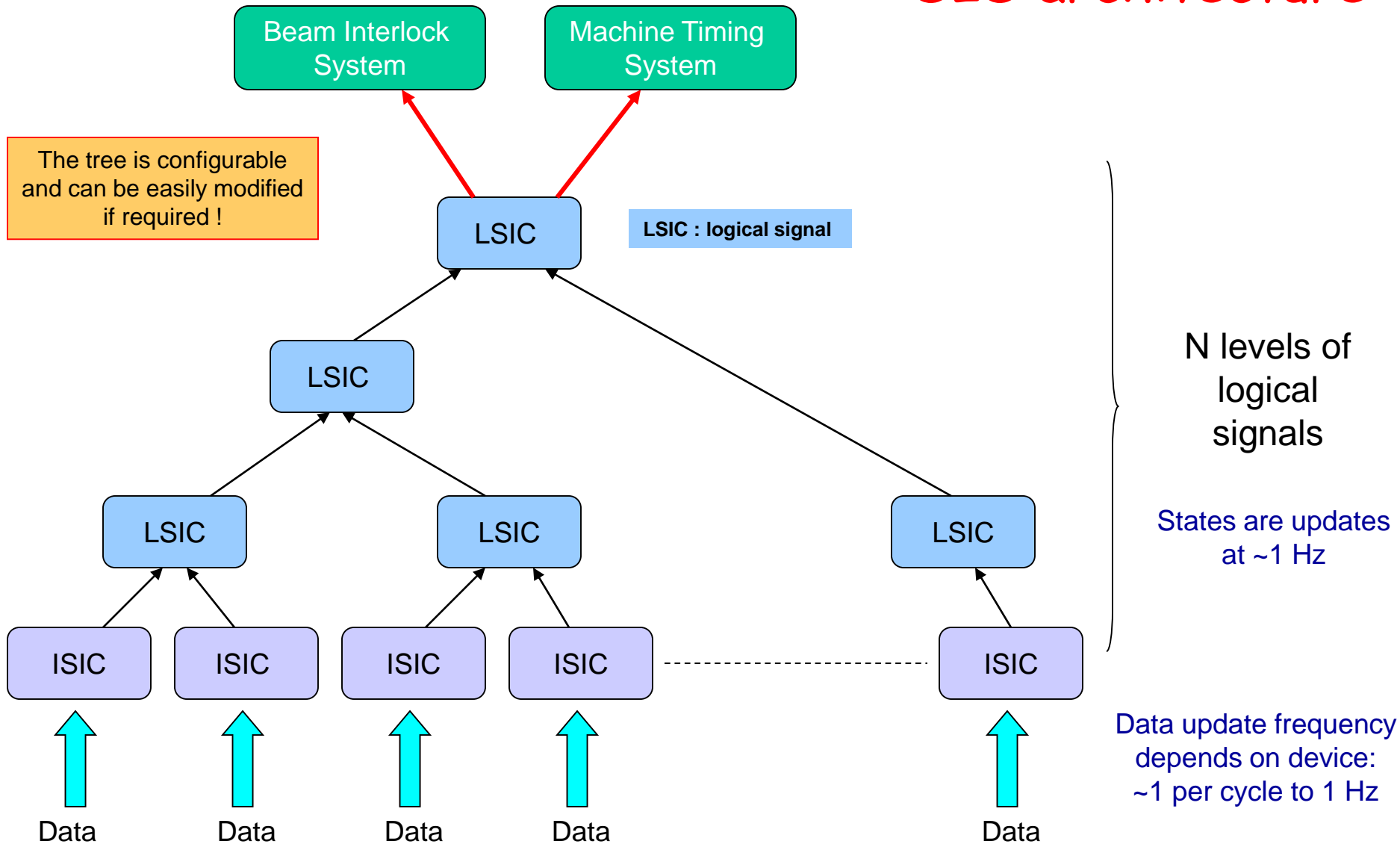# Software Interlock System
& test procedures for TL interlock system

J. Wenninger AB/OP/SPS
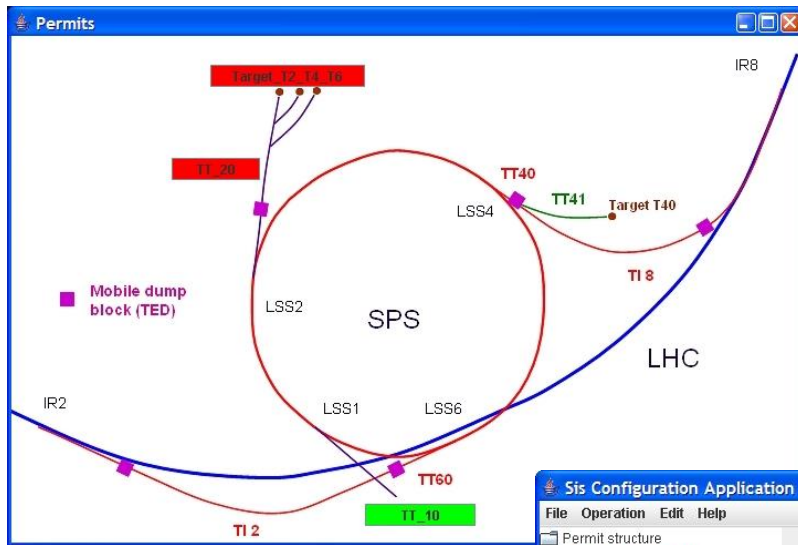
V. Baggiolini, J. Wozniak AB/CO/AP

- SIS status & milestones

- SPS buttons

- Test definitions for TL interlock

SIS architecture

Beam Interlock System

Machine Timing System

The tree is configurable and can be easily modified if required !

LSIC

LSIC : logical signal

LSIC

LSIC

LSIC

LSIC

N levels of logical signals

States are updates at ~1 Hz

ISIC   ISIC   ISIC   ISIC - - - - - - - - - - - - ISIC

Data   Data   Data   Data   Data

Data update frequency depends on device: ~1 per cycle to 1 Hz

ISIC : individual interlock channel, entry point for data (can also be logical).

SW Tests & Demo

- Performance of logical tree evaluation seems adequate even for 1 Hz rates. To be confirmed by real-life tests….

- Demo / test UI written by J. Wozniak
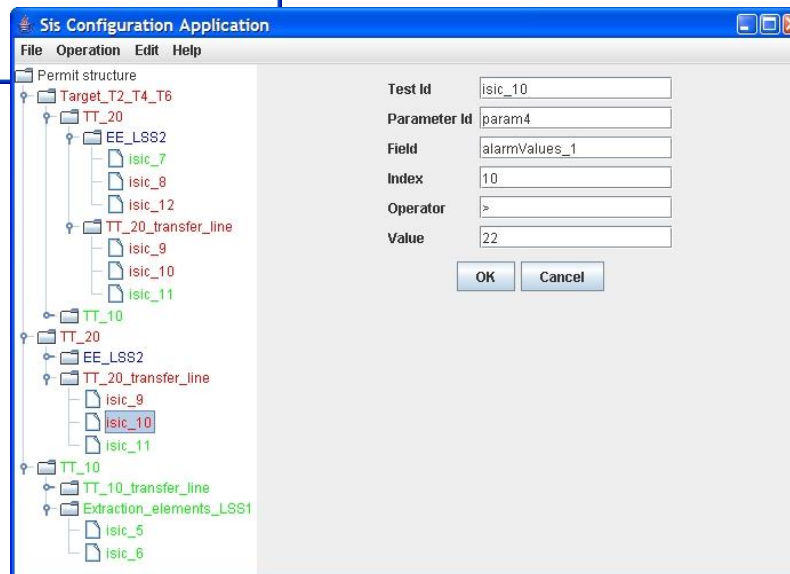
SPS beam destinations

- To stop the SPS beam production through the timing system, the SIS beam permits will be matched to the DESTINATION information (distributed in the timing telegram).
- Each beam has this destination information attached to it (set manually by OP).
- The SIS will inform the timing system that beams to a given destination must be inhibited due to a fault condition.

SPS beam destinations (2006) :
- FTARGET
- CNGS
- LHC1-TI2
- LHC2-TI8
- SPS_DUMP (not extracted)
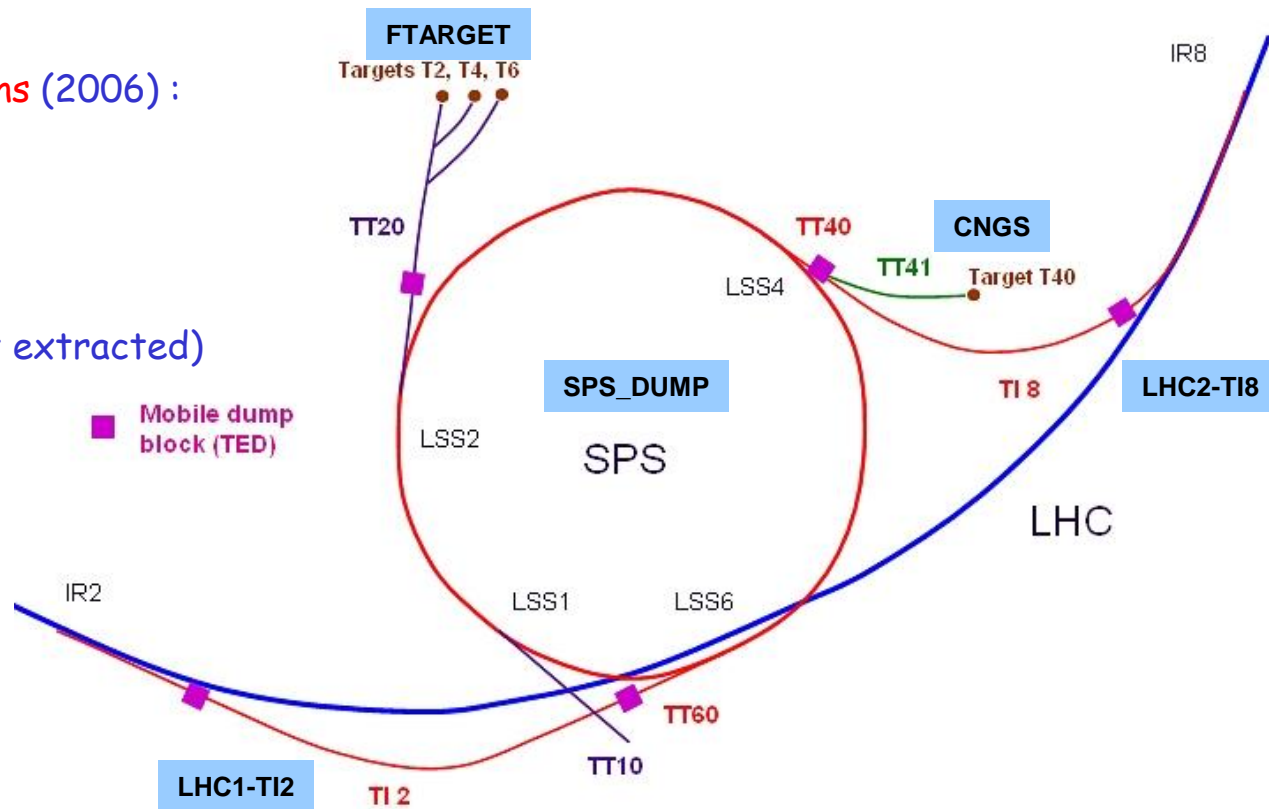
SIS permits to BICs

- One software input to each BIC that will be used by SIS to inhibit extractions/dump beams.

- The software input may be set by an external SW client through a FESA property. The client must send a ('secret') code to change the SW interlock input from TRUE to FALSE and vice-versa.

- Since the state of the SW input is 'static', a watchdog mechanism will be implemented in FESA:

    - the SW input is reset to FALSE automatically after a timeout.

    - the client must re-send(set) the permit at an interval < timeout.

    - the timeout will be configurable by a separate property (also protected by a 'code').

- Ongoing … waiting for first implementation…

Timing & Synchronization issues

- At least the SPS we have an issue of synchronization with the machine :

    - For types certain data access (BI).

    - For data integrity and update checks.

    - …

- The distribution of timing signals by SW exists but is far from roc-solid :

    1. Install a timing receiver card CTRI in the server that runs SIS[*].

    2. Implement an internal SIS timing watchdog on the SW timing distribution and stop all beams when there is a suspicion of timing distribution problems.

- The first option for the synchronization is much more solid and by far preferred – but the CO infrastructure section is (presently) opposed to it (maintenance):

    Need support from MPWG for option 1 if we agree it is a good idea !

(*) : also required for LHC feedbacks (orbit, tune…)

Milestones for 2006

- Mid-March: 1st demo version of SIS for CNGS
    - A few equipment
    - Connection to BIS (= primary safety mechanism for CNGS)
    - Connection to timing (not needed for CNGS safety)
    - GUI similar to what is already there, configuration via XML
- Mid-May: CNGS commissioning => dry run for SIS
- Mid-June: Operational deployment for SPS-Experimental areas ("Wobsu" = Wobbling survey)
    - Surveillance of 4 magnets + 2 positions
- Mid-July: CNGS semi-operational => operational version
    - Simple security mechanism for *set* access to BIS properties
    - Alarms
- End September: TI8
- November/December: Sector test

SPS CCC island buttons for <u>2006</u>

<u>Beam interlock inhibit buttons :</u>

1. A button **dump/stop all beams**, connected to one SPS ring BIC. Pressing this button will dump the circulating SPS beam and inhibit any beam in the SPS (injection kicker inhibit though the existing SPS Emergency Dump System).

2. A button **inhibit LSS4 extraction**, connected to the TT40 BIC. Pressing this button will inhibit extractions through the LSS4 extraction channel to CNGS and to TI8/LHC ring 2.

3. A button **inhibit LSS6 extraction**, connected to the TT60 BIC. Pressing this button will inhibit extractions through the LSS6 extraction channel to TI2/LHC ring 1.

<u>Timing system inhibit buttons :</u>

1. Inhibit all beams
2. Proton inhibit
3. Ion inhibit
4. MD beam inhibit (inhibit all beams marked as MD beams – similar property to the destination)
5. Inhibit beams with destination SPS_DUMP
6. Inhibit beams with destination FTARGET
7. Inhibit beams with destination CNGS
8. Inhibit beams with destination LHC1-TI2
9. Inhibit beams with destination LHC2-TI8

Interlock Tests for TLs

- First draft of test procedures document was sent to some 'guinea pigs' for feedback on the general structure of the document, missing points…

- From the feedback (thank you for the time and replies !):

  - Structure of the document changed in 2 main parts: one for the conditions, phases, general issues… and one for the tests themselves.

  - Tests re-ordered, commissioning phases clarified.

  - Classification of tests following the external requirements:

    - Machine timing and/or 'settings management' → control system in 'advanced' state !

    - Beam in SPS.

    - Beam in TLs.

- Some of the tests overlap with ISTs (Ind. System Tests) – point will be added that some ISTs should/must be repeated as a final check:

  - Similar to the DSO access system acceptance tests before a machine restarts, where he 'samples the system'.

  - We may want to test everything that is accessible from applications in the CCC ?

- Next advanced draft for first week of March → wide circulation.

Equipment lists

- While finishing the first draft for the interlock test procedures, I realized that there was no exhaustive list of interlocked equipment…

  →Assembled all equipment / devices lists into a document.

- The list are presently checked by people responsible for them… Some feedback from BT and AT/VAC.

- Should the lists

  - be approved ?

  - 'just' be published such that they are available in official form ? And updated when they change…

Summary of interlocked devices

	LSS4	TT40	TI8	TT41	LSS6	TT60	TI2	Total
Septum converters		1				2		**3**
Dipole converters	8	2	6	2	8	1	7	**34**
Quad. converters		4	15	14		6	19	**58**
COD converters		3	42	16		5	47	**113**
Total converters	8	10	63	32	8	14	73	**208**
FMCM		3	3	2		2	3	**13**
TEDs & PPDs		1	2	2		1	1	**7**
Vacuum valves		1	6	4		2	5	**18**
Collimators			7				7	**14**
Beam Position Monitors	20			23	20			**63**
Beam Loss Monitors	8	6	33	12	13		34	**106**
Profile monitors	2	3	9	8		3	10	**35**
Total	**38**	**24**	**123**	**83**	**41**	**22**	**133**	**464**

I surveillance (ROCS)

+ WIC, girders, septum magnet surveillance, kickers.