Machine Protection Working Group

Minutes of the 55th meeting, held 17th March 2006

Present: B. Dehning, G. Guaglio, C. Ilgner, K. Kahle, V. Kain, D. Macina, V. Montabonnet, B. Puccio, R. Schmidt, L. Serio, R. Steinhagen, M. Stockner, J. Uythoven, C. Zamantzas, M. Zerlauth

Meeting Agenda:

- Beam Loss Monitor electronics and beam dump thresholds [C. Zamantzas]
- FMCMs for additional protection in case of mains disturbances [M. Zerlauth]
- AOB [R. Schmidt]:
  1. News on 'CRYO-OK'
  2. Collaboration with ETH-Zürich on safety and reliability issues

Beam Loss Monitor electronics and beam dump thresholds [C. Zamantzas]

In his presentation, **C. Zamantzas** discusses the design and constraints of the LHC Beam Loss Monitoring (BLM) electronics (see slides for details).

There are about 3700 beam loss monitors distributed in the LHC. The BLM acquisition electronic is split into two parts. The low-level electronic (BLMCFC) cards located inside the tunnel can serve each up to 8 ionisation chambers. They perform the required current to frequency and analogue to digital conversions (CFC & ADC). Two of these BLMCFC cards are connected using optical fibre to an acquisition card (BLMTC) on the surface. The surface cards are themselves based on FPGA technology and perform the more complex signal processing, concentration and beam loss threshold comparison that is used to eventually dump the beam if required. Each BLM crate consists of up to 16 of these processing cards connected to up to 16 detectors each, a combiner card that returns the accumulated result to the Beam Interlock Controller, a PowerPC and a general timing card.

The present surface acquisition card performs the data transmission error checks, combines the CFC and ADC data coming from the tunnel cards and computes the running sums over 12 different time windows. The time windows range from 40 us up to 84 seconds. Finally the results of each window are compared against a given threshold table, which is a function of energy and acquisition frequency. The number of threshold tables matches the number of input channels. By using a second table, the card may distinguish the BLM channels into “Maskable”, “Not-Maskable” and “Not-Used”. In addition, the surface cards provide monitoring of the card functionality similar to the Beam Interlock Controller.

In order to provide more flexibility using these BLM thresholds, **C. Zamantzas** proposes that he could additionally implement a threshold scaling by factors of two if required. This could be implemented using bitwise shift registers that are easy to implement and use only a minimum additional amount of the available card resources.

He points out that a further extension of the BLM logic is limited due to constraints imposed by the used chips, front-end and operating systems. He stresses that it is not advisable to fully use the available FPGA capacity. The currently implemented logical function already exploits about 95% of the available memory and 86% of the available logical units inside the FPGA. Apart from the FPGA

and memory constraints, a further upgrade is limited by the operating system used by the crate's PowerPC. Presently, LynxOS is limited to map less than 192 MB per crate which translates to a maximum of 8 MB per acquisition card. The present card implementation uses approximately 14 MB. The additional space can be addressed through paging.

During hardware commissioning, the initial threshold tables and the FPGA firmware will be stored in a non-volatile memory, available on-board, through the VME bus using the crate's PowerPC. On a crate power up the FPGA copies the table in its internal memory space during its initialisation process. Only after the end of this process and the foreseen power-up test procedure the beam permit signal will be send. Thus, in order to use tables that have been updated from the last initialisation the crate needs to be rebooted which consequently will lead to a beam dump.

However, in order to be able to run these cards more autonomously and to disable this unsecured access to the FPGA firmware and the threshold tables, each card has a hardware switch that decouples the acquisition card and prevents further write access through the VME bus. Further write access will then only be possible locally through an external access port on the front of the BLM crate. Though 'write' access is disabled, the status of the card, and particularly the status of the switch, can still be monitored through the VME bus.

Since open access (open switch) to the BLM cards is an issue with respect to criticality, **B. Dehning** inquires which Safety Integrity Level (SIL) would be requested during beam commissioning and consequently at which point the switch in each BLM surface card should be used to make the threshold settings immutable through the VME bus.
ACTION: R. Schmidt

It was identified that the management and consistency of the actual card configuration and the one stored inside the databases of the tunnel BLM cards is an issue.

FMCMs for additional protection in case of mains disturbances [M. Zerlauth]
M. Zerlauth discusses the additional protection through the Fast Magnet Current Change Monitors (FMCM) in the event of mains disturbances (see slides for details).

The FMCMs are foreseen to be used in the LHC and the SPS-LHC/CNGS transfer lines and provide an additional level of safety. They will detect fast current changes in critical normal conducting magnets and consequently dump the beam in case of a failure (see minutes of MPWG meeting #43 for details). Due to its high accuracy and sensitivity, the same system may also detect disturbances of the mains electricity network for instance, due to thunderstorms.

The minimum required disturbance rejection for LHC equipment connected to the 400 and 230 V networks, respectively, has been defined within an LHC engineering specification (see 'Main Parameters of LHC 400V/230V Distribution System' EDMS 113154). The document specifies tolerance levels of voltage swells of 50% over 10 ms, voltage dips of -50% over 100 ms and maximum transients of up to 1200 V for 0.2 ms.

K. Kahle points out that all powering equipment bought by TS-ES is tested by default to this engineering specification as part of the acceptance tests. **R. Schmidt** inquires whether the used CO VME crates and PLCs have similarly been tested against above voltage perturbations. **M. Zerlauth**

stresses that most of the local power supplies for electronics supply could normally withstand these specified disturbances, partially due to the use of un-interruptible power supplies (UPS). **R. Schmidt** proposes that conformance with the above engineering specification should be tested experimentally, particularly for the used VME and PLC systems.
ACTION: M. Zerlauth

K. Kahle will be invited to present more detailed information on UPS, in particular with respect to reliability and availability.
ACTION: R. Schmidt

Presenting the schematic layout of CERN's powering network, **M. Zerlauth** shows how an exemplary global 50% voltage dip in one phase of the mains network propagates and cascades through the different higher and lower voltage levels. The voltage dip increases for each lower voltage level and can reach more than 100% with respect to the initial voltage dip. However, the increased propagation is always from higher voltage to lower voltage stages. The upward propagation is much less significant in the CERN network. The observed number of voltage variation ranges from 8 per month for the 400kV, 20 per month for the 18kV and 35 per month for the 400V network. Most (60%) of the incidents where dips, 30% transients, 10% swells and 0.4% due to mains failures of which 20% were due to thunderstorms.

The weakest links in the LHC in terms of susceptibility are the high current power converters which can be grouped into switching mode (60A-8kA), main dipole thyristor (13kA) and general thyristor converters as for example being used for the dump septa. The switch mode converters are supplied through the 400 V and the thyristor converters are supplied through the 400V and 18kV AC networks. The function generator and DCCT electronics are powered either directly through the 400V lines or UPS and are therefore not affected by the voltage variations.
Simulations for the different power converter types were performed for the specified voltage perturbations by V. Montabonnet (see slides for details). The analysis shows that the thyristor power converter used for normal conducting magnets such as the septa are most likely prone to mains disturbances due to their high power throughput and low storing capacity and are hence identified as the weakest links. Most of these magnets are already foreseen to be equipped with FMCMs.

In conclusion, **M. Zerlauth** shows that the present FMCM detection levels and performance is presently a factor four better and about a factor 10 faster than expected current deviations of the 400V network and is capable to capture those failure modes and dump the beam before the situation becomes critical for the beams. The same applies to errors in the higher voltage stages.

AOB **[R. Schmidt]**:

News on 'CRYO OK':
There will be a meeting between the experts involved to discuss possible solutions on how to abort powering in case the 'CRYO OK' permit is absent. The actual risks, protection requirements and possible solutions should be (re-) evaluated. Presently an implementation of the powering abort on the PLC-to-PLC level is preferred to PVSS-to-PVSS and hard-wired solutions. Studies are ongoing.

Collaboration with ETH-Zürich on safety and reliability issues:

R. Schmidt and **J. Wenniger** initiated a collaboration with the 'Laboratory for Safety Analysis' of the ETH Zürich. They will provide a PhD student and help in bringing in advanced techniques for modelling and optimisation of complex technical systems with respect to performance, reliability and risks. The scope of their present field covers general applications as well as energy systems such as nuclear power plants.