LHC Beam Loss Monitoring System

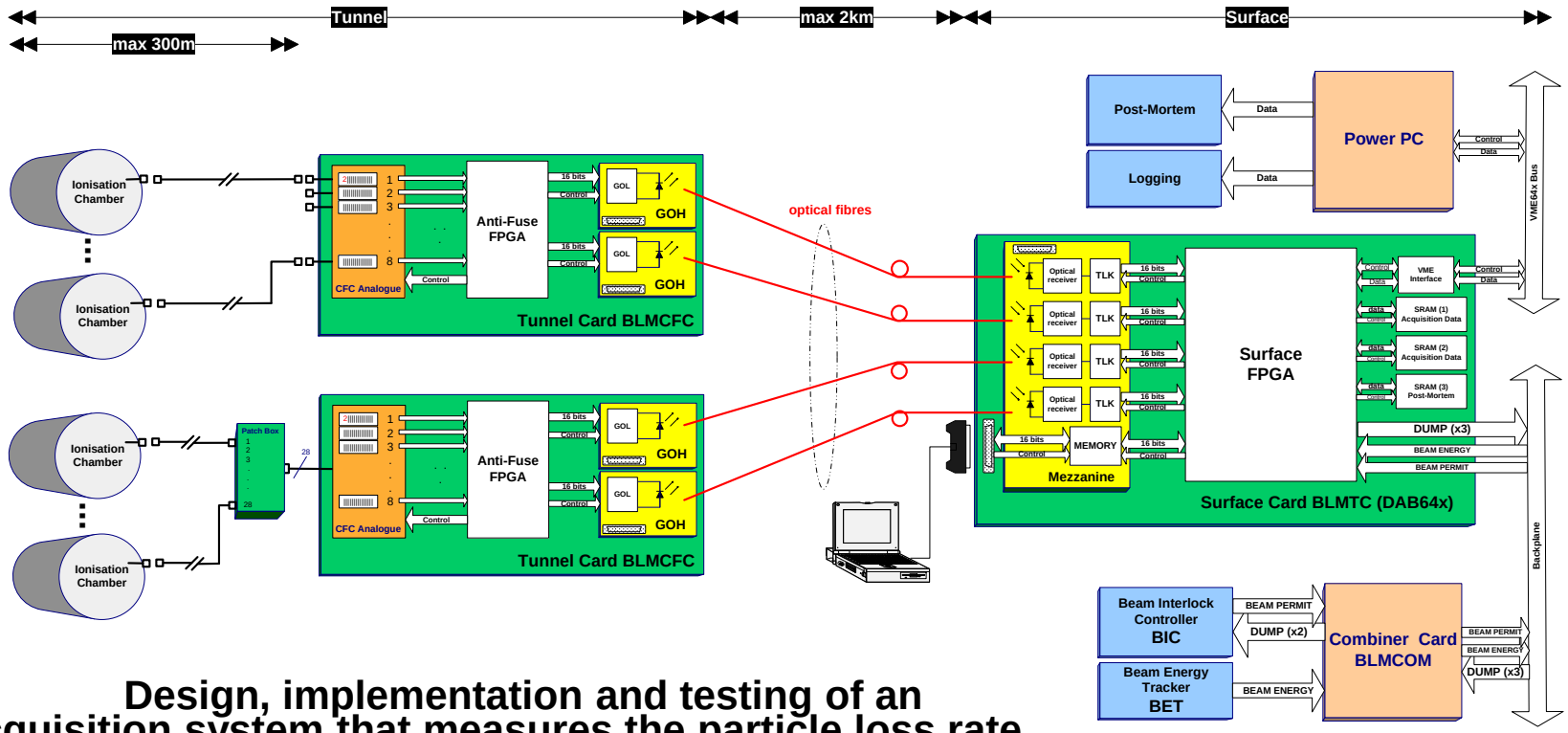
Beam Loss Monitor electronics and Beam Dump Thresholds

LHC Machine Protection Working Group

LHC Beam Loss Monitoring System

- BLM Overview
- Surface Card (BLMTC)
- Processes running in the Surface FPGA
  - Real-Time Analysis of Data
  - Threshold Comparator & Masking
- Scaling Down the Threshold Values (Proposal)
- Configuration of the DAB64x
  - Configuration Schemes (x3)
- Outlook

BLM Overview

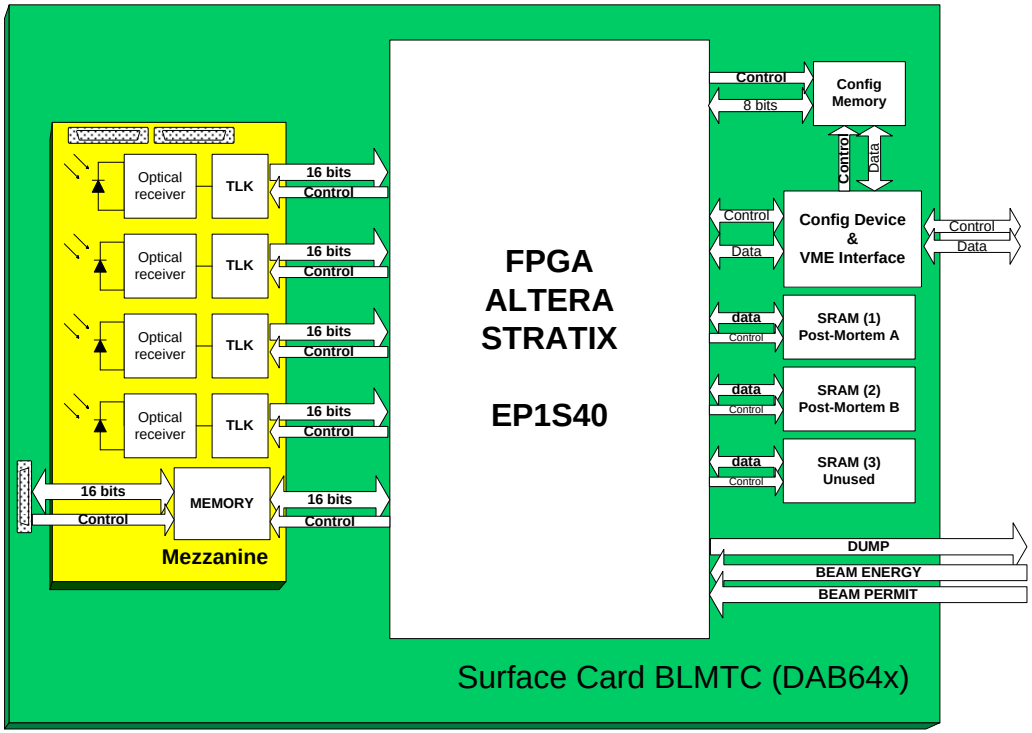


Design, implementation and testing of an acquisition system that measures the particle loss rate.

Main components of the system:

- 3700 Detectors
- Current to Frequency Converters (CFCs)
- Analogue to Digital Converters (ADCs)
- Tunnel FPGAs: **Actel**'s 54SX/A radiation tolerant.
- Communication links: Redundant **G**igabit **O**ptical **L**inks.
- Surface FPGAs: **Altera**'s Stratix EP1S40 with 780 pin.

Surface Card (BLMTC)

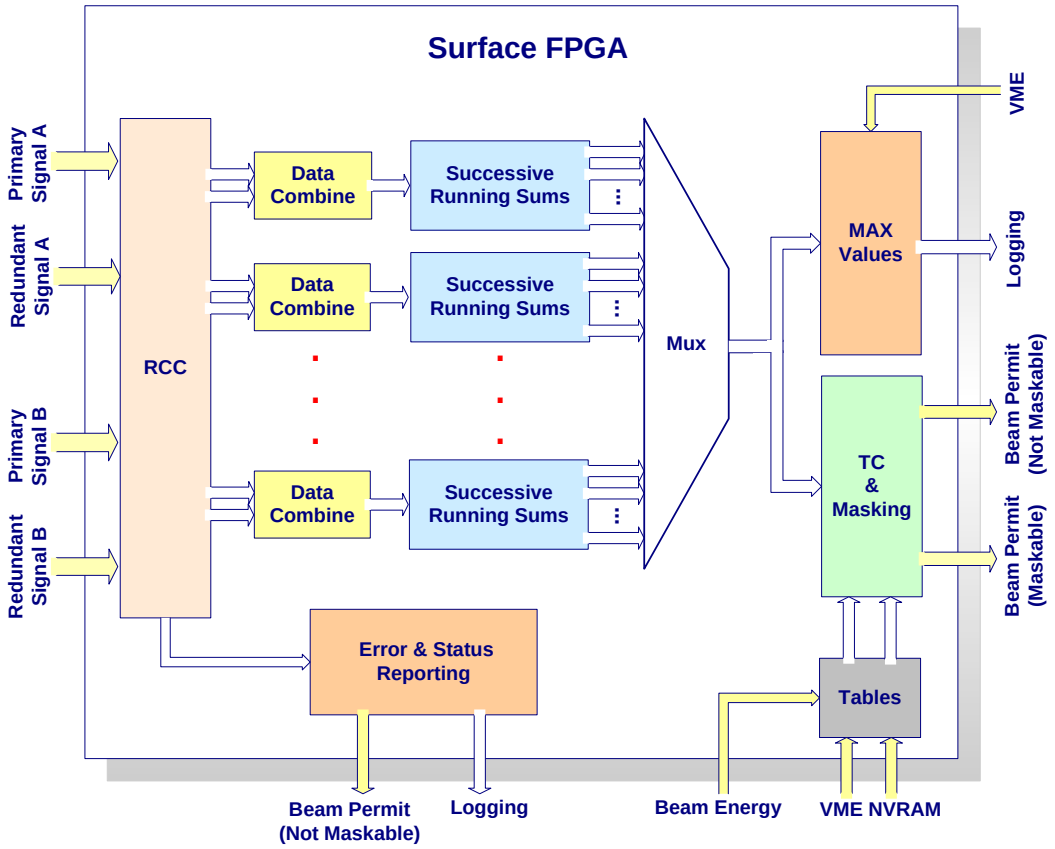


DAB64x specifications

- **Stratix FPGA**
  - **Vertical Migration to EP1S40**
- **SRAM memories (x3)**
  - **512K x 32bit**
- **Connectors for Mezzanine**
  - **2 x 64pin PMC connectors**
  - **Provide 3.3V, 5V, GND, and**
  - **Connection to 114 FPGA I/O pins.**
- **Card bus**
  - **VME64x**

Stratix Device Features		
Features of **EP1S40** Device	Available	Used
Logic Elements	41,250	35,475 (86%)
M512 RAM blocks (32 ×18 bits)	384	299 (78%)
M4K RAM blocks (128 ×36 bits)	183	174 (95%)
M-RAM blocks (4K ×144 bits)	4	0 (0%)

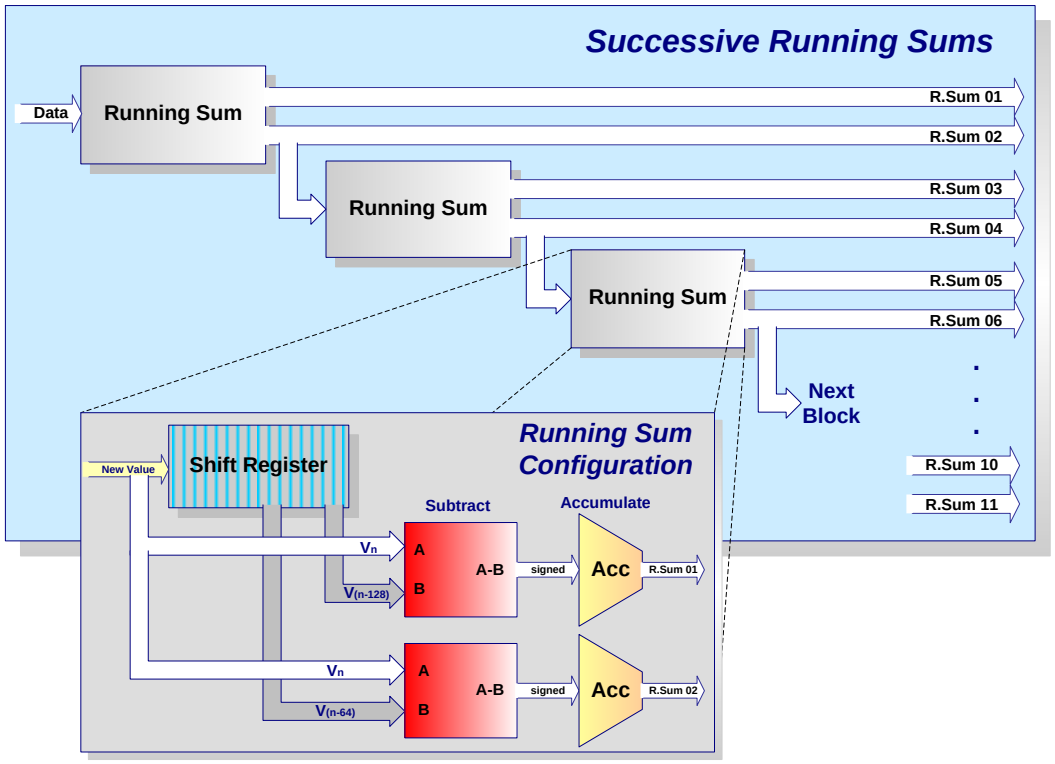
Processes running in the Surface FPGA



Processing Block	LE	M512	M4K
RCC	4 %	8 %	-
DataCombine	4 %	-	-
SRS	30 %	70 %	57 %
TC & Masking	13 %	-	35 %
ESR	4 %	-	1 %
MAX Values	31 %	-	2 %
Total Resources Used	**86 %**	**78 %**	**95 %**

- **Receive, Check & Compare (RCC)**
  - Receives, De-serialises and decodes the transmitted packets.
  - Checks for errors.
  - Compares the packets.
- **Data-Combine**
  - Merges the ADC and the CFC data into one value.
- **Successive Running Sums (SRS)**
  - Produces and maintains various histories of the received data in the form of Moving Sum Windows.
- **Threshold Comparator (TC)**
  - Compares the sums with threshold limits.
- **Masking**
  - Distinguishes between “Maskable” and “Not-Maskable” channels.
- **Supervision and Logging**
  - Error & Status Reporting (ESR)
  - Maximum Values of the SRSs.

Real-Time Analysis of Data



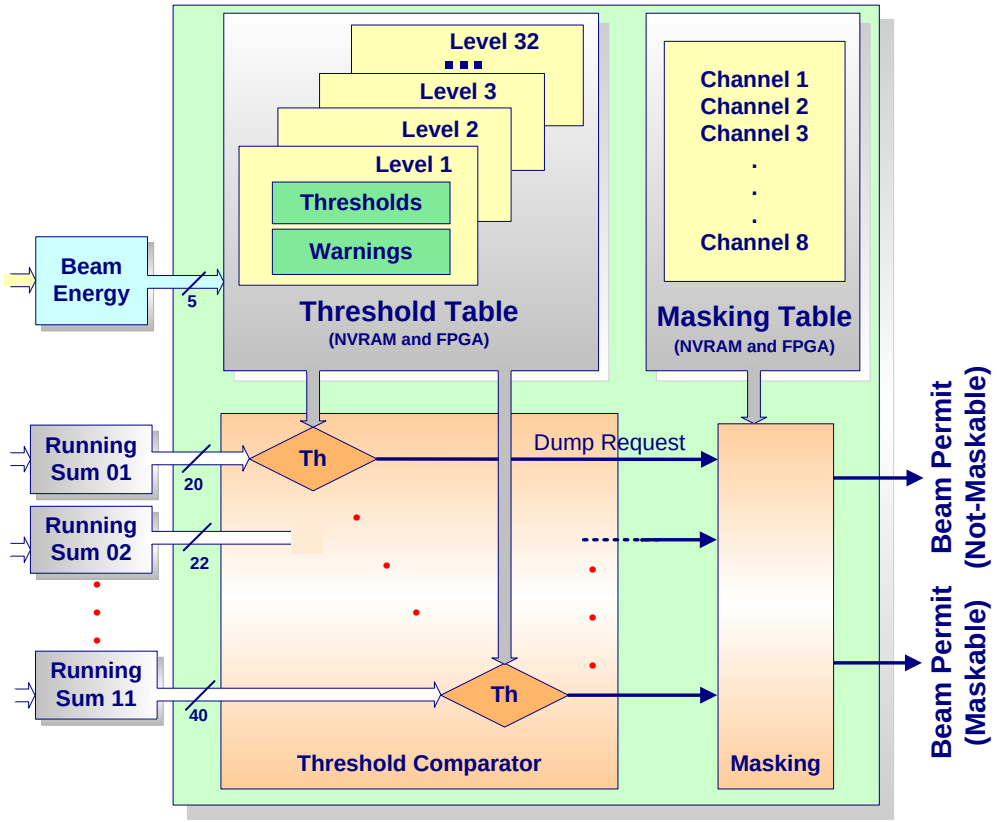
Running Sums

- Multi-point Shift Registers holds data
- Successive calculation of Running Sums
- Range 40µs - 84s (12 Running Sums)
- Maximum values of the last second are continuously calculated and kept.

Table 1: Successive Running Sums configuration

Running Sums		Refreshing		Shift Register Name	Signal Name	bits used
40 µs steps	ms	40 µs steps	ms			
1	0.04	1	0.04		RS 00	**20**
2	0.08	1	0.04		RS 01	**22**
8	0.32	1	0.04	SR1	RS 02	**22**
16	0.64	1	0.04		RS 03	**22**
64	2.56	2	0.08	SR2	RS 04	**26**
256	10.24	2	0.08		RS 05	**26**
2048	81.92	64	2.56	SR3	RS 06	**32**
8192	327.68	64	2.56		RS 07	**32**
32768	1310.72	2048	81.92	SR4	RS 08	**36**
131072	5242.88	2048	81.92		RS 09	**36**
524288	20971.5	32768	1310.72	SR5	RS 10	**40**
2097152	83886.1	32768	1310.72		RS 11	**40**

Threshold Comparator & Masking



Threshold Table

- Threshold depends on energy and a acquisition time.
- Unique thresholds for each detector.
- Read at system power-on from an external Non Volatile RAM or it can be included in the Configuration file.
- Space required: 32 KB

Table 1: Memory Utilisation by the Threshold Table

Width (Bits)	Detectors	Energy Levels	Running Sums	Values	Total (Bits)
32	16	32	8	4,096	131,072
64	16	32	4	2,048	131,072
		Total	**12**	**6,144**	**262,144**

Masking Table

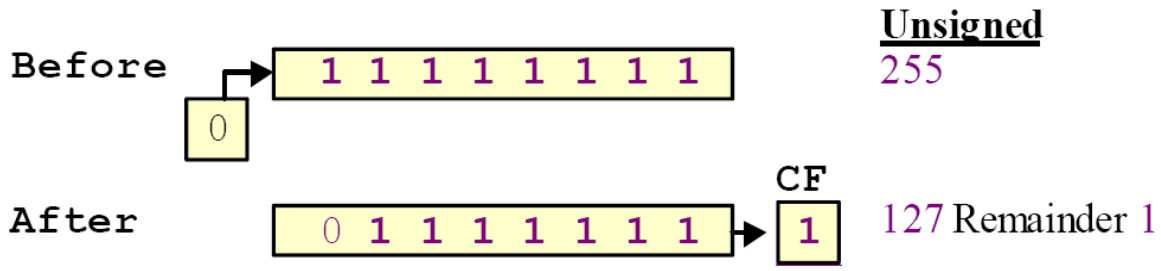
- Masking of channels is allowed only when safe.
- Unique masking for each detector.
- Read at system power-on from an external Non Volatile RAM or it can be included in the Configuration file.

Table 2: Information included in the Masking Table

Detector	Connected	Maskable
1	No	Yes
2	No	Yes
3	Yes	No
…	…	…
15	Yes	No
16	Yes	Yes

Scaling Down the Threshold Values (Proposal)

- **Threshold values are:**
  - **Unsigned binary numbers**
  - **32 or 64 bit long**
  - ➢ **Division by 2** can be achieved by **Shifting Right** by 1 position.



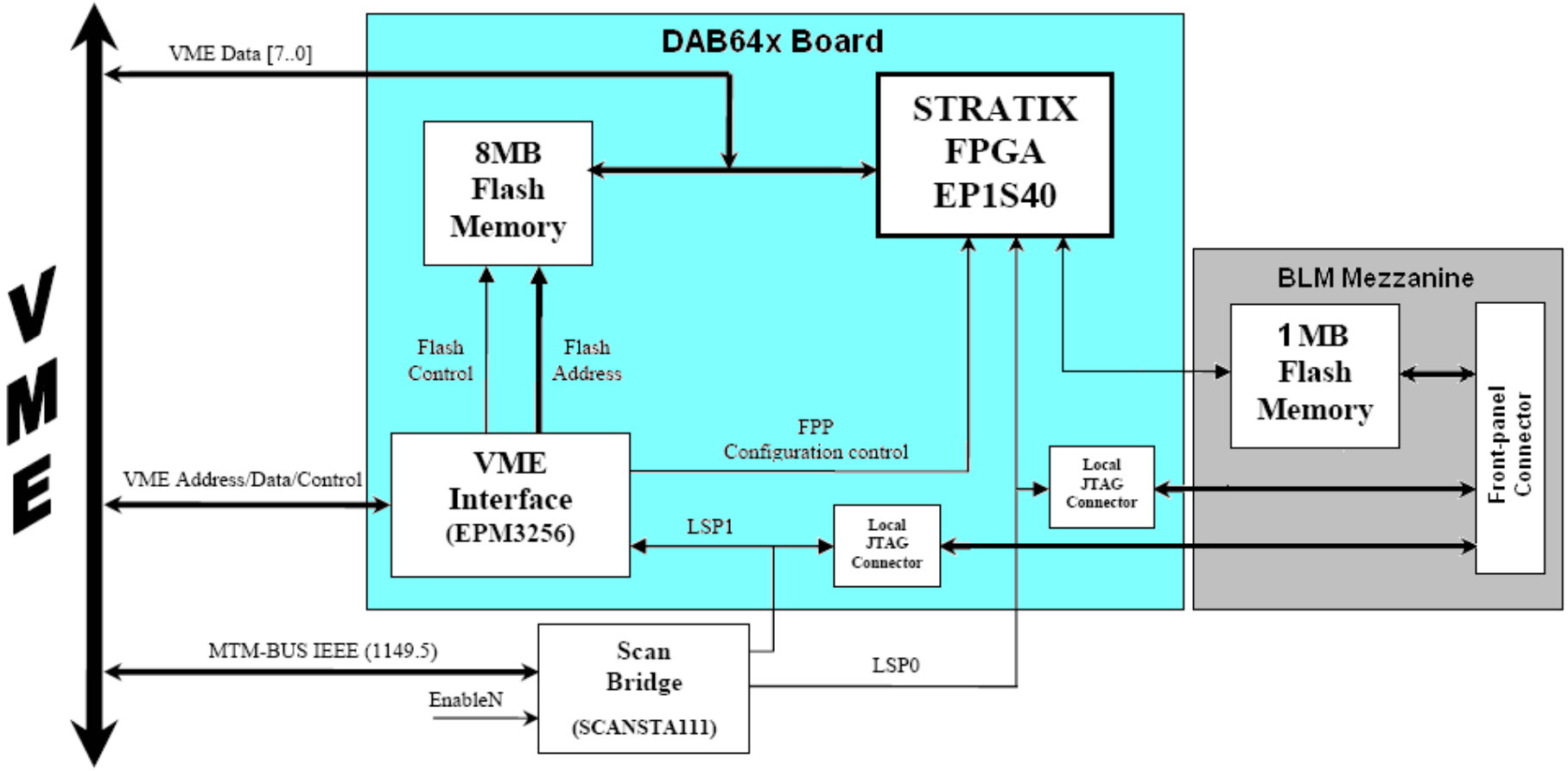
- **A simple solution could be to provide a register that holds information about the number of bits wanted to be shifted right (i.e. divide by 2, 4, 8, 16, …).**

- **Can be unique for each channel.**
- **Its simplicity requires minimum resources.**
- **Secure enough (not possible to increase Thresholds).**
- **Needs to be accessed by the CPU and loaded at every boot.**
- **Adds dependency to the CPU that is against specifications.**

Configuration of the DAB64x

Configuration Data :

- FPGA Firmware
- Card ID
- Threshold Table
- Masking Table

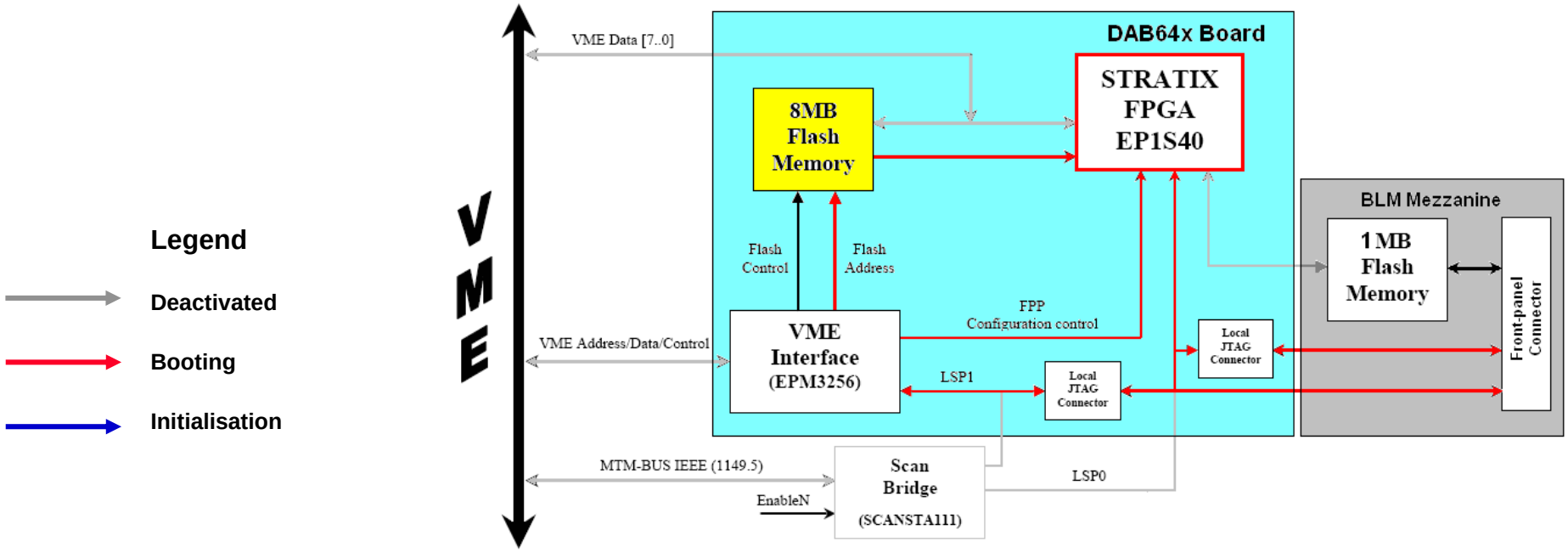


Configuration Scheme (I)

All included in the FPGA Firmware

After the system design finishes the extra information will be embedded in the firmware using a final iteration in the Quartus software.

- ✓ **Single file to be deployed on each card.**
- ✓ **System "instantly" ready after power-on.**
- ✓ **Feature already available/operational.**



Configuration Scheme (II)

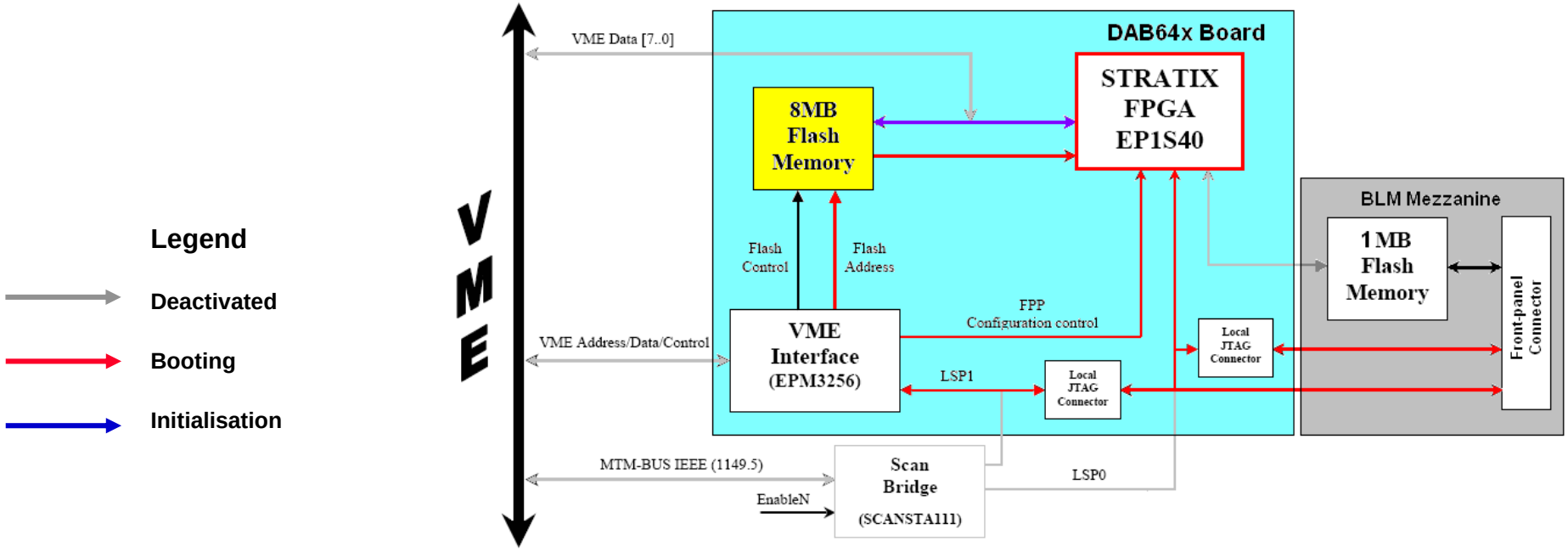
Split of Configuration Memory

Global FPGA Firmware

Unique information will be stored in the unused space of the configuration memory.

After the FPGA boot it will have to fetch the data from the

- ✓ **Multiple files to be deployed for each card.**
- ✓ **More complicated booting procedure.**
- ✓ **Future independence from Quartus Software (?).**



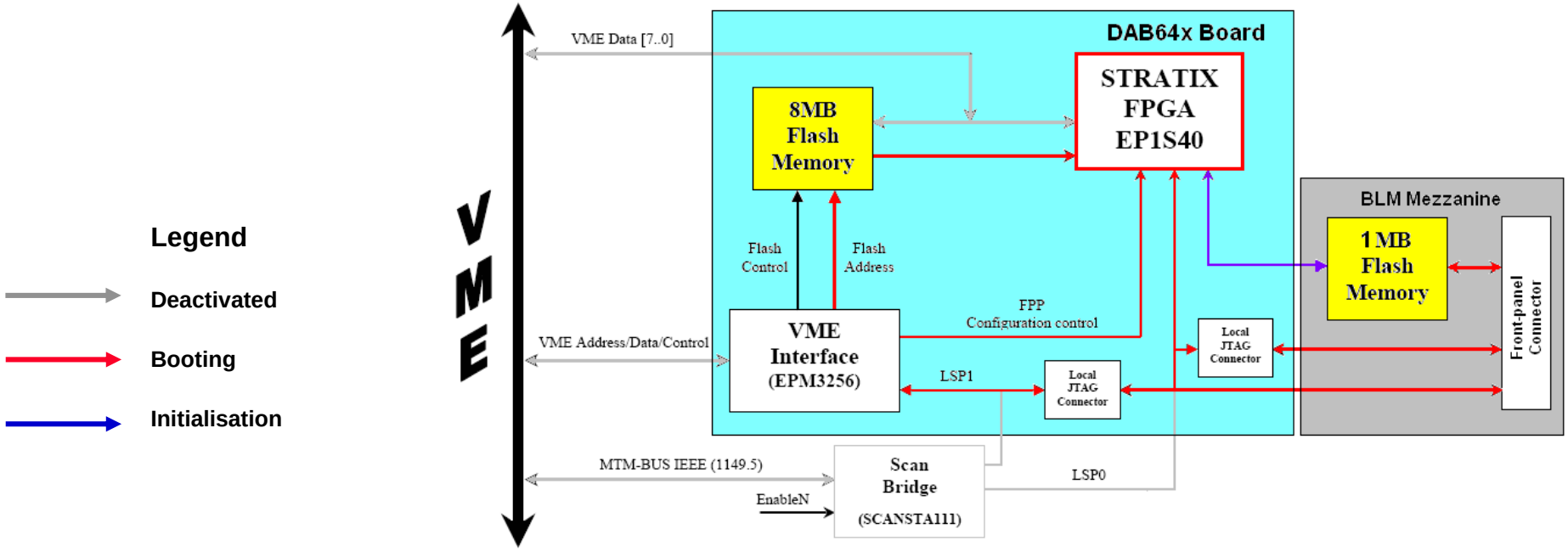
Configuration Scheme (III)

Use of both Flash Memories

Global FPGA Firmware resides on-board.

Unique information will be stored in the mezzanine card's NVRAM.

- ✓ **Multiple files to be deployed for each card.**
- ✓ **Multiple interfaces to be created.**



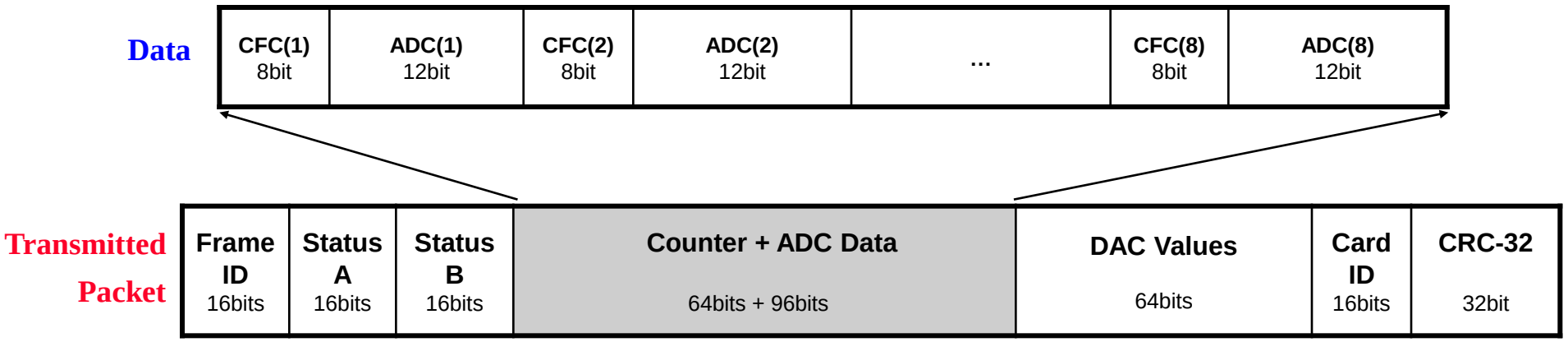
Outlook

- Provide at least one more configuration scheme.
  - Preferably the partition of the configuration memory.
- Implementation of the Post-Mortem data recording and readout.
- Implement differently the Data-Combine process to match better with the CFC card.
  - Not consistent in the region below one count/sec.
- Finalise specifications for the Supervision and Testing procedures.
  - To be proposed at every start-up the Combiner card to increase in steps the Beam energy input.
  - The Logging procedure will provide to the CPU the Thresholds which will be used for that given Beam energy.
  - The CPU will be able to compare them with those stored in a database.
- Test of a complete crate filled with pre-series boards.
  - Setup to be used also by the software people implementing the fixed displays, the Logging and later the Post Mortem.
- Finish the production of the BLM Mezzanine
  - provide a testing procedure of the cards to be installed.

Reserved Slides

Packet from Transmission

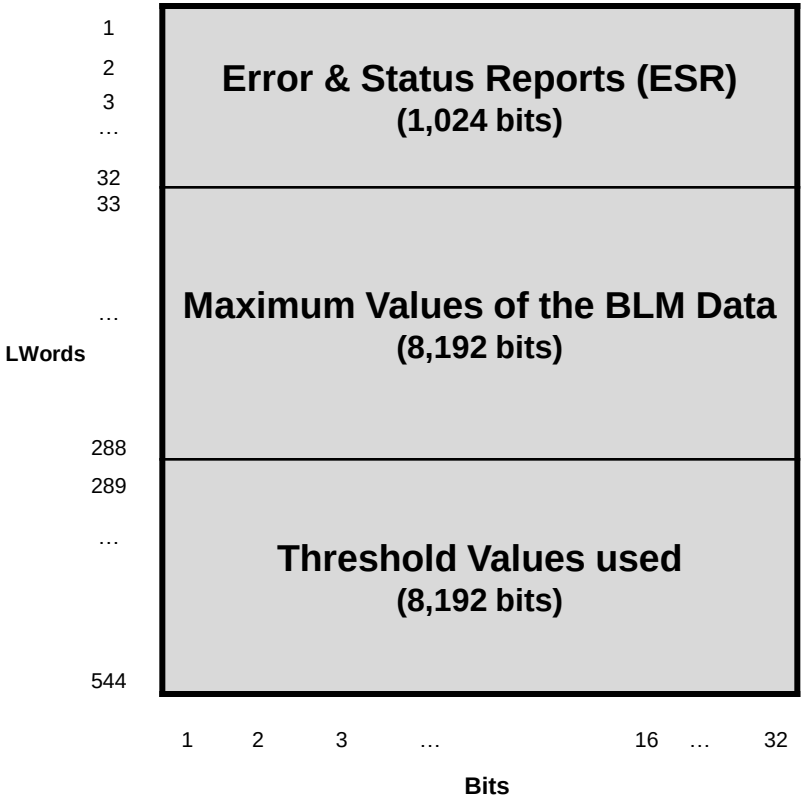
- **Updated formatting of the packet for transmission (now 320 bits)**
  - **Extended the status information**
  - **Included the DAC Values of each channel.**



- **Transmission of packet every 40µs.**
  - **The data rate must be high enough to minimise the total latency of the system .**
- **Redundant optical link**
  - **In order to increase the reliability and the availability of the system.**

Logging Data Arrangement

These data have to be read with a rate of a second in order to be stored in a database as well as to give a graphical representation for the control room.



Read every second:

- *Error & Status* Reports (ESR)(128 Bytes)
- The *Maximum Values* of the BLM Data (1 KB)
- The used *Threshold* values. (1 KB)

Read every Start-up

- Each card's complete *Threshold* table. (32 KB)

  (4,096 x 32bit + 2,048 x 64bit = 6,144 values)

Error & Status Reports (ESR)

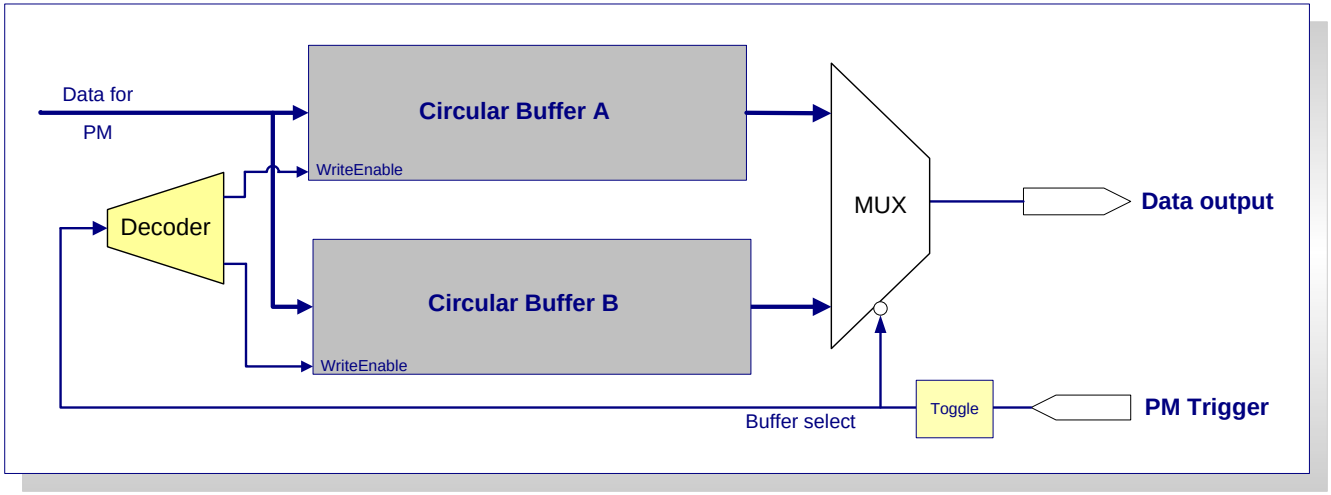
0	00	00FFC400	MaxValue Resets
1	01	00FFC404	ACQs
2	02	00FFC408	Frames to VME
3	03	00FFC40C	Dumps
4	04	00FFC410	VME Acc
5	05	00FFC414	ERRA (CRCa)
6	06	00FFC418	ERRB (CRCb)
7	07	00FFC41C	ERRC (Comp)
8	08	00FFC420	ERRD (CID)
9	09	00FFC424	ERRF (FID)
10	0A	00FFC428	StatusA, StatusB
11	0B	00FFC42C	LostFramesA
12	0C	00FFC430	LostFramesB
13	0D	00FFC434	FID, CID
14	0E	00FFC438	DAC Values 1, 2, 3, 4
15	0F	00FFC43C	DAC Values 5, 6, 7, 8

Information available:

- **ERRA:** number of CRC errors at optical link A
- **ERRB:** number of CRC errors at optical link B
- **ERRC:** different CRCs between A and B
- **ERRD:** wrong Card ID
- **ERRF:** wrong Frame ID
- **Dump:** number of beam dump triggers
- **LostFramesA & LostFramesB**
- **Card ID**
- **Each Detector's DAC value**
- **Voltage and temperature Status**

Post Mortem Data Recording (I)

- **Two circular buffers**
  - A. 2000 turns of both signals received
  - B. Integrals of 10 ms (data needed for further analysis)
- **Double the above buffer and toggle between them using the stop PM recording trigger**
  - Never stop recording (i.e. avoid start input)
  - Test of PM will be possible anytime
  - Accidental/error-triggering proof



Post Mortem Data Recording (II)

- **PM freeze from TTCrx through the backplane.**
- **Time-Stamp appended later by crate CPU.**
  - **At PM freeze the CPU records the time and later when it reads the PM Data appends it to them.**
- **Calculations:**
  - **Minimum required: 1000 turns**

=> 2000 acquisitions * 320 bits packet * 2 packets

=> ~ 160 KB/card * 16 cards/crate = 2.5 MB / crate

  - **Available:**

3xSRAM chips of 512K x 32bit = 6 MB / card