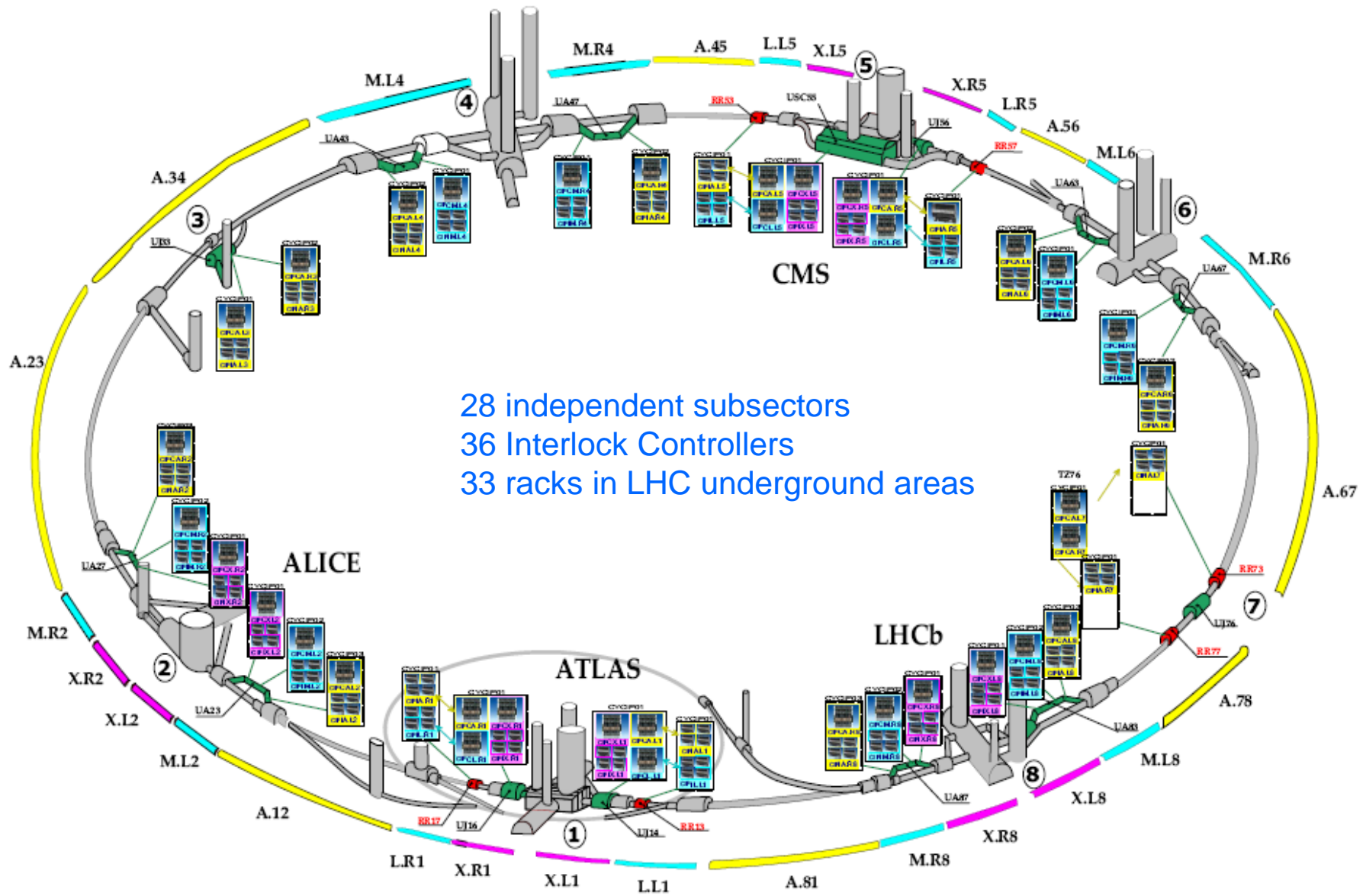




# Secure configuration for the Powering Interlock Controller



J. Blanco AB/CO/MI 29 January 2007



28 independent subsectors  
 36 Interlock Controllers  
 33 racks in LHC underground areas

**PVSS**

**DB**

Startup & Monitoring



Layout DB  
Configuration DB  
CVS



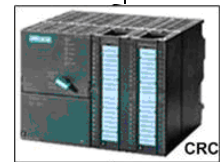
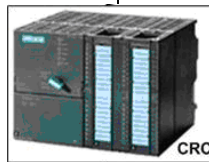
Ethernet

**PLC**

**PLC**

**PLC**

Circuit Protection  
BIC Interface



PROFIBUS

PROFIBUS

PROFIBUS

...

**matrix**

**matrix**

**matrix**

Redundant, fast  
BIC Interface

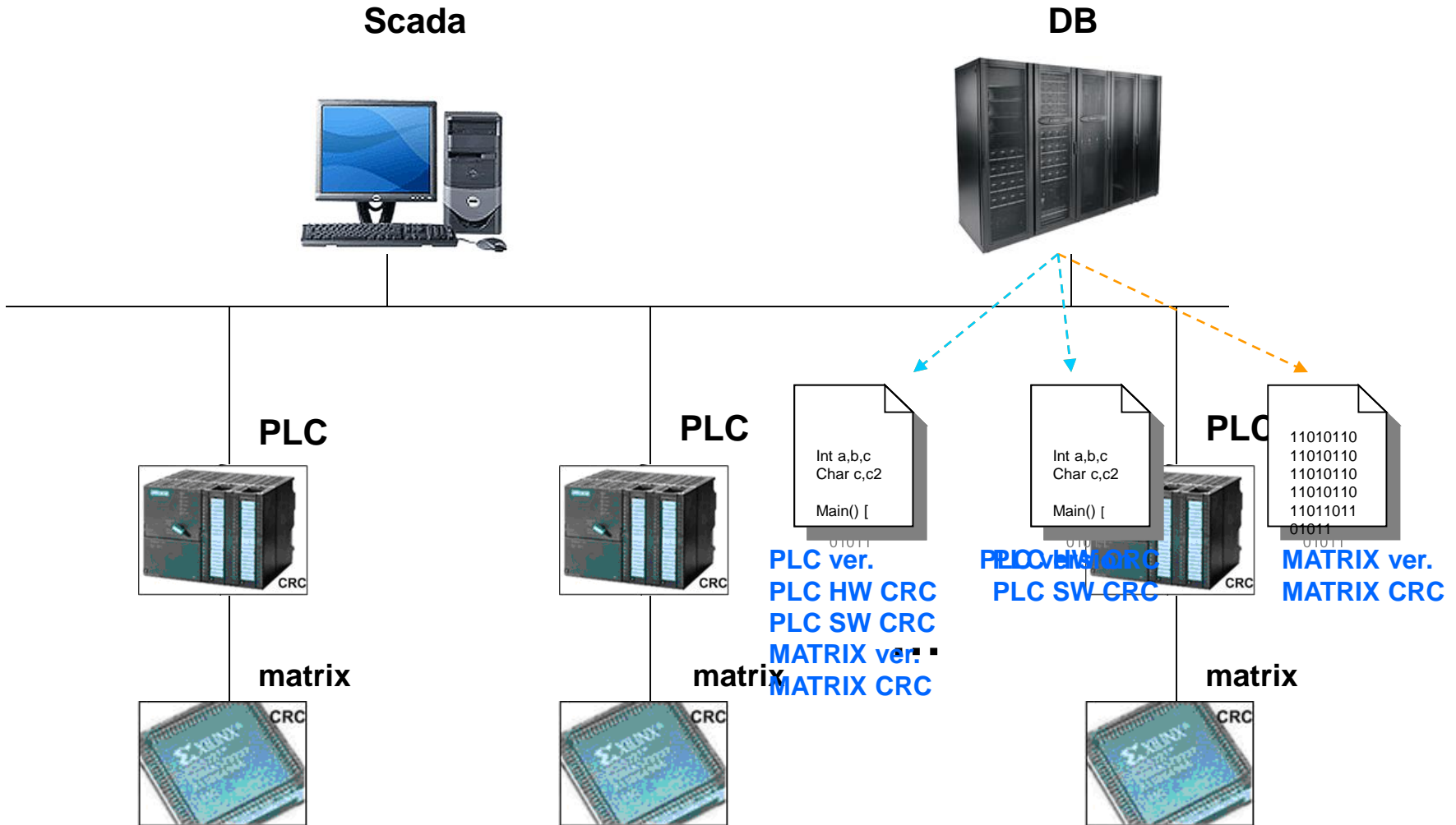




# Aims

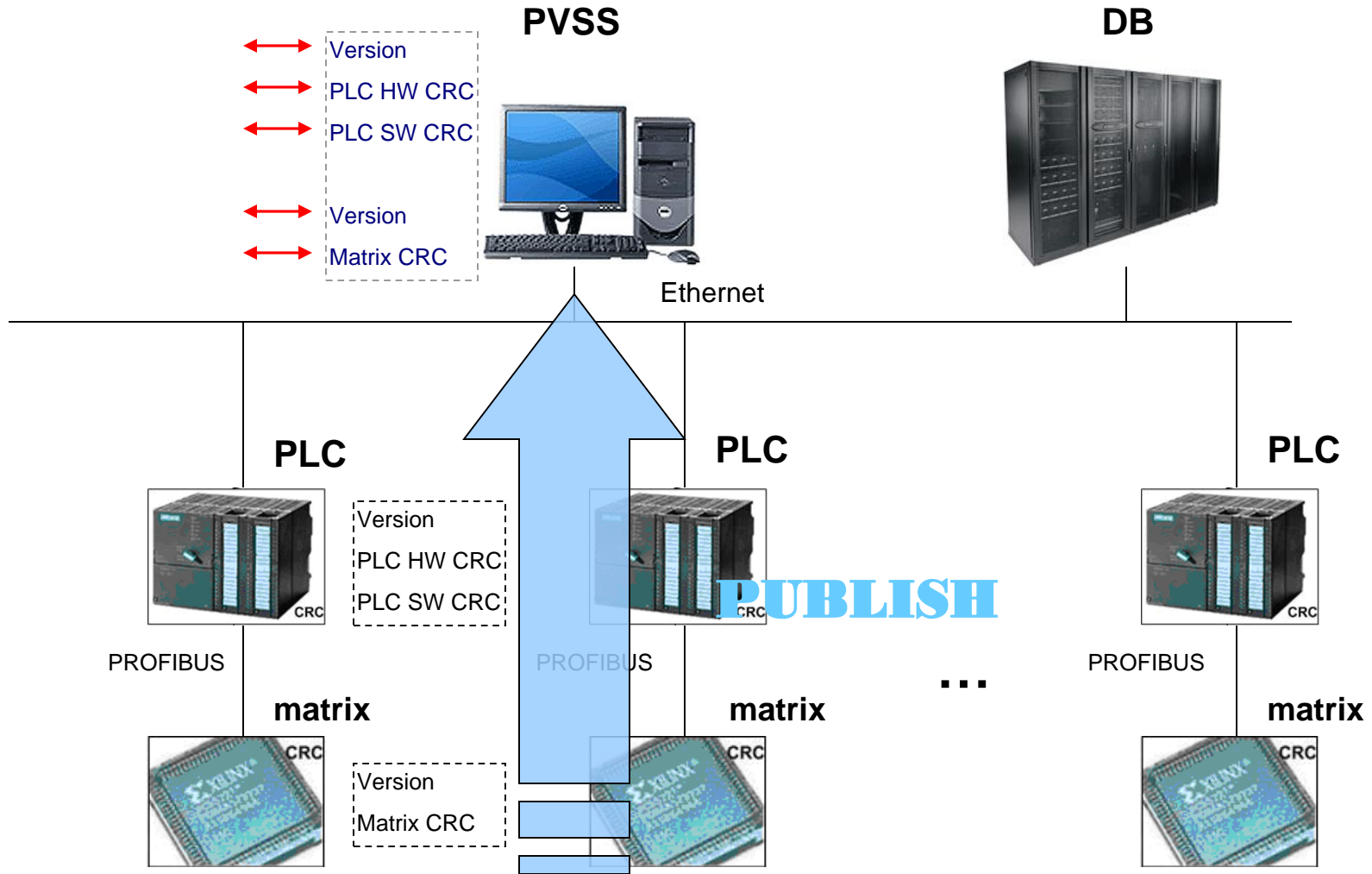


- **Help operations & experts to**
  - Avoid inversion of configuration data between PLC's
  - Assure version integrity between all the software components (PLC, PVSS, Matrix)
  - Assure integrity of configuration data between all the system components (PLC, PVSS, Matrix)
  - Assure the trust of the files downloaded from the DB server
  - Safely change operational parameters without changing hardware configuration
- **Does not protect against**
  - Manual post-editing of configuration data



## Supervision application config file

- The PVSS application is responsible for the consistency of all the configuration data as well as the coherency of the program versions for the CPLD-PLC-PVSS
- It contain
  - Version number of the config file.
  - The CRC's for the PLC and CPLD
  - The versions of the PLC and CPLD code.
- The overall coherency will depend on the correctness of the PVSS configuration file.



- Enable/Disable 'Give Permit' command at PVSS level.

**CIP.UA83.ML8**

CFP UA83 CIPML8 DATA Connection OK

**CIP.UA83.ML8**

CONFIGURATION DATA OK  Refresh

**Versions**

PLC side		PVSS side
A38D4091	PLC HW config	A38D4091
178B833A	PLC SW config	178B833A
2	PLC version	2
D2	Matrix config	D2
15	Matrix version	15

**Informations**

PVSS PIC component	4
PIC ID	4F316
PLC Restarts	21

**Settings**

MATRIX validity period (s.)	3600	Apply
-----------------------------	------	-------

**Status**

QPS OK

Circuit OK

Ready to Permit    **Forced**

Permit I    **Seq**

Permit II    **Seq**

Signal Init Forced Mode Give All Remove All **Select**



- Every time a Faceplate of a PIC is opened in the SCADA systems all 5 parameters are verified.
- Before a ‘give permit’ command is sent, the 3 PLC related parameters (HW CRC, SW CRC, Version) are checked. The 2 CPLD parameters (CRC, Version) are verified only if the last verification is older than a maximum of 1 hour.
- Every time a ‘give permit all’ is sent all the parameters are verified.

CIP.UA83.ML8 Powering interlock controller for the matching sec...  
CIP.UA83.ML8

CONFIGURATION DATA OK  Refresh

Versions

PLC side		PVSS side
A38D4091	PLC HW config	A38D4091
178B833A	PLC SW config	178B833A
2	PLC version	2
D2	Matrix config	D2
15	Matrix version	15

Informations

PVSS PIC component	4
PIC ID	4F316
PLC Restarts	21

Settings

MATRIX validity period (s.)	3600	Apply
-----------------------------	------	-------

CIP.UA83.ML8 Powering interlock controller for the matching sec...  
CIP.UA83.ML8

CONFIGURATION DATA BAD  Refresh

Versions

PLC side		PVSS side
A38D4091	PLC HW config	BE6A6587
178B833A	PLC SW config	AB404AAA
2	PLC version	2
D2	Matrix config	D2
15	Matrix version	15

Informations

PVSS PIC component	4
PIC ID	4F316
PLC Restarts	21

Settings

MATRIX validity period (s.)	3600	Apply
-----------------------------	------	-------

- After download from database, all configuration data will be archived in CVS
- Validation during hardware commissioning

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Click on a directory to enter that dire

Current directory: [pico - PIC Conf](#)

## CIP\_Config\_Data/CIP.UA83.XL8/

Click on a directory to enter that directory. Click on a file to display its revision history and to get a chance to display diffs between revisions.

Current directory: [pico - PIC Configuration Files](#) / [CIP Config Data](#) / CIP.UA83.XL8

File
<a href="#">Parent Directory</a>
<a href="#">CIP.TZ76.AL7/</a>
<a href="#">CIP.TZ76.AR7/</a>
<a href="#">CIP.UA23.AL2/</a>
<a href="#">CIP.UA23.ML2/</a>
<a href="#">CIP.UA23.XL2/</a>
<a href="#">CIP.UA27.AR2/</a>
<a href="#">CIP.UA27.MR2/</a>
<a href="#">CIP.UA27.XR2/</a>
<a href="#">CIP.UA43.AL4/</a>
<a href="#">CIP.UA43.ML4/</a>
<a href="#">CIP.UA47.AR4/</a>
<a href="#">CIP.UA47.MR4/</a>
<a href="#">CIP.UA63.AL6/</a>
<a href="#">CIP.UA63.ML6/</a>

File	Rev.	Age	Author	Last log entry
<a href="#">Parent Directory</a>				
<a href="#">PIC UA83 XL8.zip</a>	<a href="#">1.1</a>	7 weeks	jblancos	PLC program Version 1.7 PLC config Version: 2.0 Remarks: Cryo Comm PLC-PLC spec...
<a href="#">PIC UA83 XL8 No PSoft.zip</a>	<a href="#">1.1</a>	7 weeks	jblancos	PLC program Version 1.7 PLC config Version: 2.0 Remarks: Cryo Comm PLC-PLC spec...
<a href="#">matrixcode CIP UA83 XL8.jed</a>	<a href="#">1.1</a>	8 weeks	jmarieth	Add of the matrix compiled code
<a href="#">matrixmask CIP UA83 XL8.txt</a>	<a href="#">1.1</a>	2 months	jmarieth	*** empty log message ***
<a href="#">plcD CIP UA83 XL8.txt</a>	<a href="#">1.2</a>	2 months	jmarieth	New version number for PLC_SW (2.0) and CPLD (15) New URL for [html page]
<a href="#">plc CIP UA83 XL8.txt</a>	<a href="#">1.2</a>	2 months	jmarieth	New version number for PLC_SW (2.0) and CPLD (15) New URL for [html page]
<a href="#">pvss CIP UA83 XL8.txt</a>	<a href="#">1.4</a>	5 weeks	jmarieth	New header field containing the list of PC connected to the PIC

Show only files with tag:  Module path or alias:



- Adding equipment or electrical circuits
  - Probability very low.
  - Imply changes in the PC, QPS and PIC.
  - Imply changes in the Hardware part of the config data → re-commissioning must be done.
- Removing equipment or electrical circuits defined as Auxiliary (corrector circuits)
  - High probability.
  - PC powering that circuit should be switched off and the interlock cable should be disconnected.
  - No config file modifications needed.
- Removing equipment or electrical circuits defined as Essential (main circuits)
  - Low probability.
  - Should be redefined as auxiliary → SW part of PLC config file needs to be modified as well as the MATRIX mask.



# Changes of operational parameters



- **Change the 'POWERING SUBSECTOR OFF' flag**
  - Low probability.
  - Update the Software part of the PLC config file.
  - Quick functional test of the modification from the CCC sufficient
- **Change the 'BEAM DUMP' FLAG**
  - Medium-low probability.
  - Update the Software part of the PLC config file.
  - Change the MATRIX mask of the CPLD.
  - Quick functional test of the modification from the CCC sufficient

- ES summarizing the design issues finalized and will soon be distributed for engineering check
- Similar ideas implemented for PLC systems as MCS for VME front-ends to
  - Later integration into MCS?
- Assist operations with configuration management and changes of operational parameters

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LHC Project Document No. LHC-S-PIC-0001 rev 0.3
CERN Div./Group or Supplier/Contractor Document No. AB/CO
EDMS Document No. 999999
Date: 2006-12-12

## Functional Specification

### THE COMMISSIONING OF THE HARDWARE IN THE LHC SECTORS

### SOFTWARE AND SECURE CONFIGURATION FOR THE POWERING INTERLOCK SYSTEM

#### Abstract

This document describes the software functionalities of the industrial controllers and the associated supervision system of the powering interlock system. It describes in detail the implemented protection mechanisms and the way to securely configure and change the associated operational parameters. Several failure and maintenance scenarios are described and the procedures for a correct reconfiguration of the system are defined. After their initial deployment for the powering interlock system of sc magnets (PIC), the same mechanisms will be put in place for the protection of nc magnets (WIC).

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