Fast beam current change monitor "$\frac{di}{dt}$"

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July 2, 2009

Measurement devices

- totally 8 Fast Beam Current Transformers (FBCTs)
- 4 FBCTs in rings (FBCTR), 2 FBCTRs per beam, installed in UA47 (racks BY10, BY11)
- provide measurements on bunch and turn basis[1], two different bandwidths (200MHz bunch-bunch, ≈2.5MHz for time insensitive turn-turn measurements), two different gains (2×10^{10} and 2×10^{11} charges)
- measurement systems distributed into two racks. if one rack fails measurement can be provided by other one (development)
- two monitors (one per beam) are connected to CIBUD to provide information whether there is a circulating beam. The threshold is currently set to $\approx 3 \times 10^{9}$p.

[1] EDMS 359172

$\frac{dI}{dt}$ FUNCTIONAL SPECIFICATION

FBCTRs are connected to BIS via CIBU(D). They will ensure that total beam loss over few turns does not exceed predefined threshold.

- loss is calculated from turn by turn measurements
- calculation involves a lot of factors (filtering, DC signal restoration, calibration factors etc.), must be done almost on-fly (in hardware) $\longrightarrow$ right settings matter of compromise. **Proposal:** settings stored in Critical Settings Management (MCS) system.
- measurement relies on Beam Synchronous Timing (BST): no BST $\longrightarrow$ no intensity measurement $\longrightarrow$ trigger beam dump

Interlock trigger conditions

- two thresholds defined:
  - DUMP intensity loss: beam dump will be requested
  - ALARM intensity loss: alarm shall be generated
- and two moving windows per measurement applied on data. This permits triggering on a) fast loss over a small number of turns, b) small loss over many turns
- low-bandwidth measurements (lower noise, timing insensitive) used.
- appropriate gain channel selection done automatically.

Algorithms implemented in FPGA, all required values entered via FESA taking into account calibration coeffs for FBCT in question.

Input data requirements

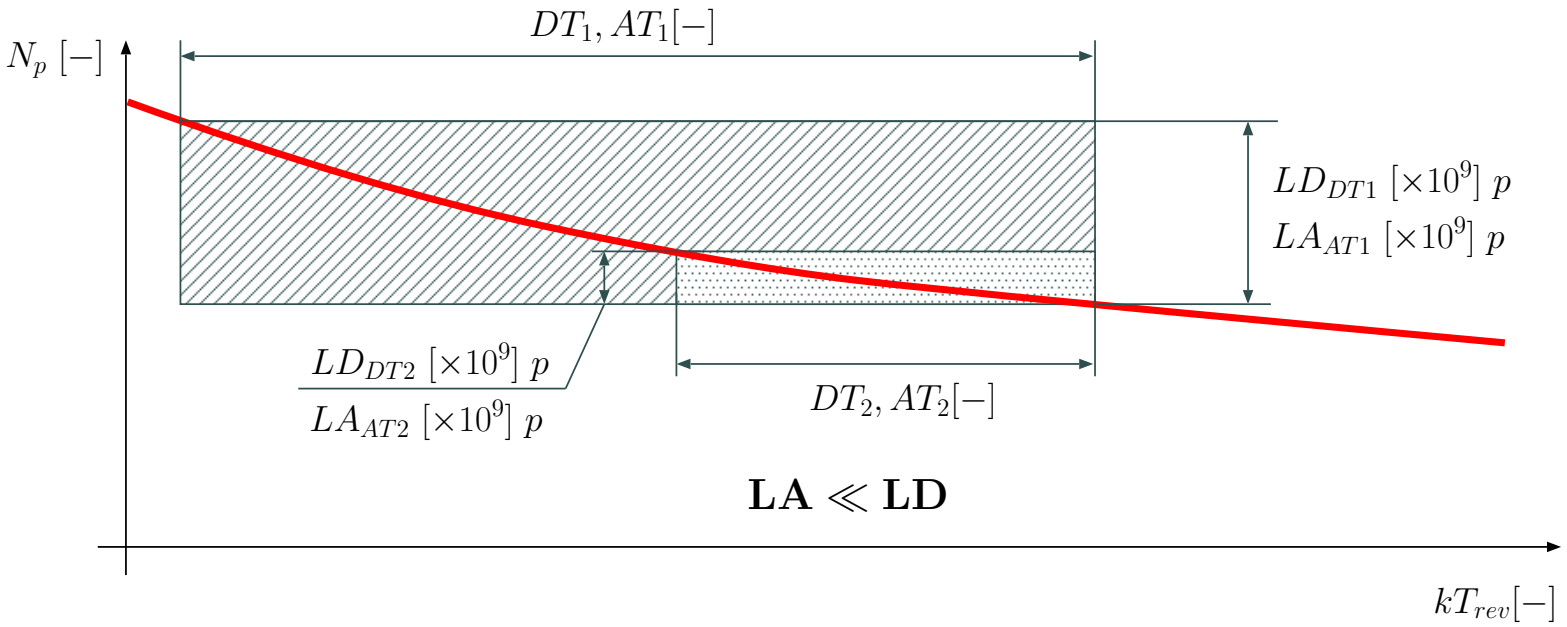

Figure: Different moving windows evaluating losses

- *LD*, *LA*: losses expressed in $\times 10^9$ charges
- *DT*, *AT*: window sizes, expressed in number of turns

Connection to the BIC system

- each FBCTR will provide an output signal for CIBU (double output of the same signal generated at FPGA level)
- having "operational" and "development" systems imposes that only "operational" system will now provide information
- once "development" becomes "operational 2" the signals will be regrouped and "**AND**" combination for beam1 and beam2 will be provided
- interlock is failsafe - whatever goes wrong (out of tolerance, cabling problems in our systems ...) results in request for dump
- interlock must be maskable to allow setting up of the beam with safe beam

Open points

- minimum and maximum limits for number of turns for moving windows calculations
- threshold values in number of charges to be defined
- CIBU connection