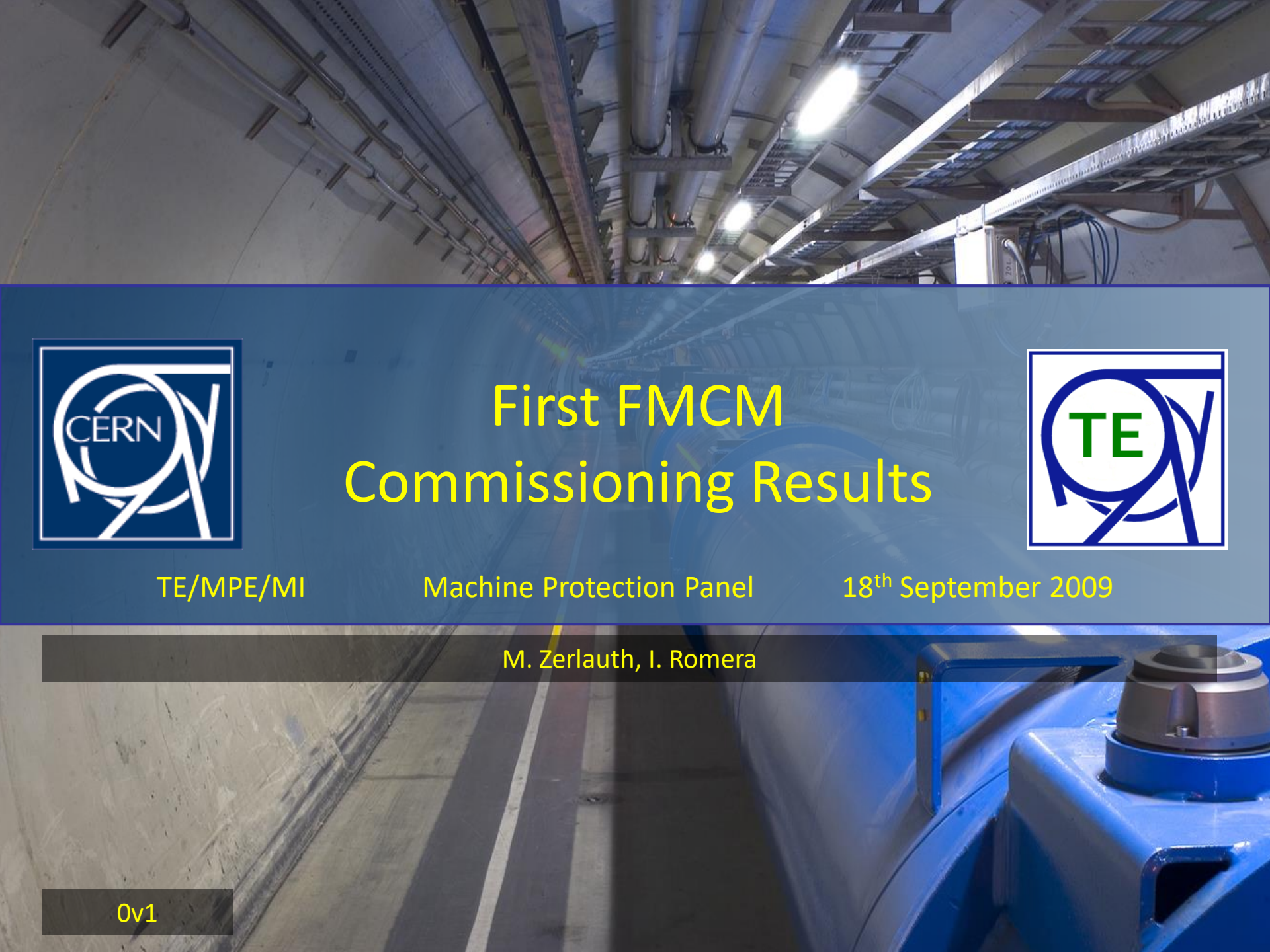


First FMCM Commissioning Results

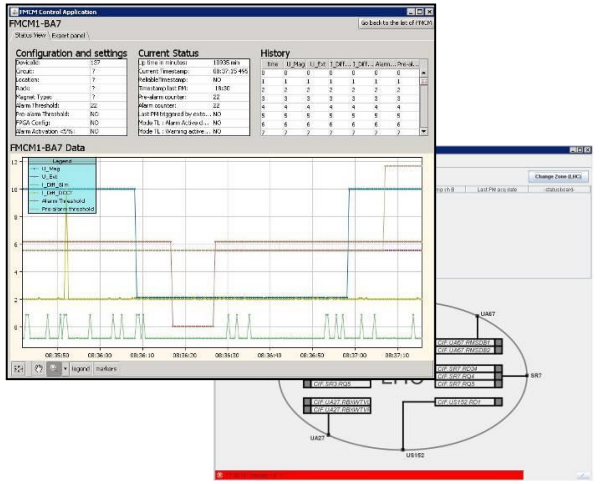
TE/MPE/MI Machine Protection Panel 18th September 2009

M. Zerlauth, I. Romera

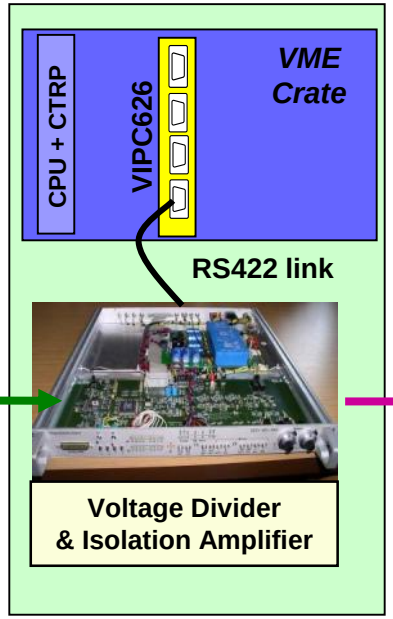
0v1

FMCM @ LHC

- 14 Fast Magnet Current Change Monitors already successfully commissioned and in operation for some 2 years in TI2, TI8/CNGS
- 12 additional FMCMs installed on nc circuits of LHC
  - Separation dipoles RD1.LR1, RD1.LR5
  - RQ4.LR3/7, RQ5.LR7, RD34.LR3/7
  - Dump septas RMSD.LR6B1/2
  - ALICE compensators RBXWTV.R2/L2
- Functionality slightly different from TL
  - no fast cycling magnets
  - continuous Beam Permit instead of Permit window
  - Interlock only active > 5% of Unom
  - Need to detect $\Delta I/I$ of $3.5*10^{-4}$ in <1ms
  - Installed in BIC racks, cables >>



Ethernet



Measurement of PC or circuit voltage

Beam Dump to BIS

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Protection of nc circuits

Beam Dump to BIS

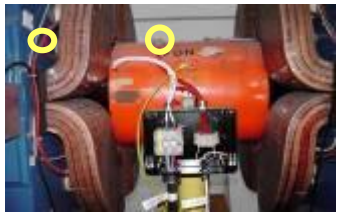
WIC

Status info

Power Permit

Power Converter

Thermo-switches @ 60°C + Water Flow



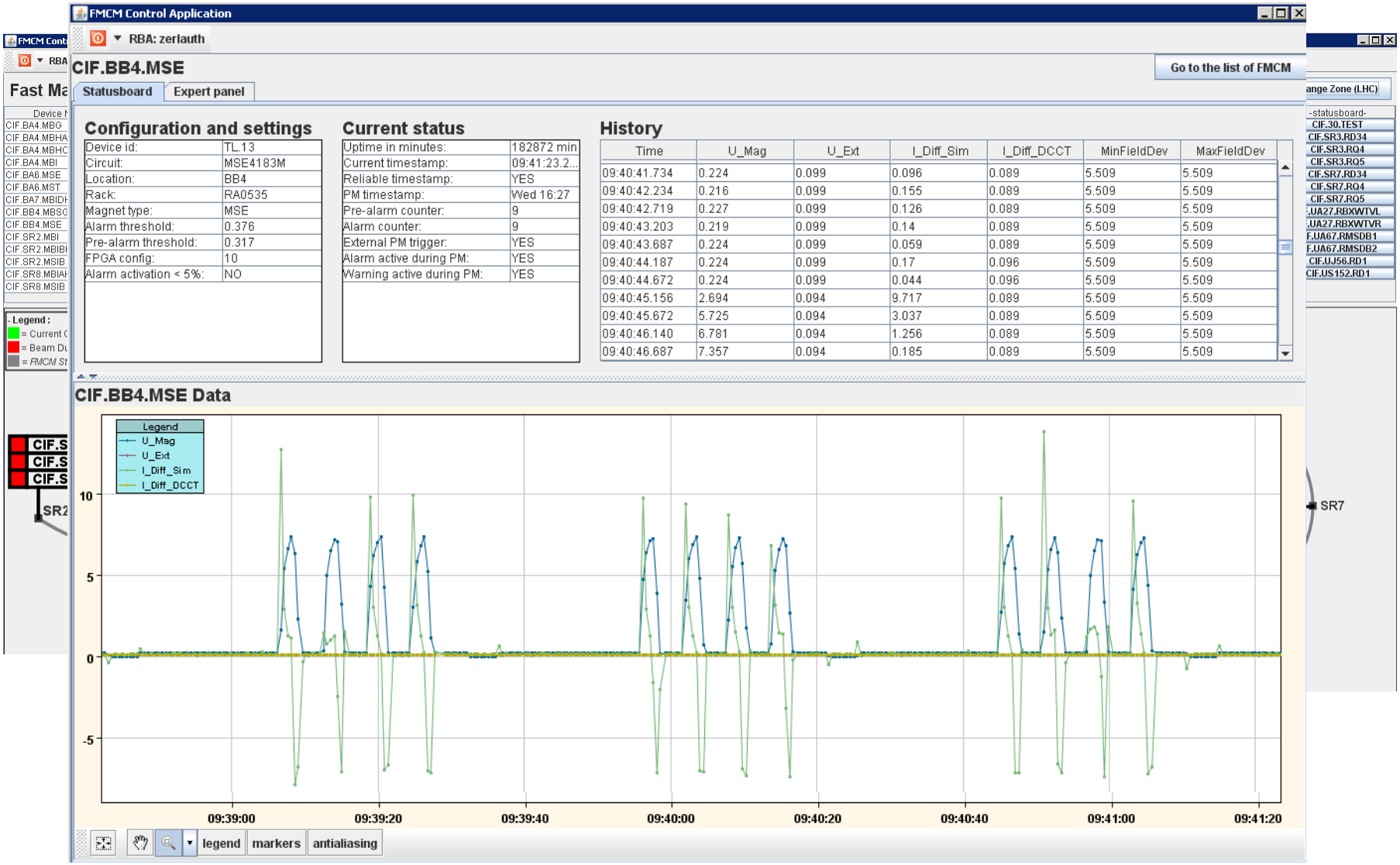
Thermo-switches @ 60°C + Water Flow

RQ4.LR3/7
RQ5.LR3/7
RD34.LR3/7

RD1.LR1/5
RMSD.LR6B1/2
RBXWTV.R2/L2

Beam Dump to BIS

FMCM Supervision



Courtesy of N.Hoibian

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1st MPS dry-runs in IR2

- Gather first experience for MPS checkout of FMCMs in LHC to
  - Establish conditions for the tests
  - Setting up and tuning of devices
  - Test procedures and duration
  - Documentation of results

- Profit from HCC powering phase 1 in S12, prepared nc circuits of IR2 for test on 1st of September

  +

- Dry-runs for automated procedures to test Beam Permit exchange of main clients with BIS (FMCM, WIC, BLM, BTV,…)
- Successfully validated first version of sequences in operational environment
- See future presentation of I.Romera

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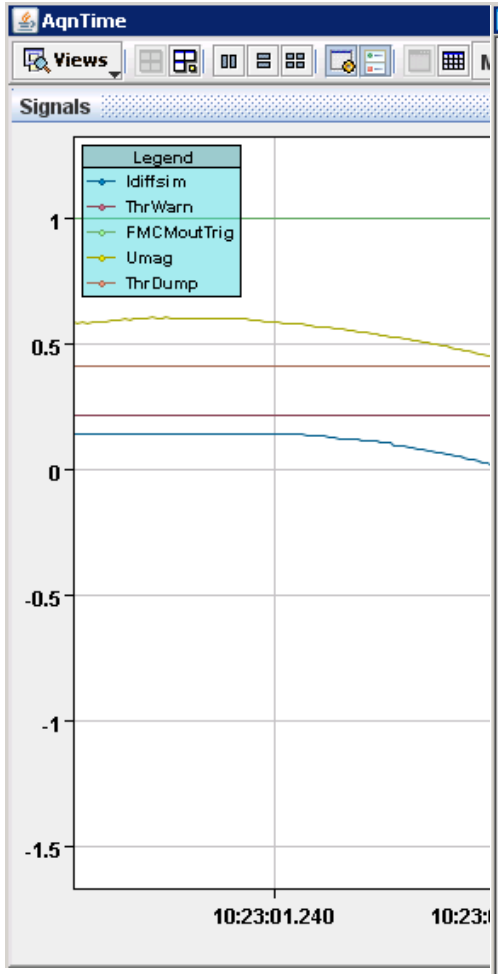
Results I_INJECTION

- Test at I_INJ (Ramp to I_INJ and provoke FGC_STATE Fault)



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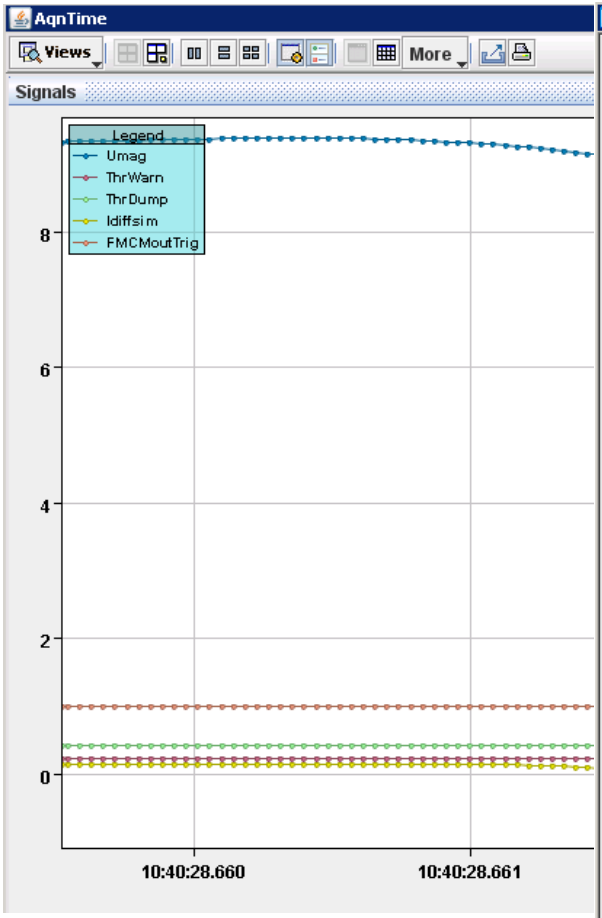
- Test at I_INJ (Ramp to I_NOM and provoke FGC_STATE Fault)



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Conclusions

- Tests were executed as specified in document, <30 min / device
- FMCM performed (better) than expected, due to slow ramps and more stable supplies
- Requirements met without difficulties, still > margin in detection threshold
- For operation thresholds probably to be relaxed in favor of stability (determined not by noise but mainly by di/dt & acc = change of voltage at start / end of PLEP)
- Add additional test for failure case of V_max applied by converter when at I_INJ in procedure (see studies of A. Gomes Alonso)
- For FMCM and WIC, MPS tests could be scheduled at early stage – what is an early (but still safe) date to start (still >> interventions ongoing)

- Nice surprise: Due to new FM352 module, the WIC reacts for this failure case well before the FMCM (internal fault signaled by PC before the output stage is switched off)

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- MPS share-point site: https://espace.cern.ch/LHC-Machine-Protection

Machine Protection web site

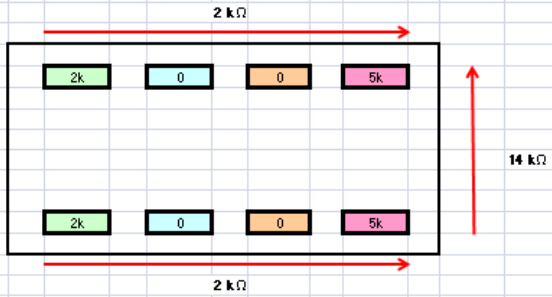
Machine Protection web site

View: Resume

ns Tested | Repetition | Status

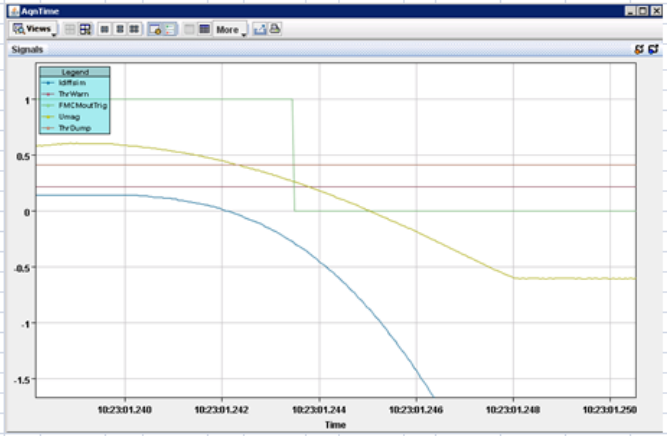
MPS Checkout for Device	CIF.UA27.RBXWTVL		
Device Id; Location	HCCIF_____-DS000028; CYCIB01=UA27		
Date	04. Sept 2009		
Time	10.00 - 10.40		
Warning Threshold	0.4		
Dump Threshold	0.2		
I_DIFF_SIM DURING RAMP	0.05	V	
I_DIFF_SIM @ FLAT TOP	0.0022	V	
I_nom	600	A	
I_Inj	40		
U_mag @ I_nom (600A)	3.5	V	Adjusted!
U_mag @ I_Inj (40A)	0.6	V	
FMCM trigger @ Injection @ I_nom	YES		

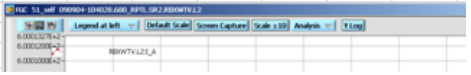
Voltage Divider Settings for test (adjustable Isolation Amplifier!)



Test at I_INJ (Ramp to I_INJ and provoke FGC_STATE Fault)

Time	10:23:01		
A&B WIC trigger @	10:23:01.	238264	
A&B FMCM trigger @	10:23:01.	243489	
Δt [FMCM-WIC]	5.225	ms	
I @ trigger of WIC	40	A	
I @ trigger of FMCM	39.999	A	
ΔI/I [WIC]	0	1.E-04	
ΔI/I [FMCM]	0.25	1.E-04	Specification > 3.5 E-4





Test at I_NOM (Ramp to I_NOM and provoke FGC_STATE Fault)

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FIN

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