Changes in Powering Interlocks during X-mas shut-down

Changes during X-mas shut-down

- **Firmware upgrade** in all 36 PIC PLCs
  - Possibility for extended diagnostics (e.g. in case of memory corruptions on CIP.UJ14.LL1 on 11-AUG-10 06:00 PM,…)
  - Lab tests ongoing, will be transparent

- **Upgrade of PIC PVSS SCADA**, including two relevant new features
  - **AUTOMATIC HEATER DISCHARGE**: in case of loss of >=2 heaters for MB and >=1 heaters for individually powered magnets (IPQ, IPD, IT)
    - Validation prior/during HWC phase
  - **SECTOR_ACCESS**: Procedures released and mechanism integrated into in LHC sequencer
    - Validation during HWC phase

- **Replacement of CIPAA board in CIP.UA87.AR8** which was exchanged following incident in mid September 17th
  - Complete re-commissioning during HWC phase

Hardware (re)-commissioning

CIRCUIT NAME	LAST PASSED TEST	TESTS EXEC	LAST EXEC	SUC	UNDER EXEC						
RCBXH1.R1	24 HOUR HEAT RUN	0 / 11 (0%)	_	_	_	PCL	PCC.5	PIC2 CRYO-OK	PIC2 QPS-OK	PIC2 PC PERMIT	PIC2 POWERING FAILURE
RCBXH2.R1	24 HOUR HEAT RUN	0 / 11 (0%)	_	_	_	PCL	PCC.5	PIC2 CRYO-OK	PIC2 QPS-OK	PIC2 PC PERMIT	PIC2 POWERING FAILURE
RCBXH3.R1	24 HOUR HEAT RUN	0 / 11 (0%)	_	_	_	PCL	PCC.5	PIC2 CRYO-OK	PIC2 QPS-OK	PIC2 PC PERMIT	PIC2 POWERING FAILURE
RCBXV1.R1	24 HOUR HEAT RUN	0 / 11 (0%)	_	_	_	PCL	PCC.5	PIC2 CRYO-OK	PIC2 QPS-OK	PIC2 PC PERMIT	PIC2 POWERING FAILURE
RCBXV2.R1	24 HOUR HEAT RUN	0 / 11 (0%)	_	_	_	PCL	PCC.5	PIC2 CRYO-OK	PIC2 QPS-OK	PIC2 PC PERMIT	PIC2 POWERING FAILURE
RCBXV3.R1	24 HOUR HEAT RUN	0 / 11 (0%)	_	_	_	PCL	PCC.5	PIC2 CRYO-OK	PIC2 QPS-OK	PIC2 PC PERMIT	PIC2 POWERING FAILURE
RQSX3.R1	24 HOUR HEAT RUN	0 / 12 (0%)	_	_	_	PCL	PCC.5	PIC2 CRYO-OK	PIC2 QPS-OK	PIC2 PC PERMIT	PIC2 POWERING FAILURE

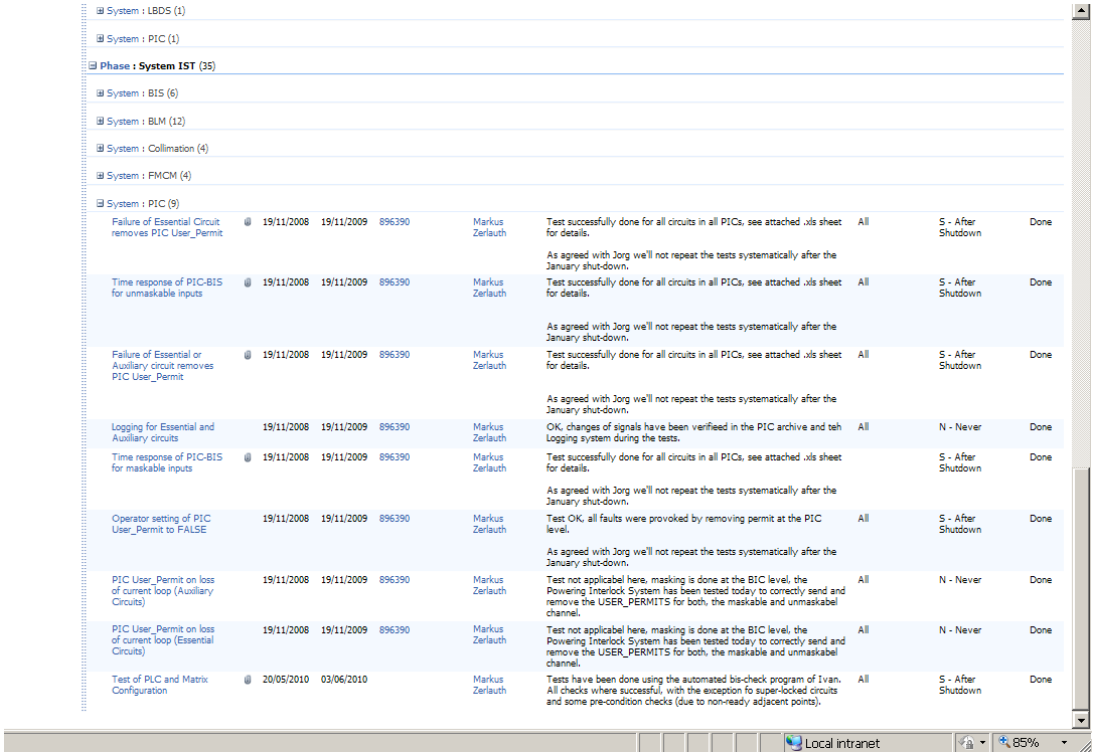
EXECUTION PLAN						
PIC2 CIRCUIT QUENCH VIA QPS	PIC2 FAST ABORT REQ VIA PIC	PIC2 TEST HW LINKS	PCS	PNO.d3	PNO.a3	PIC2 GLOBAL PROTEC.MECH
PIC2 CIRCUIT QUENCH VIA QPS	PIC2 FAST ABORT REQ VIA PIC	PIC2 TEST HW LINKS	PCS	PNO.d3	PNO.a3	PIC2 GLOBAL PROTEC.MECH
PIC2 CIRCUIT QUENCH VIA QPS	PIC2 FAST ABORT REQ VIA PIC	PIC2 TEST HW LINKS	PCS	PNO.d3	PNO.a3	PIC2 GLOBAL PROTEC.MECH
PIC2 CIRCUIT QUENCH VIA QPS	PIC2 FAST ABORT REQ VIA PIC	PIC2 TEST HW LINKS	PCS	PNO.d3	PNO.a3	PIC2 GLOBAL PROTEC.MECH
PIC2 CIRCUIT QUENCH VIA QPS	PIC2 FAST ABORT REQ VIA PIC	PIC2 TEST HW LINKS	PCS	PNO.d3	PNO.a3	PIC2 GLOBAL PROTEC.MECH
PIC2 CIRCUIT QUENCH VIA QPS	PIC2 FAST ABORT REQ VIA PIC	PIC2 TEST HW LINKS	PCS	PNO.d3	PNO.a3	PIC2 GLOBAL PROTEC.MECH
PIC2 CIRCUIT QUENCH VIA QPS	PIC2 FAST ABORT REQ VIA PIC	PIC2 TEST HW LINKS	PCS	PNO.d3	PNO.a3	PIC2 GLOBAL PROTEC.MECH

- From PIC side, **re-commissioning after short shut-down or HW intervention** on interlock systems should be considered **identical** (aiming at full automation)
- Goal of re-commissioning is to **re-test all HW interlock functions** + (eventually SW interlocks if relevant changes have been applied) ~ 2000 tests
- Drop SW related tests (tbc with other system experts), drop PIC1, drop PC Permit test (as exercised in all other tests) -> **implicit validation via Logging**,…

Tests prior/during beam commissioning

- Possible **modification of PIC-BIC configuration** after HWC period (NC circuits have to be re-included in the configuration), either way a re-validation is advisable
  - **Use of automatic tools**, estimate ~ 4-5 hours for all machine ?
  - Preparing **integration into LHC sequencer** for regular execution

  - https://espace.cern.ch/LHC-Machine-Protection/Lists/MachineProtectionList/Resume.aspx



System : LBDS (1)
System : PIC (1)
Phase : System IST (35)
System : BIS (6)
System : BLM (12)
System : Collimation (4)
System : FMCM (4)
System : PIC (9)

Failure of Essential Circuit removes PIC User_Permit	19/11/2008	19/11/2009	896390	Markus Zerlauth	Test successfully done for all circuits in all PICs, see attached .xls sheet for details. As agreed with Jorg we'll not repeat the tests systematically after the January shut-down.	All	S - After Shutdown	Done
Time response of PIC-BIS for unmaskable inputs	19/11/2008	19/11/2009	896390	Markus Zerlauth	Test successfully done for all circuits in all PICs, see attached .xls sheet for details. As agreed with Jorg we'll not repeat the tests systematically after the January shut-down.	All	S - After Shutdown	Done
Failure of Essential or Auxiliary circuit removes PIC User_Permit	19/11/2008	19/11/2009	896390	Markus Zerlauth	Test successfully done for all circuits in all PICs, see attached .xls sheet for details. As agreed with Jorg we'll not repeat the tests systematically after the January shut-down.	All	S - After Shutdown	Done
Logging for Essential and Auxiliary circuits	19/11/2008	19/11/2009	896390	Markus Zerlauth	OK, changes of signals have been verifieed in the PIC archive and teh Logging system during the tests.	All	N - Never	Done
Time response of PIC-BIS for maskable inputs	19/11/2008	19/11/2009	896390	Markus Zerlauth	Test successfully done for all circuits in all PICs, see attached .xls sheet for details. As agreed with Jorg we'll not repeat the tests systematically after the January shut-down.		S - After Shutdown	Done
Operator setting of PIC User_Permit to FALSE	19/11/2008	19/11/2009	896390	Markus Zerlauth	Test OK, all faults were provoked by removing permit at the PIC level. As agreed with Jorg we'll not repeat the tests systematically after the January shut-down.	All	S - After Shutdown	Done
PIC User_Permit on loss of current loop (Auxiliary Circuits)	19/11/2008	19/11/2009	896390	Markus Zerlauth	Test not applicabel here, masking is done at the BIC level, the Powering Interlock System has been tested today to correctly send and remove the USER_PERMITS for both, the maskable and unmaskabel channel.	All	N - Never	Done
PIC User_Permit on loss of current loop (Essential Circuits)	19/11/2008	19/11/2009	896390	Markus Zerlauth	Test not applicabel here, masking is done at the BIC level, the Powering Interlock System has been tested today to correctly send and remove the USER_PERMITS for both, the maskable and unmaskabel channel.	All	N - Never	Done
Test of PLC and Matrix Configuration	20/05/2010	03/06/2010		Markus Zerlauth	Tests have been done using the automated bis-check program of Ivan. All checks where successful, with the exception fo super-locked circuits and some pre-condition checks (due to non-ready adjacent points).	All	S - After Shutdown	Done

Local intranet 85%

Fast Magnet Current Change Monitors + WIC

- **FMCM**
  - **No HW nor SW changes** foreseen for X-mas shut-down
  - No need for repetition of tests @ injection, would like to propose some **type tests (end-of fill) for 4TeV with at least one RD1, RMSD** -> If end-of-fill no dedicated time needed, otherwise 2 ramps

- **WIC**
  - **No HW changes** foreseen for X-mas shut-down
    - Tbc: Relocation WIC from US85 to UA83
  - **Interlock checks** (cabling, etc…) as part of HWC
  - **PVSS upgrade** with new CIBU tests interface
    - **WIC-BIC tests** with automated tools (1 hour)