LHC BLM changes During the Technical Stop 2010/11

B. Dehning

CERN BE/BI

Hardware Changes

- Dismounting and remounting of BLM equipment for the removing of the paint for 76 DN 200 valves in sector 2-3
- Visual inspection of chambers with serial number 1000 to 2000 search for cold soldering
- Installing of tow special NG 18 cable (shielded twisted pair) to improve noise behavior, Point 3, test with current source
- Exchanging of high voltage divider in signal boxes, Point 3
- Replacing of a backplane in the tunnel rack (test of new version), Point 3, test with current source
- Removing of a BLM on the MKI.2L, test with current source
- Installing of WorldFip cables in the arc racks all LHC (to be decided)

Soft and Firm-Ware Changes

- Combiner FPGA (BLECS):
  - Add a shift register to hold the last 16 energy receptions and send those to Logging
  - Modify the connectivity check function
    - threshold comparison should includes boundaries (>= in state of >) to stop the BLMCC_ to fail...sometimes
    - Increase the word size to completely match the size of RSUM9 to avoid overflow (appearing on the BLMCC_)
  - Add the "Stop HV" function. To minimize the offset increase when turning off crates (and avoid the need of a CFC_RESET afterwards)
  - Modification of the installed and spare cards: - Exchange of 2 resistors to allow increase of modulation voltage (decrease of R332 and R335) to get better measurements with SEM and LIC...
  - Check and probable exchange of SR3.L BLECS due to HV readings stuck: http://bdidev1/bdisoft/operational/issuetrack/viewIssue.php?issueNumber_rqd=1371
- Threshold comparator FPGA (BLETC)
  - Add filter information in the settings and applications
  - Enable the card serial and firmware version checks done in the FPGA to remove the beam permit
  - Change XPOC data delivery:
    - Send data directly to PM server
    - Remove the two subscriptions (one from XPOC server and one from Logging)
  - Produce and add in the Logging and PM separate Dump Request variable for those coming from statuses and those from measurements over threshold
  - Remove 1.3 s data (we still have some doubts because of complexity)
  - Add filter info
  - Re-test with more 40 us samples / monitor (currently 2048)
  - Sync ATLAS BLM version: ○ Integrate changes in XPOC and PM libraries

Tests

- Automatic on Vertical Slice Test system (before releasing new firmware)
  - Linearity, impulse, and some predefined patterns of input signals check
  - Inject predefined patterns in the XPOC and PM Buffers
  - And others …
- Exhaustive Threshold triggering tests (ring with installed system)
- Reception and Status tests (continuous, ring with installed system)
- Functional test tests with pilot beams
  - Global: injected pilot beams, de-bunched them and initiate dump
  - Threshold triggering: close one of the collimator jaws of a TCP at point 3 and injected 3 times pilot beam 1

Procedure for new firmware release

- A few hours of manual testing
  - Carry out simulation with test benches all parts affected
- Perform hardware-based test
  - CRC errors
  - CID errors
  - FID errors
  - Lost frames
- 24 hours of automatic testing
  - Execute the software-based “Exhaustive testing”
  - All tests need to pass!
- Inspection of the code changes by the verification engineer
  - Independent review