Upgrade of the LHCb Tracking system
Hardware requirements and technological status

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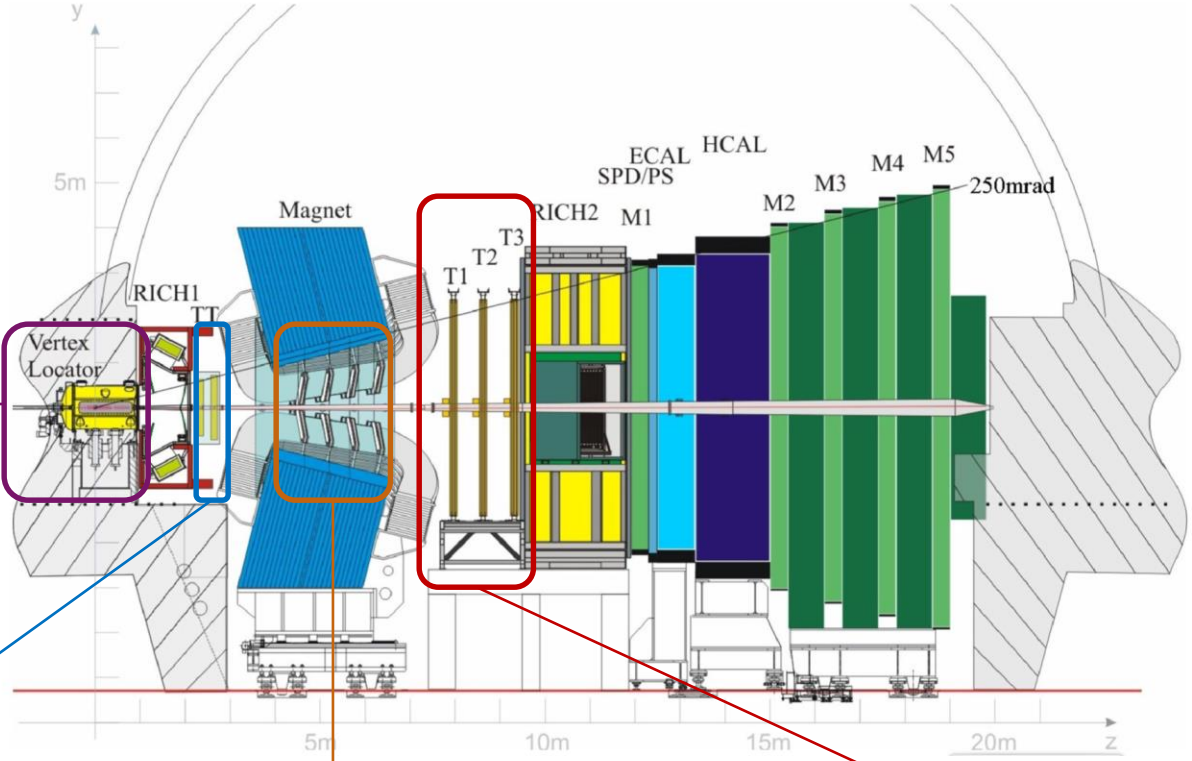
THE TRACKING SYSTEM UPGRADE



VELO
Pixel with timing

Upstream Tracker
From strip to CMOS

Magnet stations
Tracking on magnet sides

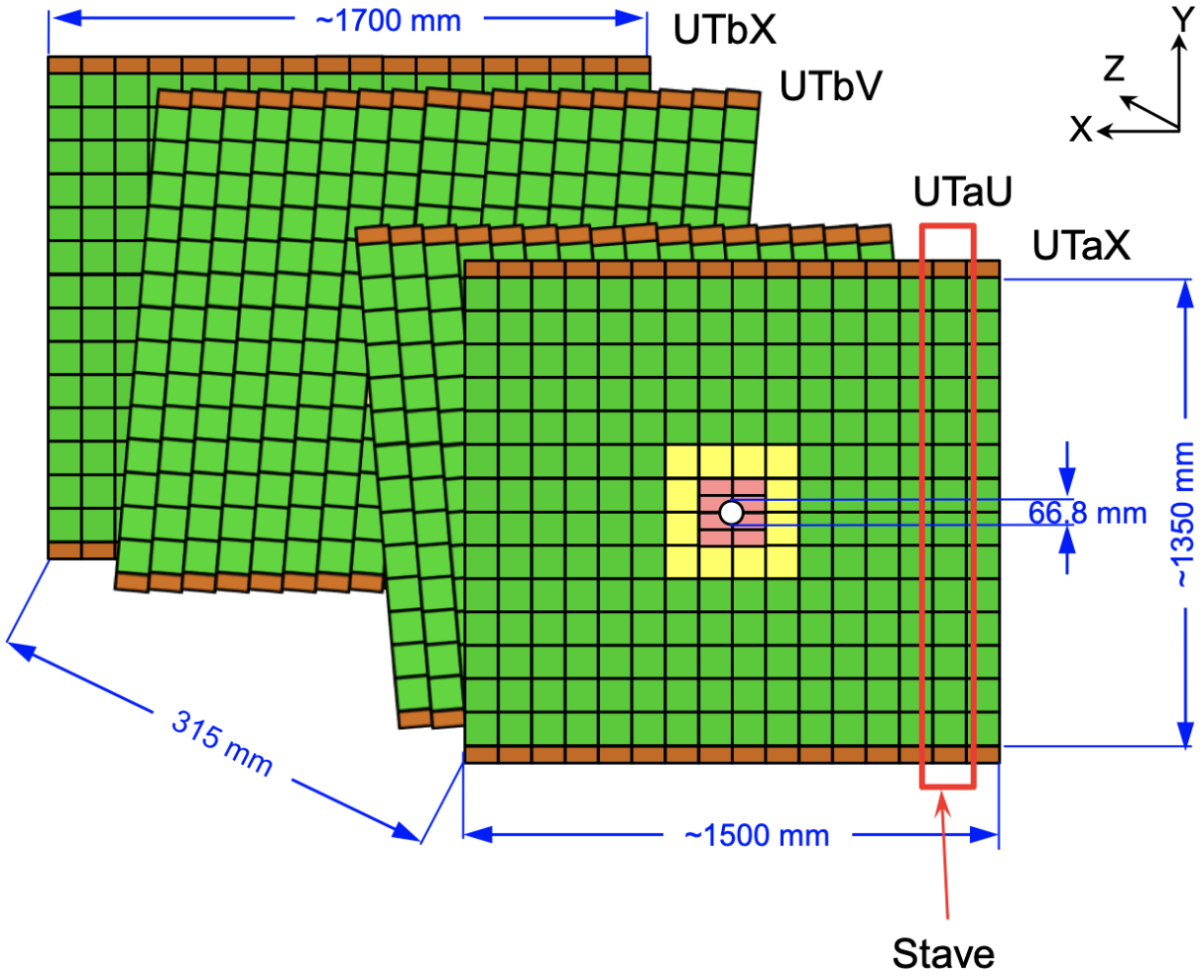
Mighty Tracker
Combine SciFi & CMOS

THE UT UPGRADE – FROM STRIPS…

Sensor	A	B	C	D
Type	p-in-n	n-in-p	n-in-p	n-in-p
Thickness(μm)	320	250	250	250
Pitch (μm)	187.5	93.5	93.5	93.5
Length (mm)	~100	~100	~50	~50
Strips/sensor	512	1024	1024	1024
SALTs/sensor	4	8	8	8
Numbers	888	48	16	16

- Four planes of silicon strip detectors, readout ASICs at sensor proximity.
- Higher segmentations near the center. Max occupancy ~ 1.4%.
- Stave structure: modules on 2 sides for overlapping, readout at 2 ends.
- In total 68 staves, 968 sensors, 4192 ASICs.

The present UT upgrade



The UT upgrade – From strips… to pixels

UT is key to connect VELO and MIT track segments

UT is essential for Upstream and Downstream tracks

Possibility of standalone UT track segment

- Will likely require three UT stations
- Could improve and speed-up track matching
- Could provide momentum estimation

Need of timing is being studied

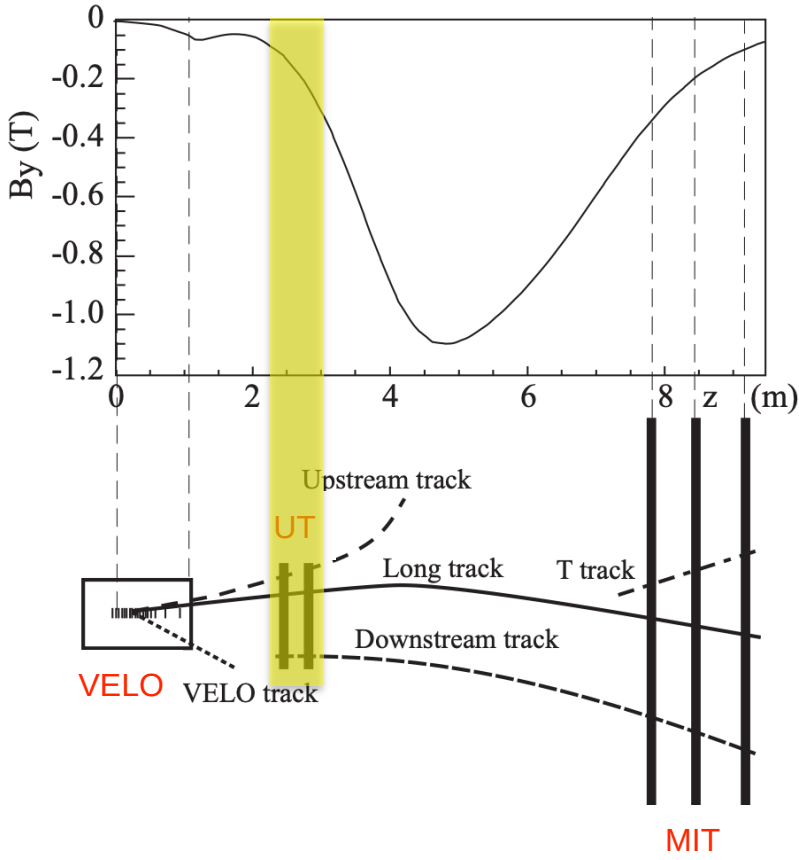
- Minimum requirement: BX identification, few ns time resolution
- Tracking: e.g. background rejection, sub-ns time resolution

Need to handle high-occupancy of most central Pb–Pb collisions

Solution: replace the Si strips with CMOS MAPS

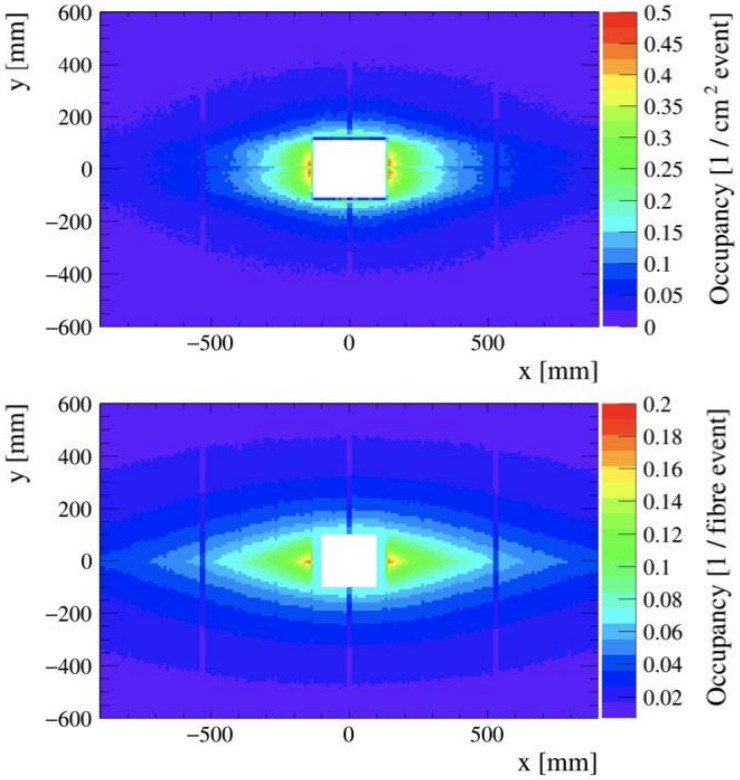
Large interest within the French HI community and beyond…

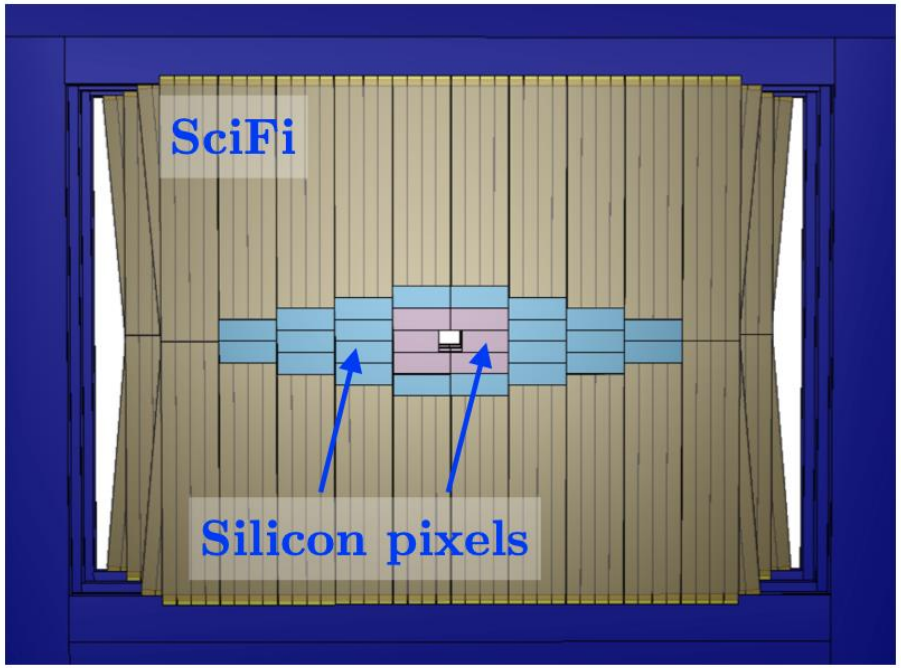
- LLR, LPNHE, Irfu, Subatech,…
- Several labs in China



The Mighty tracker

- $\int \mathscr{L} = 300\text{fb}^{-1}$ ⇒ significant fibre radiation damage in inner region
- $\mathscr{L}_{\text{inst}} = 1.5\times10^{34}\ \text{cm}^{-2}\ \text{s}^{-1}$
  ⇒ very high occupancy (up to 20%/fibre/event)
  ⇒ SciFi must be replaced near beam pipe to maintain the same (or better) tracking performance
- Solution: instrument the inner region with a pixel detector, while keeping scintillating fibres in the outer region





Inner + Middle + SciFi Tracker
=
Mighty Tracker

(Distinguish between Inner and Middle regions because LHCb is exploring the option to install Inner part for Run4)

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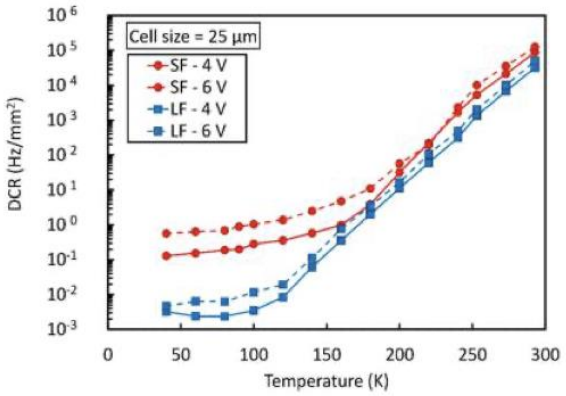
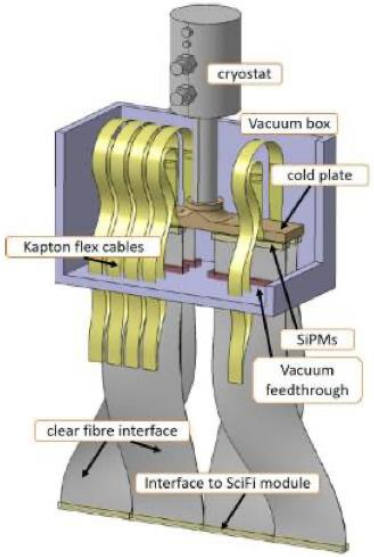
SciFi enhancement

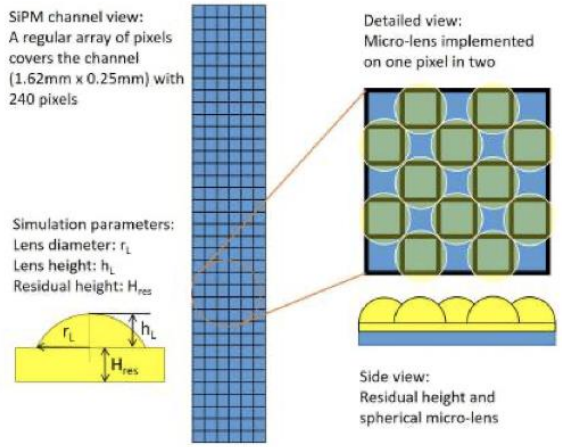
Major improvement seen cryogenic cooling to allow to run below -120 °C

- Essential to maintain reasonable noise rate for SiPMs after irradiation
- Should allow to reduce the cluster thresholds while keeping acceptable dark count rate





Additional interface
~ 16 % loss in light



Can gain back ~ 20 % by microlens.
Geometry packing of SiPMs also improved

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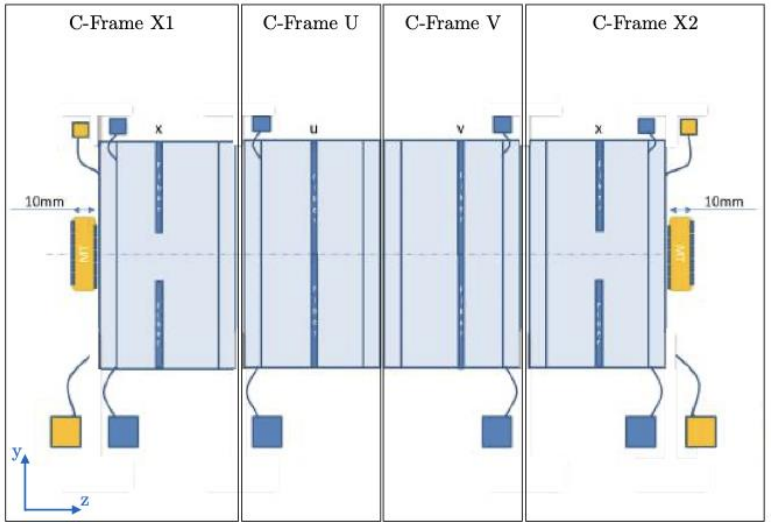
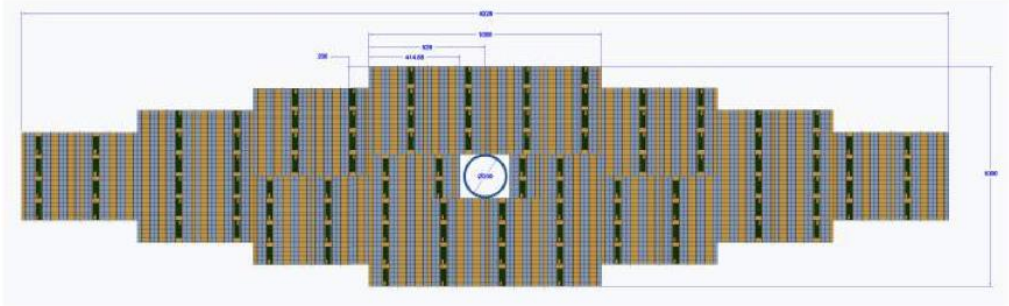
SciFi-CMOS integration

- SciFi layers and station layout similar to Upgrade 1 (modulo cryogenic cooling and mounting of layers on individual C-frames)
- Silicon layer panels (+ services) mounted on front and back of first/last x-layers in each station
- Panels integrated into Airex support box that provides thermal isolation (allowing operation below 0° C)



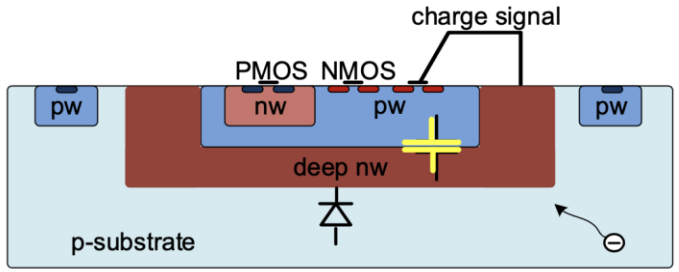


Services for Silicon run across Fiber acceptance
Care needed with material budget

Alex Bitadze, Trevor Savidge

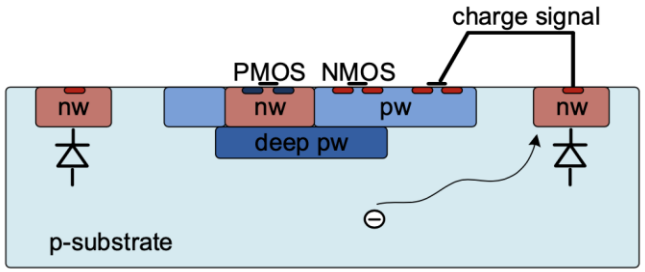
Fred Blanc

Two main CMOS options under consideration



Large collection electrode (baseline for the MT)

- Typical pixel size: 50 x 150 μm^2
- Circuitry inside the collection well (requires high field: HV-CMOS)
- High radiation hardness
- Higher noise (high capacitance)
- Higher power consumption
- Possible cross-talk (digital to sensor)
- Presently developed under AMS-180 (MuPix, ATLASPix) and LF-150 technologies (Monopix2)



Small collection electrode (baseline for the UT)

- Typical pixel size: 30 x 30 μm^2
- Circuitry outside the collection well (requires low/moderate field: LV-CMOS)
- High radiation hardness thanks to process modification (increase of depletion zone)
- Lower noise (low capacitance)
- Lower power consumption
- Less sensitive to cross-talk
- Presently developed under TJ-180 (Monopix2, MALTA2)

Main advantages

- Excellent space resolution
- Low budget
- Good radiation hardness
- High integration in monolithic technology

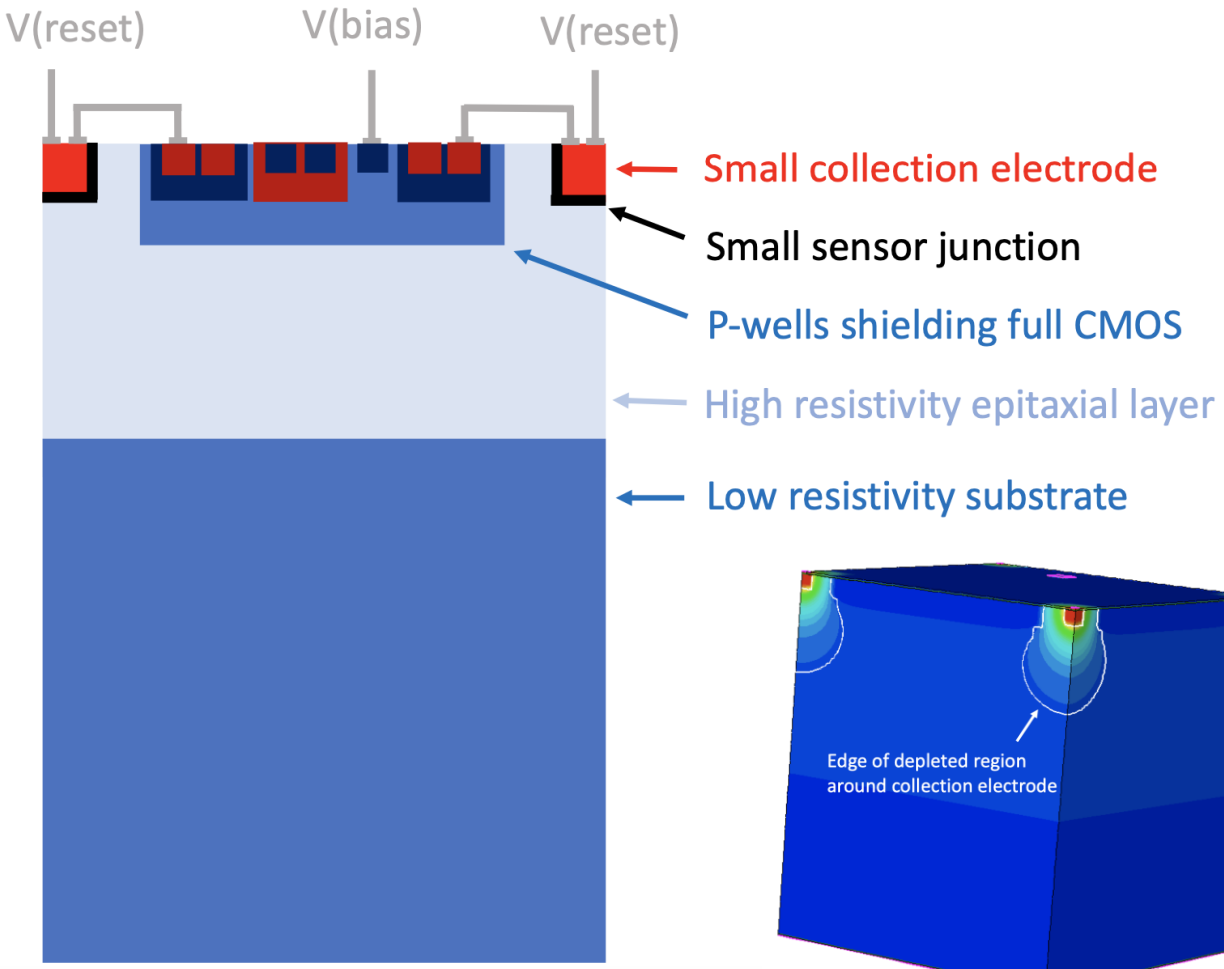
Main challenges

- Readout architecture for very high hit rate
- Provide high radiation tolerance
- Improve time resolution (eventually to sub-ns range)
- Keep low power consumption

Final choice on MAPS technology will be based on refined and consolidated detector specifications and R&D

THE TYPICAL CMOS PROCESS (TJ-180)

180nm standard imaging technology process



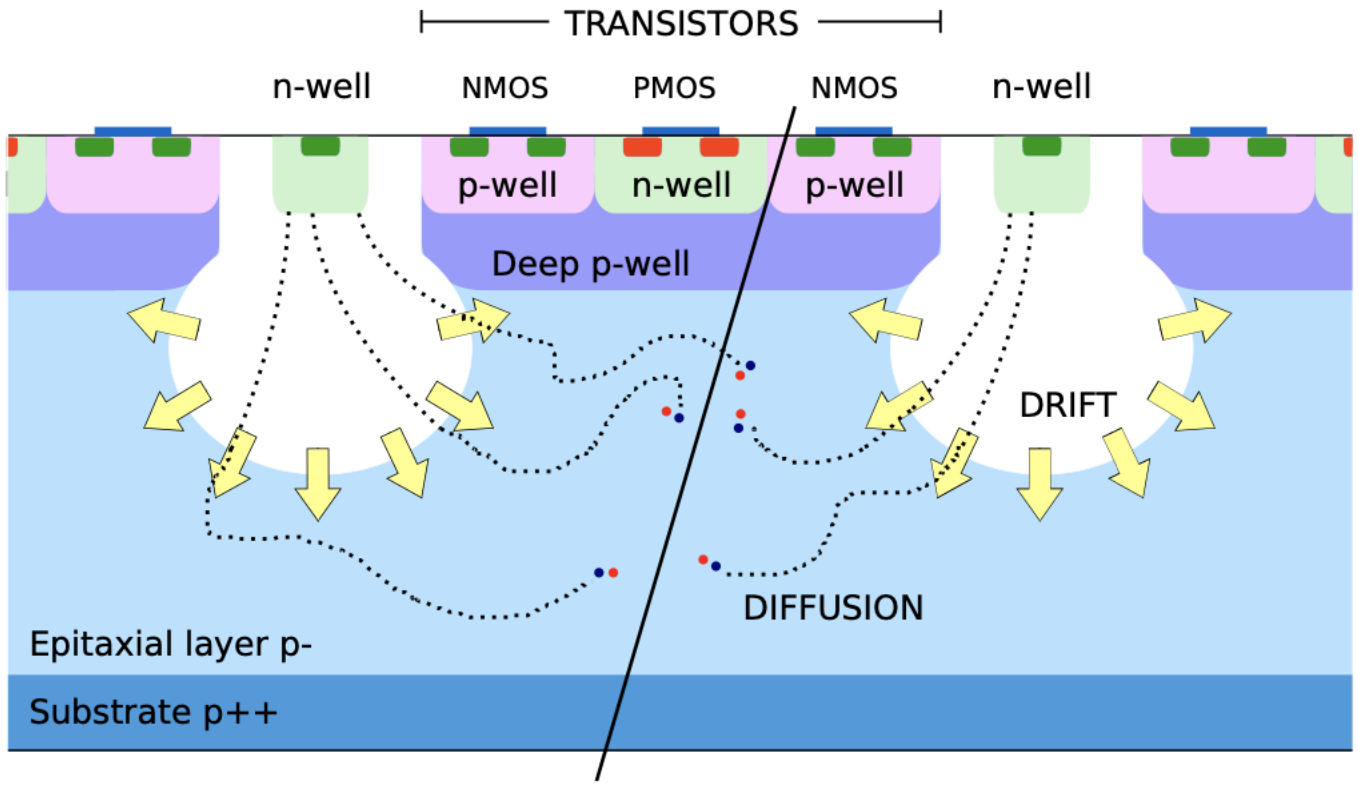
Not on scale

- Monolithic design with small capacitance
- P-well changes electric field and charge collection in active sensor volume
- Placement of full circuitry inside pixel matrix in well separated from collection electrode

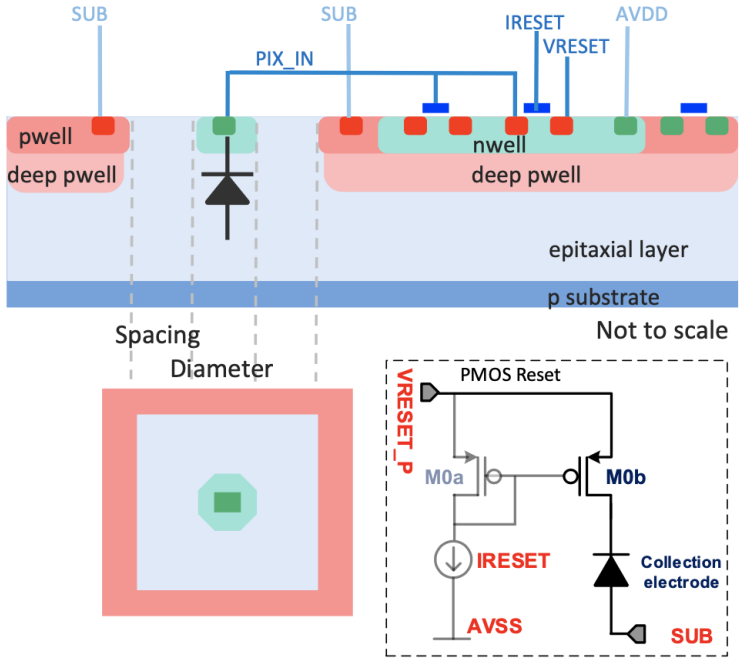
- Even with high resistivity epi-layers (few kΩ ·cm) and maximal sensor bias voltage, the depletion in the standard process is very limited

- **Limited depletion and small sensor junction**
  - Bias voltage limited by circuitry
  - Significant contribution from diffusion
  - Excellent position resolution
  - Reduced charge collection time: reduced radiation tolerance and time stamping capability
  - Reduced seed signal: reduced efficiency (even before irradiation)

THE ALPIDE EXAMPLE (TJ-180)



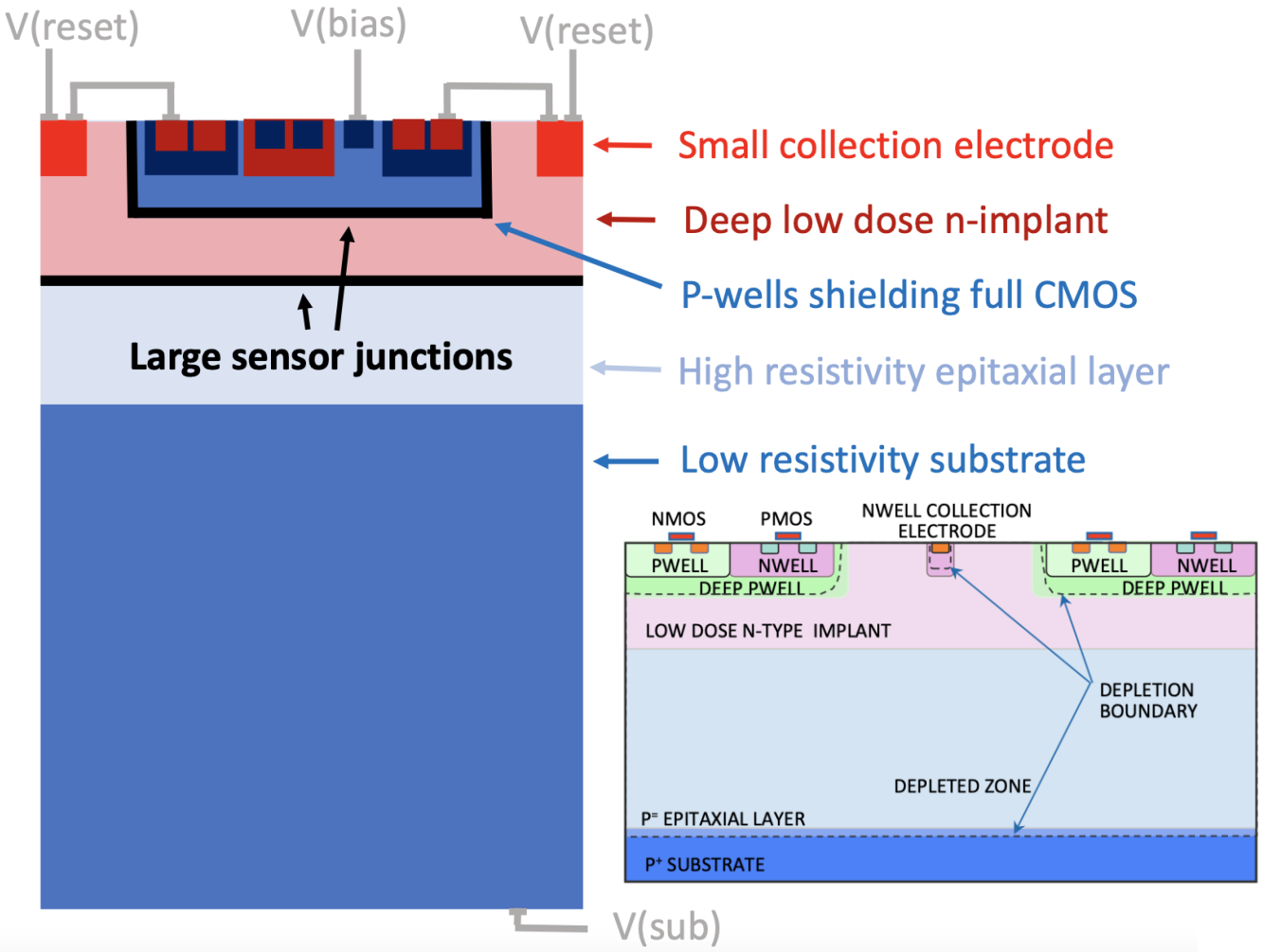
- High resistivity (> 1 kΩ ·cm) p-type epi-layer
- Bias voltage: 1.8 V
- Reserve bias (up to -6 V) for augmented (though not complete) depletion
- Small depletion depth (~ 30 μm) $d \sim \sqrt{\rho \cdot V}$



- Small collection electrode (~ 3 μm²)
- Small input capacitance (< 5 fF)
- High signal to noise ratio (~ 20)
- Charge collection time ~ 30 ns

THE MODIFIED CMOS PROCESS (TJ-180)

180nm modified imaging technology process:



Not on scale

- From MAPS to DMAPS

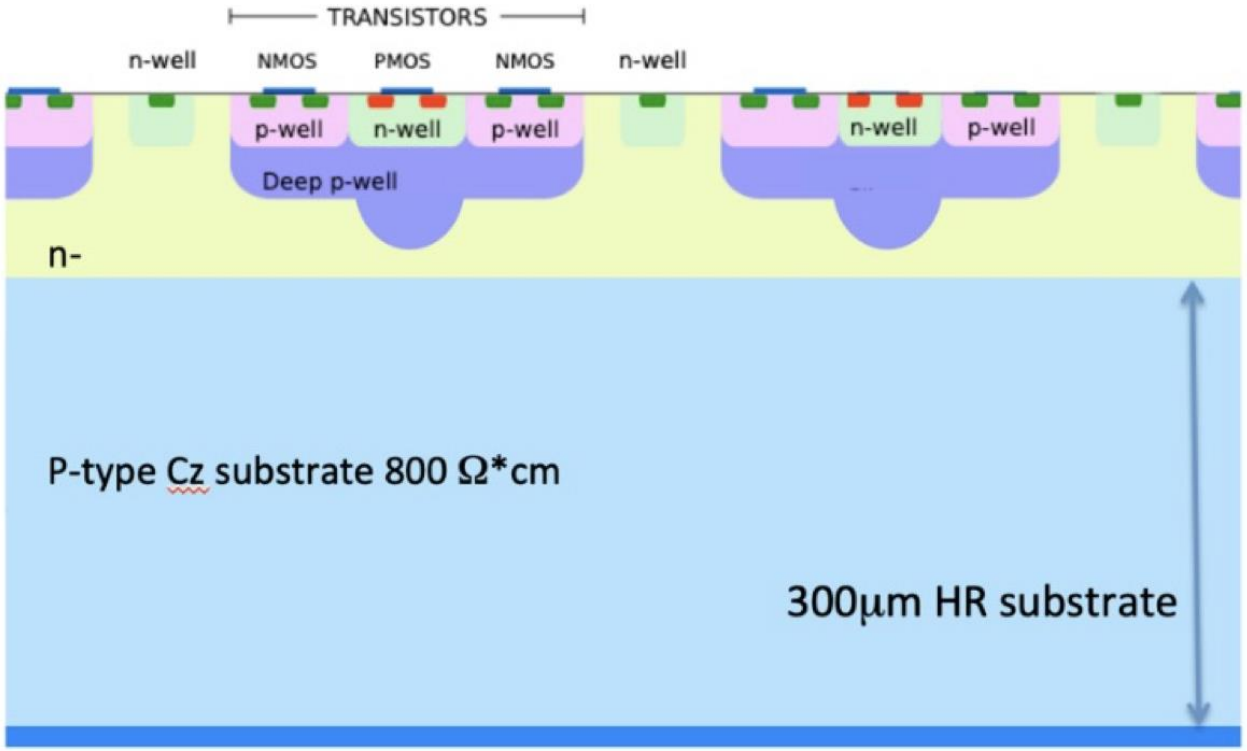
- Add large planar deep low/medium dose n-implant
- Large sensor junction
  - Full lateral depletion
- Maintain small capacitance
- No main modification to the circuitry and layout
- Isolation of P-wells and substrate
  - Substrate voltage non-limited by circuitry, higher sensor bias (tenth of volts)
- Better radiation tolerance

- Examples: TJ-MONOPIX and MALTA (for ATLAS)

What can we expect from TJ-65?

- Very active developments (CERN)
- Prototype run ongoing: results to come
- At first order: increase pitch/thickness and reduce power consumption for a given circuitry

THE TJ-CZOCHRALSKI PROCESS



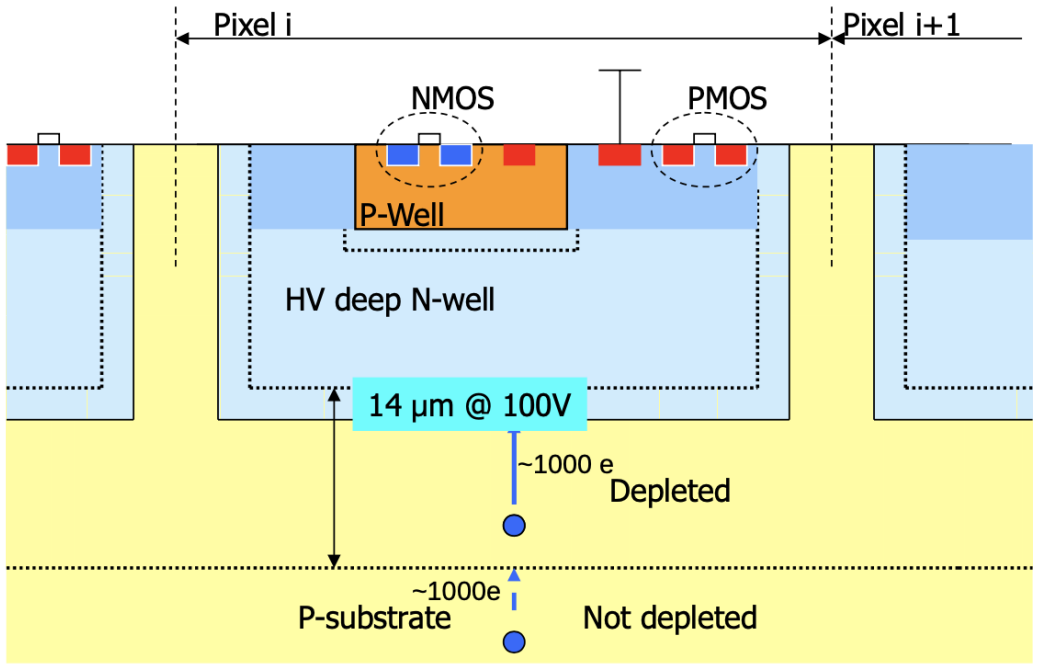
- From DMAPS to FDMAPS
  - From gas phase (epi) to liquid phase (Czochralski - Cz) epitaxial growth

- Increase the depletion layer thickness
  - Epi-layer thickness: 30 µm
  - Cz-layer thickness: 300 µm
- Keep high resistivity: 800 Ω·cm
- Can operate at 50 V reverse bias for full depletion
- Increase charge collection
- Maintain small capacitance
- No modification to the circuitry and layout
- Even better radiation tolerance and time resolution

- Tested on MALTA (MALTA-2)

Present focus of French labs

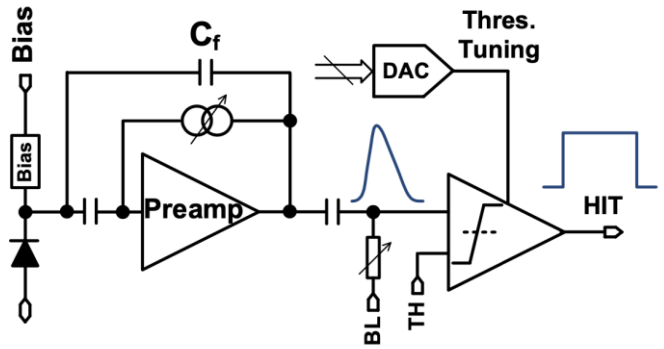
THE LARGE DIODE OPTION (AMS & L-FOUNDRY PROCESSES)



CMOS electronics placed inside the diode (inside the n-well)

Present focus of MT

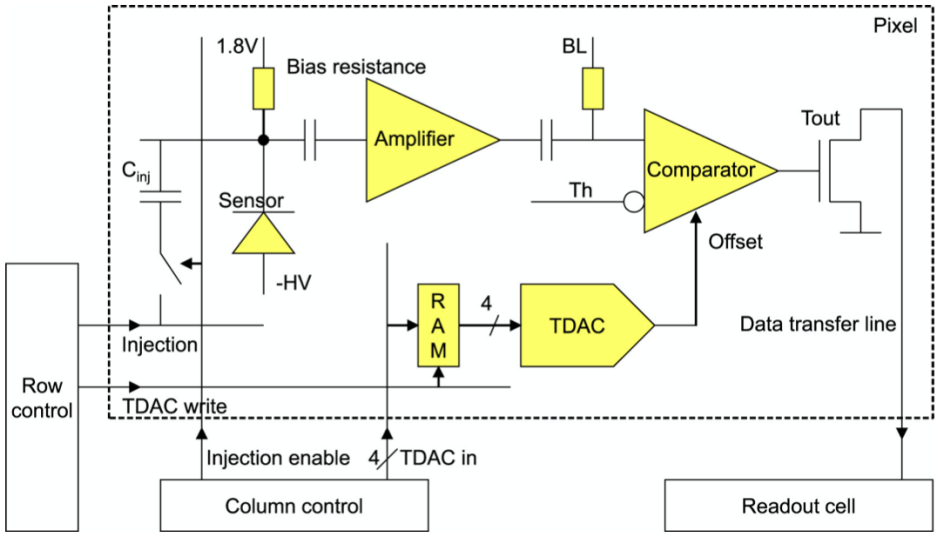
- Rather low-resistivity substrate (< 20 Ω·cm) and no epi-layer
  - Radiation induced N_{eff} almost insignificant
- Small thickness depletion zone (~ 10 µm)
  - Drift signal ~ 1000 e^-
- High breakdown voltage allows HV ~ 100 V
- Diode capacitance is rather high
- Circuitry requires rather high power consumption
  - Charge sensitive amplifier with gain independent on C_D

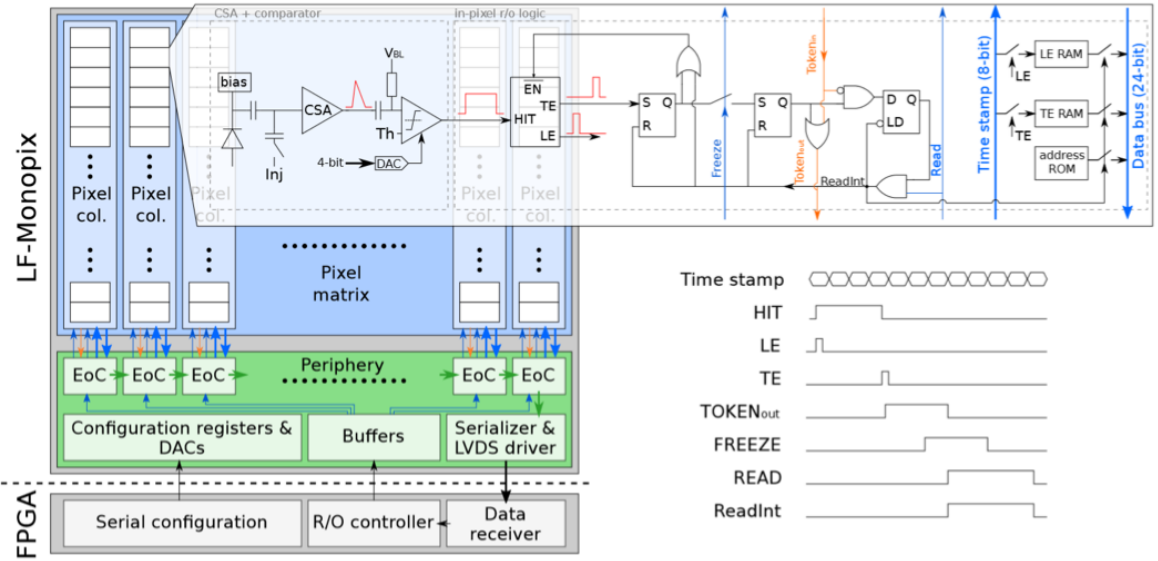


=> G ~ $1/C_f$ (typ. C_f ~ 5 fF)

$$\tau_{CSA} \propto \frac{C_D}{g_m \cdot C_f}\ ,\ ENC^2_{therm} \propto \frac{kT}{g_m}\frac{C_D^2}{\tau}$$

THE LARGE DIODE OPTION (AMS & L-FOUNDRY PROCESSES)

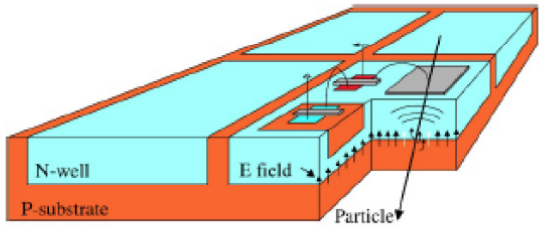




- First developed in AMS-350 technology (MuPix), then in AMS-180 (ATLASPix) with no digital circuitry in the matrix
  - Limit the power consumption
  - Readout scheme very complex and rate-limited (4-bit DAC for threshold adjustment): digital pulse brought to the periphery for ToT measurement
  - Large pixels (130 x 130 μm^2) with a matrix made of $N_{raw} = N_{col} = 400$

- Then in LF-150 (Monopix) with:
  - High resistivity (< 20 $\Omega \cdot$cm) substrate
  - Large pixels (50 x 250 μm^2) with a 129x36 matrix
  - CSA with 4-bit DAC for threshold adjustment (as for Mupix) plus in-pixel digital treatment (ToA and ToT)
  - Column drain architecture with 24-bit bus
  - Very large static current required for the circuitry (avoided during the readout phase)

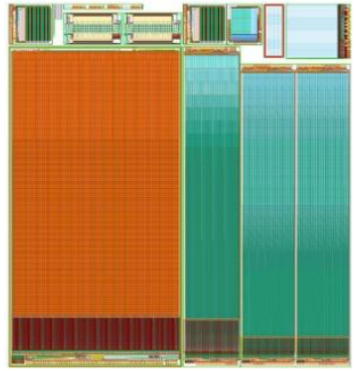
The MightyPix



- Monolithic Active Pixel Sensor (MAPS)
- Integrated pixel sensor & chip

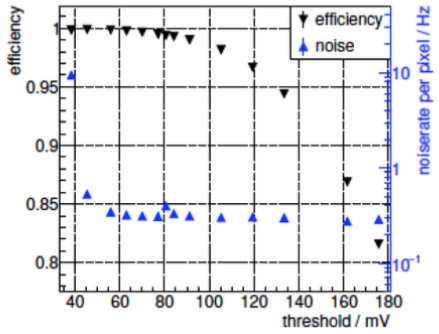
on **single** piece of silicon

  - Low-cost commercial process
  - e.g. used for mobile phone cameras
- First radiation hard CMOS tracker at LHC



- Chip based on existing MuPix/ATLASPix
- https://arxiv.org/abs/2002.07253
  - "MightyPix" Specification document in preparation

Parameter	Depleted CMOS Sensors for LHCb
Chip Size	$\sim 2\,\text{cm} \times 2\,\text{cm}$
Sensor Thickness (µm)	200 (ATLASPix3)
Pixel Size (µm)	100×300 (with smaller sizes to be explored)
Time Resolution (ns)	Must be within 25 ns window
Inactive area	$< 5\%$
Power Consumption (W/cm^2)	0.15
Data transmission (Gbps)	4 links of 1.28 Gb/s each, multiplexed to 2 and 1 links
NIEL (TBC)	3×10^{14} (6×10^{14} with safety factor)



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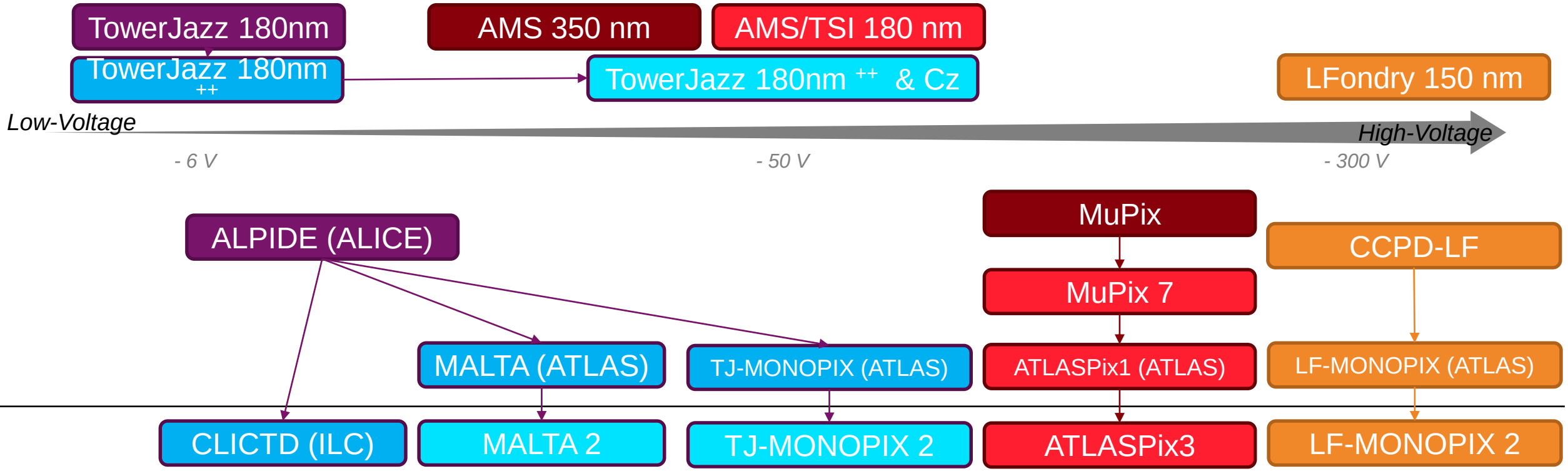
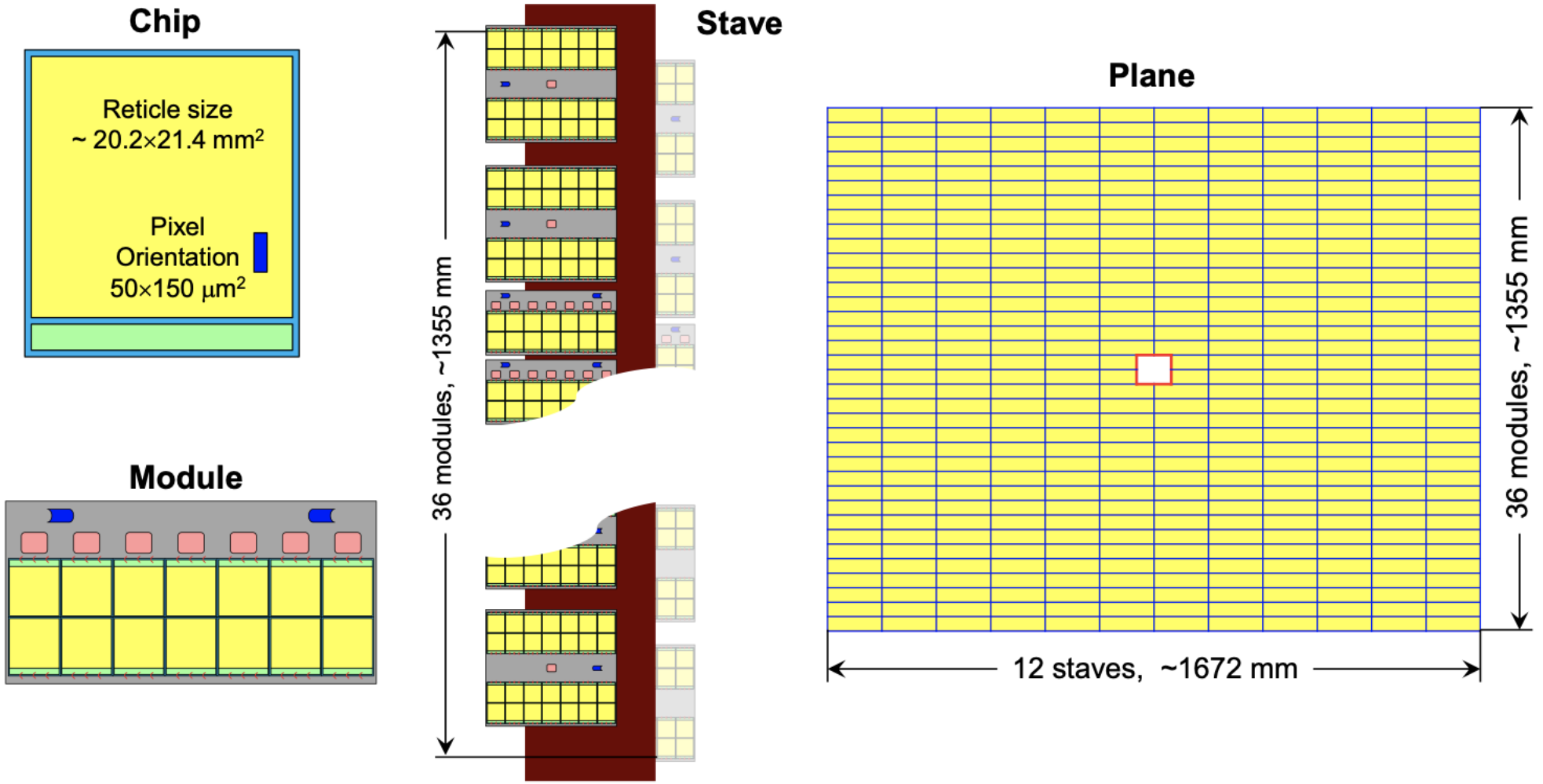
SUMMARY OF CMOS TECHNOLOGIES



Reverse Bias	- 6 V	- 50 V	- 50 V	- 80 V	- 300 V
Pixel size	300 x 30 µm^2	36.4 x 36.4 µm^2	33.04 x 33.04 µm^2	50 x 150 µm^2	50 x 150 µm^2
Time resolution	6 ns RMS	2 ns RMS	4 ns (3σ)	6 ns RMS	2 ns RMS
Threshold (noise)	200e- (14e-)	400e- (10e-)	200e- (10e-)	1640e- (160e-)	1500e- (150e-)
Power	410 mW/cm^2	80 mW/cm^2	170 mW/cm^2	225 mW/cm^2	300 mW/cm^2
TID (noise)	??	100 Mrad (30 e-)	?? (idem MALTA)	> 50 Mrad	> 100 Mrad
Efficiency (@ 2•10^{15} n_{eq}/cm^2)	99.9% (95.4%)	99.9% (95.1 %)	(98.6%)	99.9% (98%)	99.7% (98.9%)

A possible setup, very preliminary

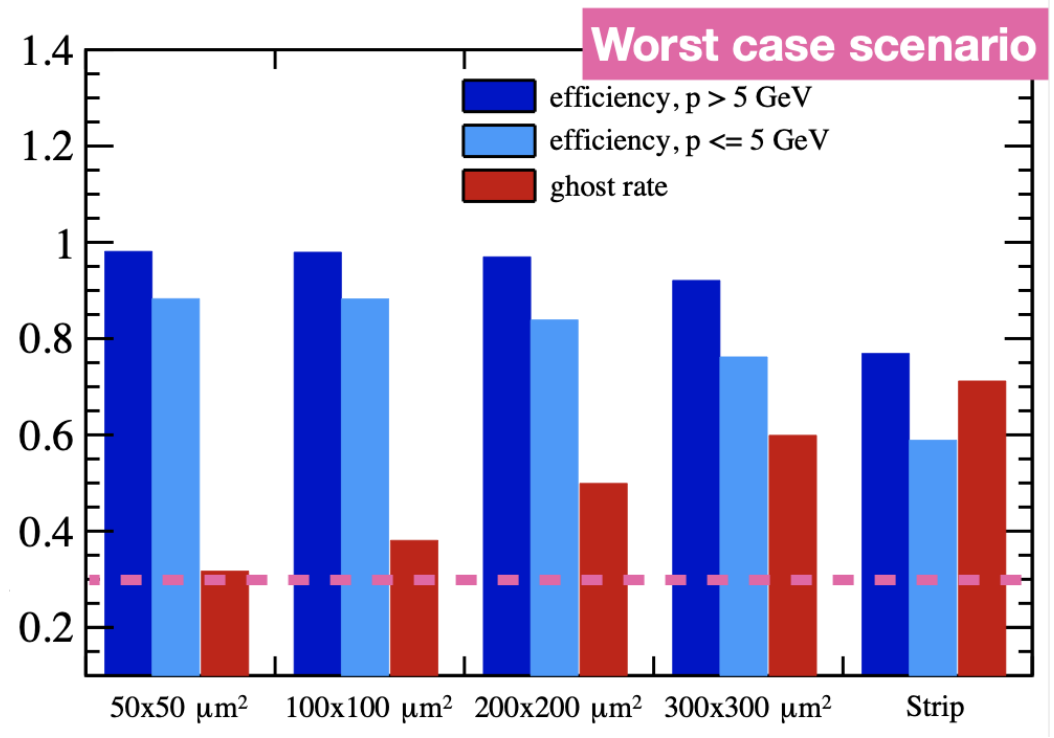


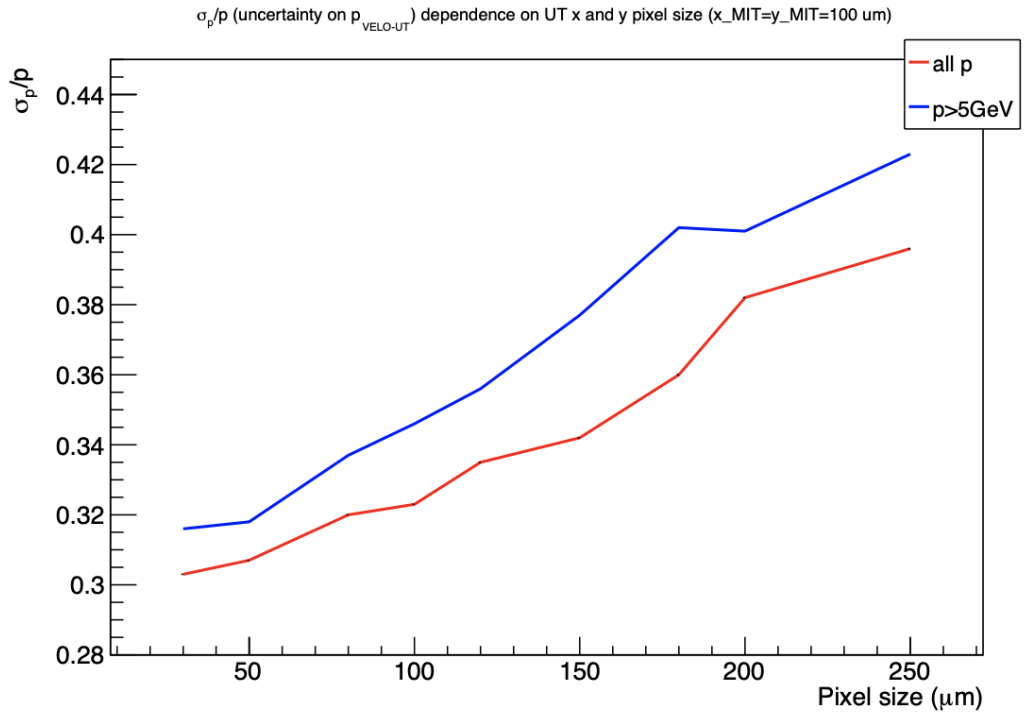
DETECTOR REQUIREMENTS

Characteristics	LV-CMOS	HV-CMOS
Chip size	3.5×3.5 cm^2	2.0×2.0 cm^2
Pixel size	30×30 μm^2	50×150 μm^2
Chip thickness	100 μm	
Position resolution	5–10 μm	15, 40 μm
Time resolution	O(1 ns)	
Power consumption	100–300 mW/cm^2	
Data rate per chip	Up to 30 Gb/s	Up to 9 Gb/s
Radiation dose	3×10^{15} n_{eq}/cm^2, and 240 Mrad TID	

A lot of requirements to be consolidated

- **Pixel size**
  - Occupancy
  - Space (→ momentum) resolution
  - Tracking performances (ghost rate)





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- **Pixel size**
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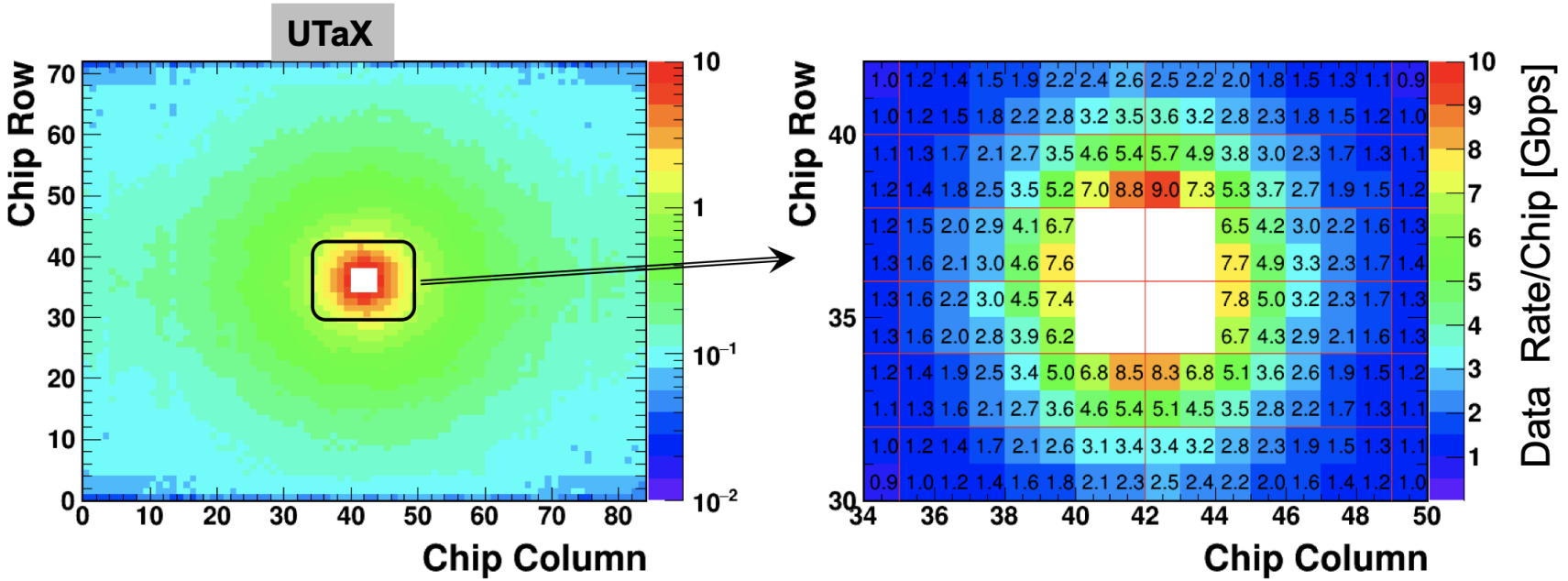
- **Chip size, detector position, number of planes**
  - Dead areas (keep below 1%) → efficiency
  - Tracking performances
  - Data rate (also depending on the readout scheme)



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- **Chip thickness and global material budget**
  - Space (→ momentum) resolution, multiple scattering
  - High impact on flex PCB conductor choice (Cu vs Al) and cooling solution (water can carbon composite)
  - Do we need to keep X/X_0 below 1% ? What is the maximum X/X_0 we can accept?

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  - Do we need to keep X/X_0 below 1% ? What is the maximum X/X_0 we can accept?
- **Time resolution (the most challenging development…)**
  - BX tagging (ns resolution) seems reasonably achievable
  - We need a detailed assessment of tracking performances to justify the need of a sub-ns resolution

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  - Space (→ momentum) resolution, multiple scattering
  - High impact on flex PCB conductor choice (Cu vs Al) and cooling solution (water can carbon composite)
  - Do we need to keep X/X_0 below 1% ? What is the maximum X/X_0 we can accept?
- **Time resolution (the most challenging development…)**
  - BX tagging (ns resolution) seems reasonably achievable
  - We need a detailed assessment of tracking performances to justify the need of a sub-ns resolution
- **Power consumption**
  - Demanding performances (fast readout, time resolution) comes with high power consumption
  - Baseline is to stay below 500 mW/cm^2 in order to be compatible with water cooling

Detector requirements

Characteristics	LV-CMOS	HV-CMOS
Chip size	3.5×3.5 cm^2	2.0×2.0 cm^2
Pixel size	30×30 μm^2	50×150 μm^2
Chip thickness	100 μm	
Position resolution	5–10 μm	15, 40 μm
Time resolution	O(1 ns)	
Power consumption	100–300 mW/cm^2	
Data rate per chip	Up to 30 Gb/s	Up to 9 Gb/s
Radiation dose	3×10^{15} n_{eq}/cm^2, and 240 Mrad TID	

A lot of requirements to be consolidated

- **Pixel size**
  - Occupancy
  - Space (→ momentum) resolution
  - Tracking performances (ghost rate)
- **Chip size, detector position, number of planes**
  - Dead areas (keep below 1%) → efficiency
  - Tracking performances
  - Data rate (also depending on the readout scheme)

- **Chip thickness and global material budget**
  - Space (→ momentum) resolution, multiple scattering
  - High impact on flex PCB conductor choice (Cu vs Al) and cooling solution (water can carbon composite)
  - Do we need to keep X/X_0 below 1% ? What is the maximum X/X_0 we can accept?
- **Time resolution (the most challenging development…)**
  - BX tagging (ns resolution) seems reasonably achievable
  - We need a detailed assessment of tracking performances to justify the need of a sub-ns resolution
- **Power consumption**
  - Demanding performances (fast readout, time resolution) comes with high power consumption
  - Baseline is to stay below 500 mW/cm^2 in order to be compatible with water cooling
- **Radiation hardness**
  - Detailed calculation is needed: present value is only a “rule of thumb” estimation

THE CHALLENGE OF THE RADIATION HARDNESS

- **Effect on the active sensor:**
  - Mostly due to charge carriers generated by ionization in the dielectric layer of the process, in particular oxide structures (gates, shallow trench insulators, spacers,…)
  - Charge trapping induces threshold shift
  - Need high depletion and drift field to collect the signal charge fast enough (before it gets trapped)
  - Need thin layers to contain power consumption from leakage currents (and appropriate reset circuit)
  - Modulated by bias and temperature: increase bias/temperature leads to damage increase (but not for annealing after irradiation)
- **Total ionizing dose**
  - Intrinsic transistor has become more and more radiation tolerant due to thinner gate oxide
  - Integrate enclosed transistors and guard rings to avoid leakage currents
- **Single event effects**
  - Single Event Upset (SEU): triple redundancy with majority voting (can be an issue also in the frontend FPGAs)
  - Latch-up: not observed at LHC (only in STAR)

Conclusions

- HL-LHC conditions require a major upgrade of all LHCb trackers
- Very important effort in prospecting solutions which use innovative techniques
- Preliminary studies (physics cases, tracking performances, technological solutions) have been made and integrated within the Framework-TDR but…
- Convergence between UT and MT on a technological choice would be highly beneficial (and is strongly suggested by the LHCC)
  - The time scale of the MT project is an additional constraint
- Simulations and performance studies are still needed to drive the technological choices (both for UT and MT)
- The R&D program started and is gaining momentum
- We have 3-4 years to complete this R&D and reach a readiness state compatible with a TDR