BCM for LHC

Beam Current Change Monitor

Collaboration:
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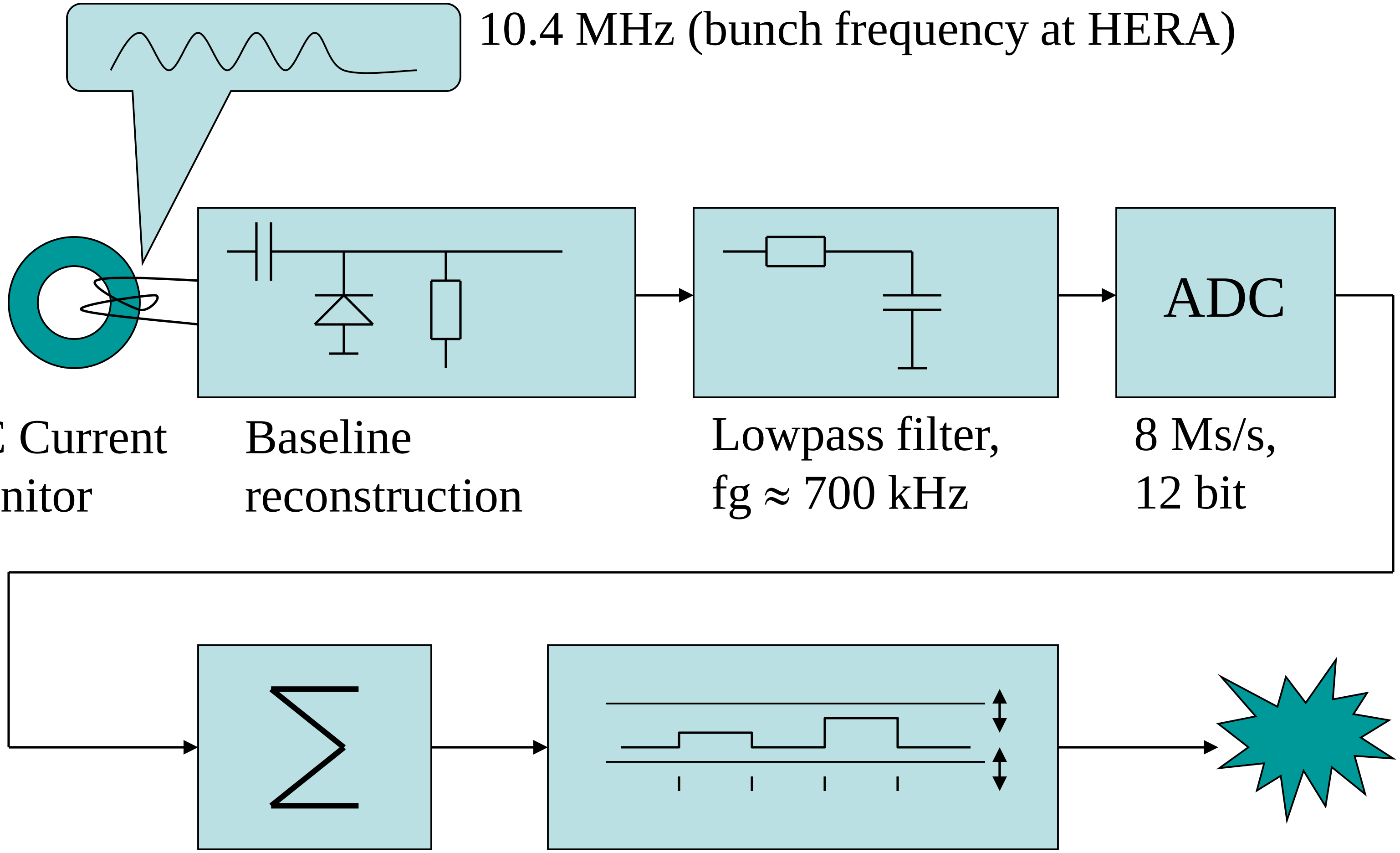
Presentation of Matthias Werner, 1 July 2010
With comments and corrections added

Purpose of BCM

- Fast detection of beam current drop, → beam dump
- Additional protection for LHC against fast beam losses
- Protection complementary to Beam Loss Monitors
- For unforeseen cases where Beam Loss Monitors might not work as expected
- Only backup protection → high reliability not so critical

Old HERA experience:
Fast ACCT beam loss alarm



10.4 MHz (bunch frequency at HERA)

AC Current monitor

Baseline reconstruction

Lowpass filter, fg ≈ 700 kHz

ADC

8 Ms/s, 12 bit

Sum over each turn; 1 turn = 21.12 us

Compare with tracking threshold

Dump Beam

CERN BCT Hardware

See papers / posters of D. Belohrad:

- 4 channels: High/Low gain, High/Low Bandwidth
- Interleaved Integrators
- 14-bit-ADC
- Baseline reconstruction at dump gap
- Mezzanine card for DAB card

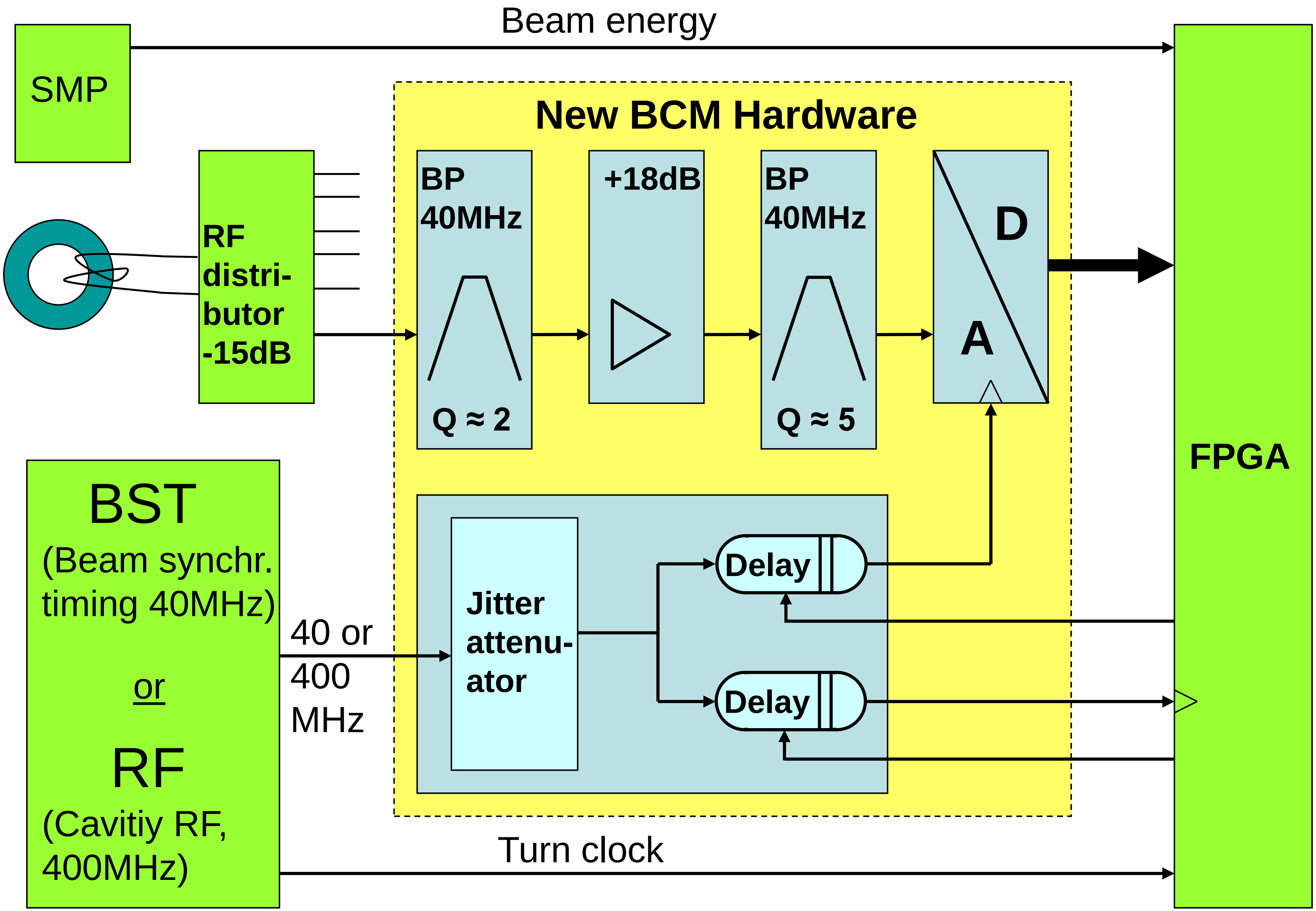
Use existing hardware or design new one?

single bunch measurement and a precise absolute measurement not necessary → concept can be changed with the following advantages:

- Independent of offsets in signal path
- Independent of toroid low cutoff frequency
- Simple and uncritical calibration once at commissioning
- Inherent baseline suppression
- High noise suppression also for frequencies < 100kHz (interesting because of power converter noise)
- Can be configured to work independent of parameters (e.g. thresholds) set by Control software (with fixed thresholds or thresholds derived from SMP = Safe Machine Parameters)
- High resolution

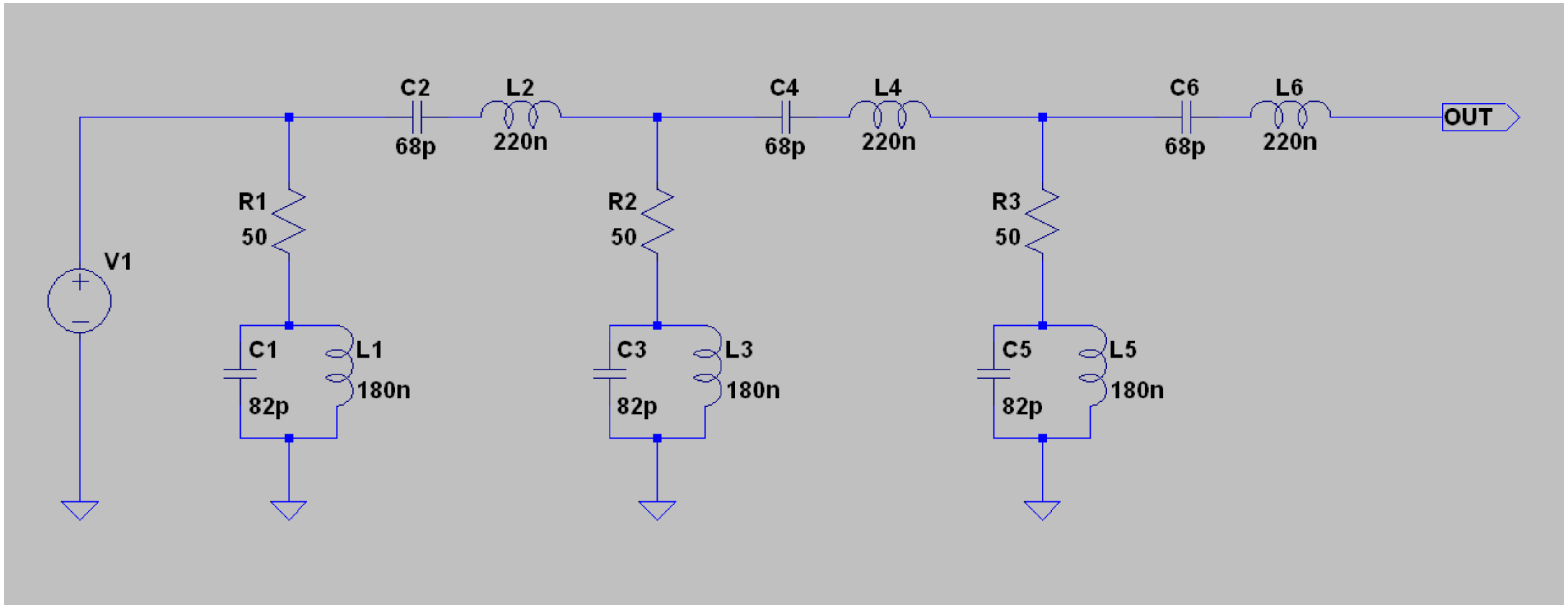
→ Easier to get high dynamic range and high resolution → proposal for new design!

New BCM hardware concept



Structure of the 40MHz bandpass filter (first stage with Q ≈ 2)

Zi ≈ 50Ω for „all“ frequencies



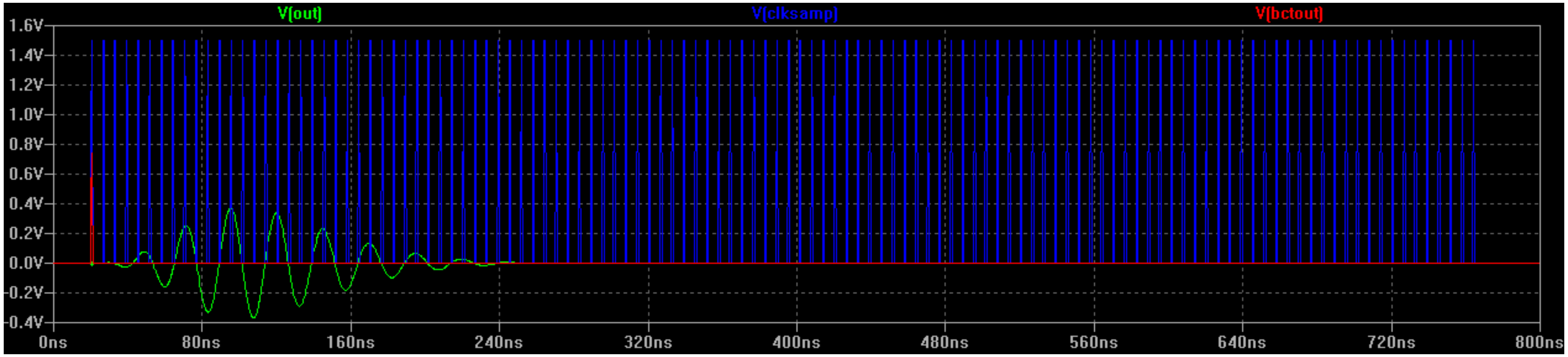
Signal simulations (1)

Red: raw signal from BCT

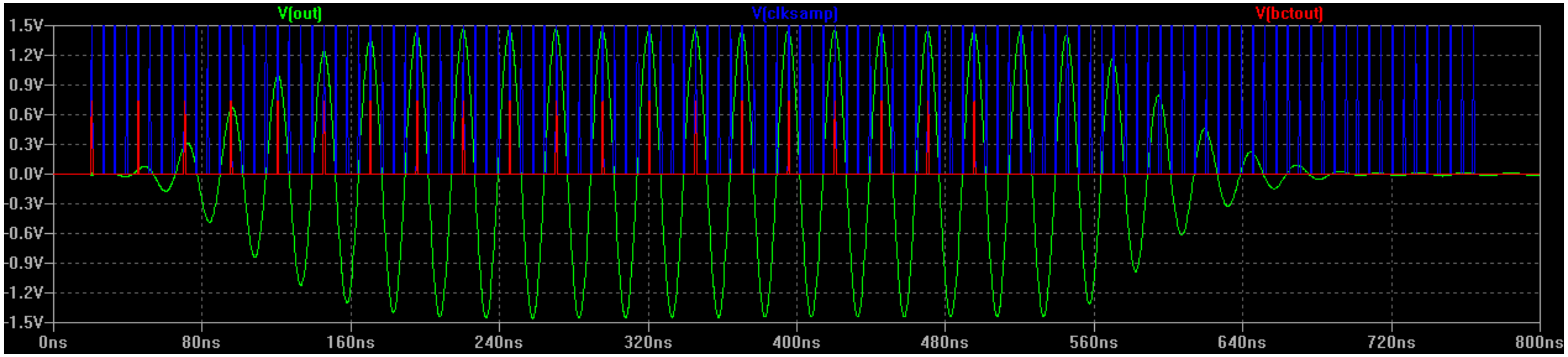
Blue: Sampling Clock 160MHz

Green: output of 40MHz filter

1 bunch

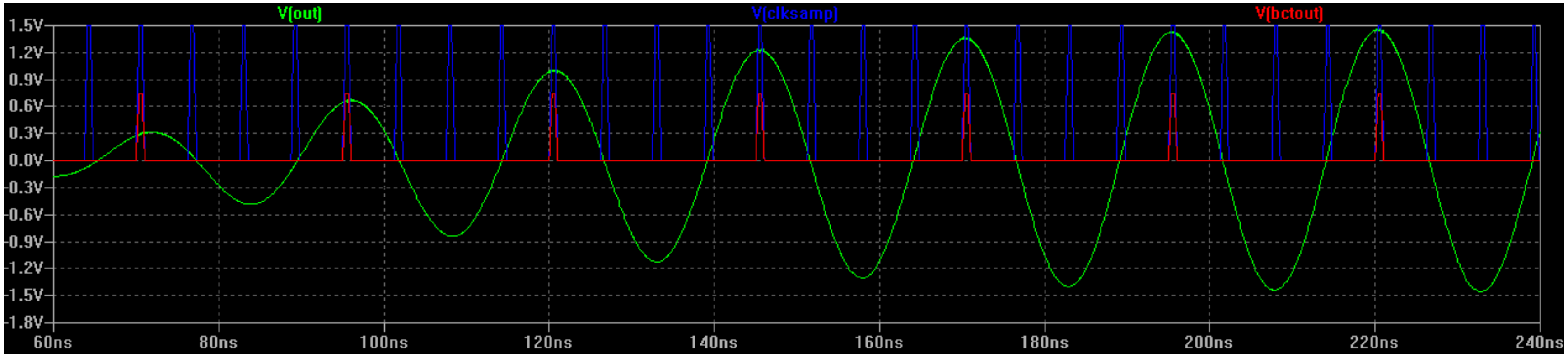


20 bunches

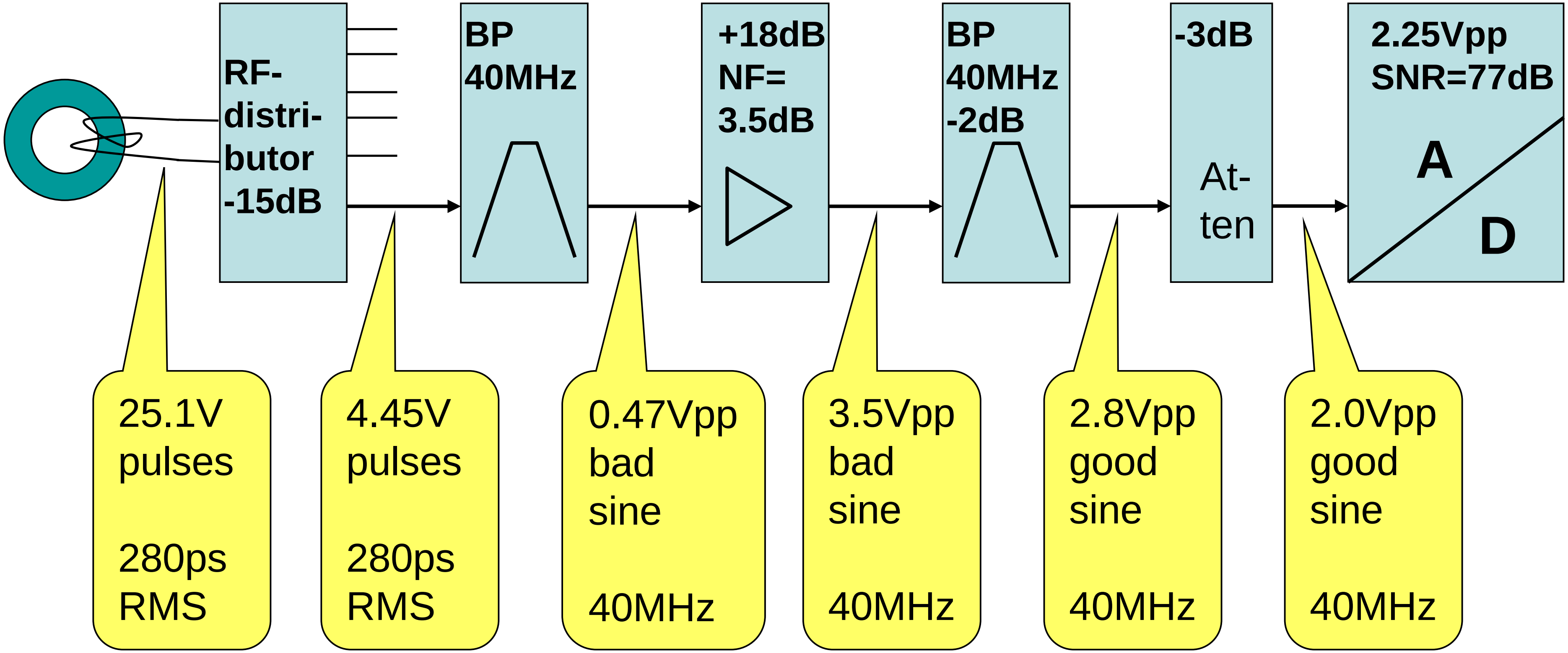


Signal simulations (2)

Detail from “20 bunches”



Dynamic range and noise (1)



RF-distri-butor -15dB

BP 40MHz

+18dB NF= 3.5dB

BP 40MHz -2dB

-3dB

At-ten

2.25Vpp SNR=77dB

A D

25.1V pulses

280ps RMS

4.45V pulses

280ps RMS

0.47Vpp bad sine

40MHz

3.5Vpp bad sine

40MHz

2.8Vpp good sine

40MHz

2.0Vpp good sine

40MHz

Amp. Input referred:
Terminated 50R noise
+3.5dB→0.67nV/√Hz,
0.47Vpp

ADC: 2.25Vpp, SNR=77dB
→noise=112uV RMS
With BW=80MHz:
12.5nV/√Hz

Theoretical min. dump threshold
(1 bunch = 1.7*10^11 p)

Worst case SNR of ADC at 40MHz:
75.6dB @ -1dBFS → 17 000 : 1

Average over 2808 bunches:
Degrade / $\sqrt{(2808+7)}$ = 53

Average over 1 bunch:
Degrade / $\sqrt{(1+7)}$ = 2.83

(+7 because of 40MHz-filter ringing)

Subtraction Top – Bottom:
Degrade / 1.41

Alarm threshold 10 sigma
(→Spurious Dump Probability
= 1.6*10^-23 per „alarm input value"):
Degrade / 10

For 2808 bunches:

Average 1 Turn:
22.7 : 1
→ $7.49*10^9$ p

Average 1 ms = 11 turns:
75.2 : 1
→ $2.26*10^9$ p

Average 10 ms = 112 turns:
240 : 1
→ $7.08*10^8$ p

Average over 1024 turns:
726 : 1
→ $2.34*10^8$ p

“Dynamic range” (ADC + statistics)

Full scale voltage (peak-peak) / noise (RMS):

Worst case SNR of ADC at 40MHz: 75.6dB @ -1dBFS	17 000
Average over 2808 bunches	* 53
Subtraction Top – Bottom	/ 1.41
Alarm threshold 10 sigma	/ 10
Result	**63 900**

Corrections / Options:

ADC SNR is typical (76.8dB), not Worst case (75.6dB)	* 1.15
Averaging over 4 parallel ADCs	* 2
non-optimum ADC design	/ 1.5
Unforeseen effects, insufficient shielding	/ 2
Averaging over multiple turns	√(turns)

Table: Theoretical Resolution

Averaging over	**RMS resolution**		**Dump threshold**	
	2808 bunches filled → $4.8*10^{14}$ p	1 bunch filled →$1.7*10^{11}$ p	2808 bunches filled → $4.8*10^{14}$ p	1 bunch filled →$1.7*10^{11}$ p
1 turn	$7.5*10^{8}$	$4.0*10^{7}$	$7.5*10^{9}$	$4.0*10^{8}$
1 ms	$2.3*10^{8}$	$1.2*10^{7}$	**$2.3*10^{9}$**	$1.2*10^{8}$
10 ms	$7.1*10^{7}$	$3.8*10^{6}$	$7.1*10^{8}$	$3.8*10^{7}$
1024 turns	$2.3*10^{7}$	$1.3*10^{6}$	$2.3*10^{8}$	$1.3*10^{7}$

Practical resolution

Effects which could degrade resolution:

- ADC nonlinearity
- EMI from power converters and other sources, affecting the BCT toroid → tests with no beam
- Position dependence of BCT → test with local bump
- Magnetic effects in toroid (no effects expected by experts)
- Timing jitter (improve by using directly 400 MHz RF?)
- What else?

What resolution do we really get?
→ First go for 0.1% in 1 ms!

Protection levels

Protection level (full beam) **for reaction time = 1 ms**	Number of particles	Part of full beam (4.8*10^14p)
Useful *	$4.8*10^{12}$	10^{-2}
(old Hera system)		10^{-2}
good	$4.8*10^{11}$	10^{-3}
First performance goal of BCM	$4.8*10^{11}$	10^{-3}
damage level (7TeV) *	$1\text{-}2*10^{10}$	$3\text{-}6*10^{-5}$
Theoretical performance limit of BCM (with 1 ADC)	$2.3*10^{9}$	$4.8*10^{-6}$
Full protection (7TeV) *	$1*10^{9}$	$2*10^{-6}$

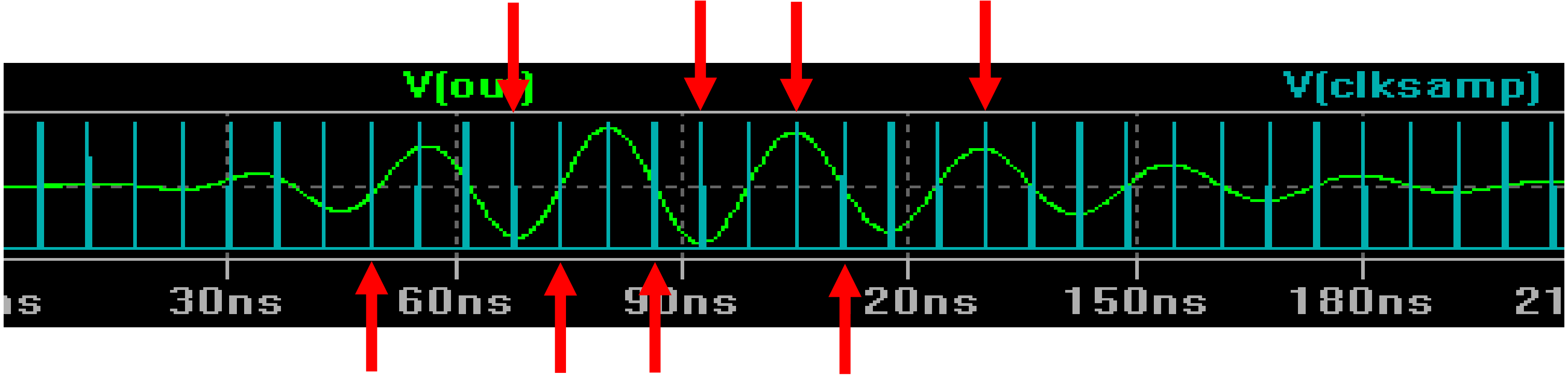
* R. Schmidt: LHC REQUIREMENTS TO MEASURE FAST CURRENT DROPS (CARE Lifetime Workshop 2004)

Signal Processing Algorithms, FPGA Firmware

- 40MHz digital filter
- Phase tracking loop
  - Initialize Si5326 chip
  - Calculate delays (initialize at injection, then track)
  - communicate delays to Si5326 chip
- Threshold tracking (fast up, slowly down)
- 2 (or 6?) Averaging stages (sliding windows!) over 1 to 1024 turns
- “Bucket mask”: only average buckets which contain beam
  - Adapt mask (only at injections? Algorithm?)
  - Apply mask
- Interlock generation
- Peak beam change detector for commissioning
- Optional: compare turn subdivisions (if single bunch losses are possible)
- Receive SMP signals to set thresholds depending on beam energy

40 MHz digital filter algorithm

4 Samples per 40 MHz period (= 160 Ms/s):



Bottom samples

Top samples

Zero rise samples

Zero fall samples

$$BeamCurrent = \sum_{one\_turn} top\_samples - bottom\_samples$$

$$PhaseError = \sum_{one\_turn} zero\_rise\_samples - zero\_fall\_samples$$

→ Apply control loop to minimize phase error

R&D issues

- To track noise, a second ADC evaluation board (and a second ADC channel to the FPGA) can be necessary for correlation measurements in order to distinguish between noise / drift from the BCT and noise / drift from the new components.
- Check different hardware options
  - Amplifier type
  - Filter type
  - ADC driver type
  - …

To be done now

- Measure the spectrum at the output of the RF distributor with everything (power converters, cavity RF) switched on but no beam.
- Test BCT output change versus beam position change in both directions
- Order components, make prototype, measure system behaviour

Open questions

- Threshold tracking:
  - which slope up (at injection)?
  - which slope down (operation)?
- Can losses occur in only one or a few bunches? → if yes: extra algorithm possible to increase sensitivity for this case.
- Instead of 2 concurrently running averagers (adjustable between 1 and 1024 turns): 6 fixed averagers over 1, 4, 16, 64, 256 and 1024 turns (89us, 0.36ms, 1.4ms, 5.7ms, 23ms, 91ms)? Or 3 fixed averagers over 1, 16, 256 turns?
- How to derive thresholds from beam energy?
- → if not: Ok to offer only averaging over 1, 2, 4, 8, 16, …, 1024 turns?
- Use 40MHz bunch clock from BST or 400MHz from RF system (less jitter)?
- Necessary or useful to compare turn subdivisions (if single bunch losses are possible)?
- Should we use the Turn clock?
- Useful to synchronize averaging to beam dump gap (to gain speed)?

Decisions

- System should be designed to work with bunch charges up to 1.7*10^{11} p (nominal: 1.1*10^{11} p).
- We first go for a prototype with a resolution of at least 10^{-3} at full charge and then decide if we can/want to improve it.
- Name of system: “BCM”

End

Thank you for listening!

Supplementary transparencies

Some LHC parameters

RF frequency	400.789 MHz
Bunch frequency	40.0789 MHz
Harmonic number	35 640
Revolution frequency	11 246 Hz
Total theoretical bunch places	3 564
Total bunches filled	2 808
Nominal / max. bunch charge	$1.1*10^{11}$ / $1.7*10^{11}$
Nominal / max. total charge (2 808 bunches)	$3*10^{14}$ / $4.8*10^{14}$
Pilot bunch charge	$5*10^{9}$

ADC noise

Effective number of bits:
ENOB = (SINAD[dB] – 1.76) / 6.02

Transition noise (grounded input):
$LSBs = 2^{ADC\_bits} / 10^{SNR/20} / \sqrt{8}$

Quantization noise of ideal ADC:
$1 / \sqrt{12}$ LSBs = 0.29 LSBs

To be more precise:
SNR is the sum of real noise and quantization noise

Dynamic range:
Full ADC voltage range / noise (RMS)
$= \sqrt{8} * 10^{SNR/20}$

Aperture delay jitter:
$SNR_{JITTER} =$
$-20*\log(2\pi * f_{in} * t_{jitter})$
→ 72.0 dB for 40MHz and 1ps

Output amplitude of bandpass for narrow input pulses

For a sequence of narrow pulses with frequency *f*,
a bandpass with 0 dB passband attenuation
and center frequency *f* outputs a sine wave
with following amplitude:

$$\boxed{U_{pk} = 2 \cdot f \cdot \int_{InputPulse} U(t) \cdot dt}$$

Example:

Pulse shape: Amplitude=1V, Trise=0.5ns, Ton=0.5ns, Tfall=0.5ns
→ Integral U(t)*dt = 1nVs

Pulse frequency = Bandpass center frequency = 40 MHz

→ Output amplitude = 80mV (=160mVpp)

Hardware decisions

2nd Filter 40MHz:

- Input impedance compensated Bandpass?
- uncompensated Chebychev Lowpass?

Amplifier:

- Operational amplifier (e.g. LMH6703 or OPA687)? → Low S12
- Microwave Gain Block (e.g. GALI-74+ or GALI-51+ or ERA-5XSM+? → Low Noise

Additional High Gain Channel (Gain * 4 ?)

- useful for operation where all bunches are < 25% nominal
- Useful for single bunches

ADC array:

- Possibly improve SNR by using 4 ADCs (6 dB) → extra R&D, large PCB, critical design

Shielding

- Shielding of the filters, the preamplifier, the ADC?

50R-Input-Resistor:

- Which type of 50R Resistor at input? 0.25W at full machine and good RF properties! →1W type?

What else?