LHC BLM SYSTEM:
POSSIBLE MODIFICATION SCHEMES TO KEEP OR TO FORCE TRUE THE BEAM PERMIT SIGNAL AT INJECTION

(AKA: LHCBLM SUNGLASSES)

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Current Design

In order to provide a failsafe design, among others, the following rules have been used:

- No mode or function can force the beam permit to true.
- The complete acquisition and processing chain does not have any other mode than the operational.
- Signal can be added but not subtracted.

Prerequisites for any modification

- Minimum impact on SIL and avoid branching
- Keep testability and traceability
- As few as possible changes in the system

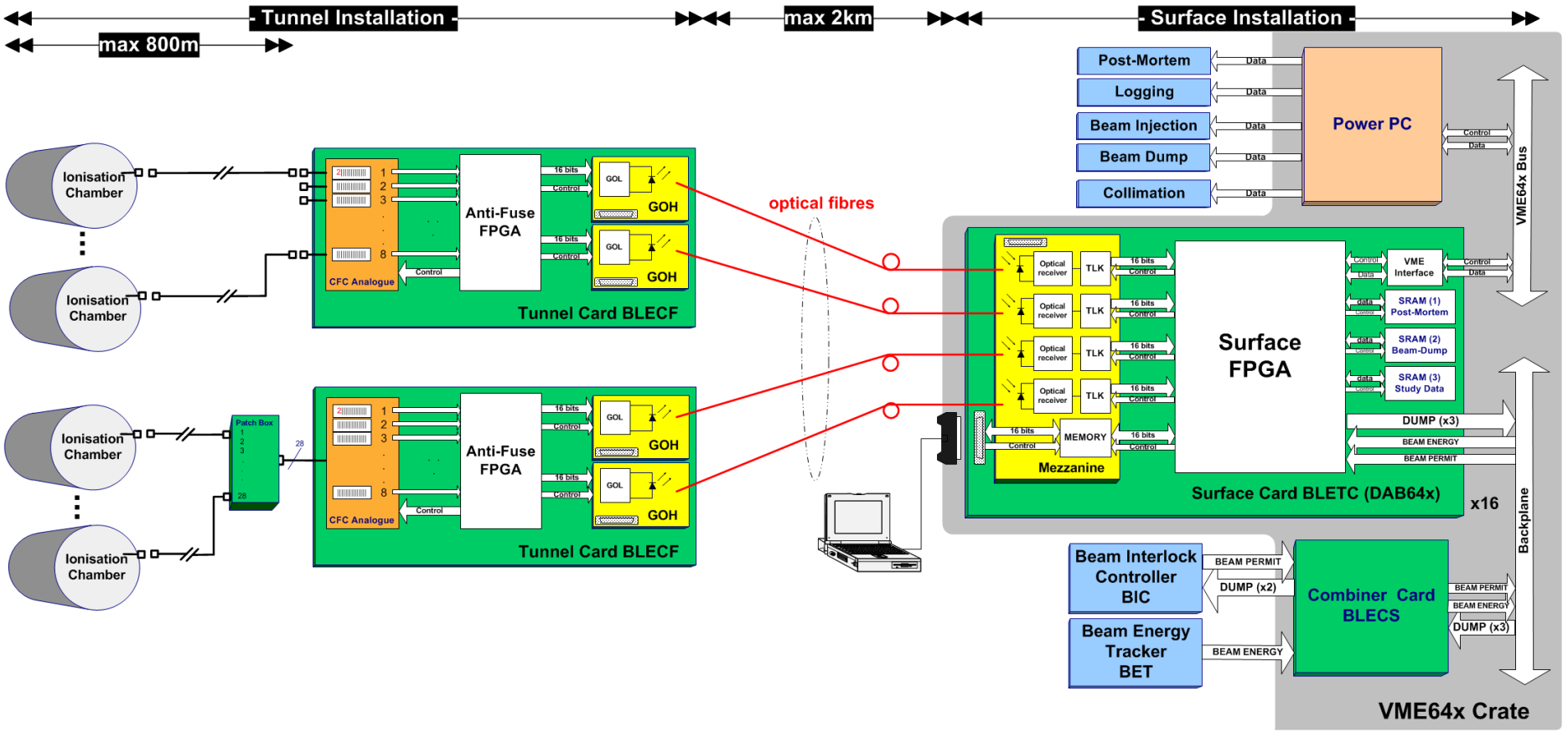
Therefore:

- Connectivity check (part of the System Sanity checks) should be still possible.
- FPGA Firmware modifications should be applicable globally – maintain one firmware for all crates.
- Expect notification signal to be of high dependability.

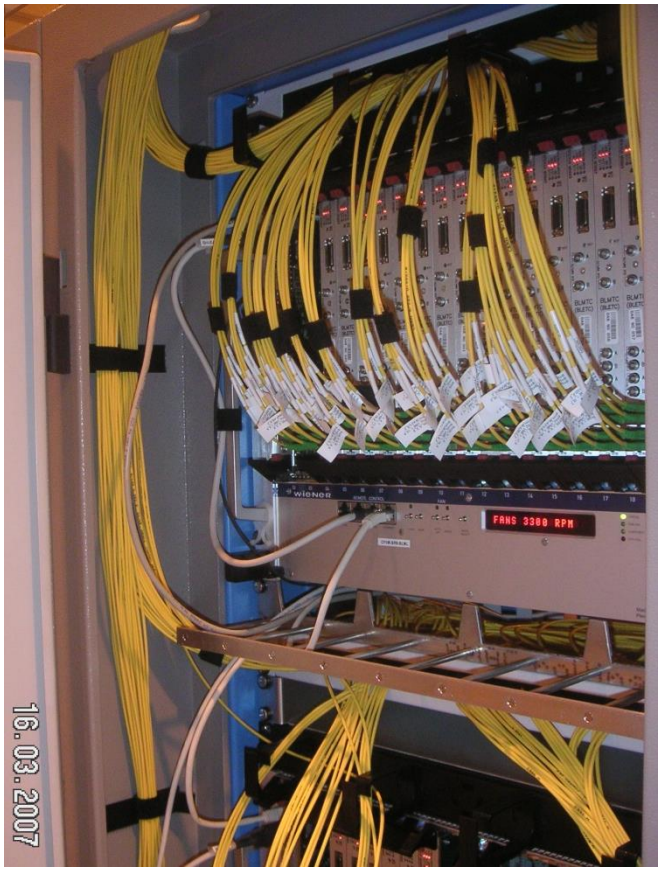
Some reminders to ease the discussion on the possible modifications

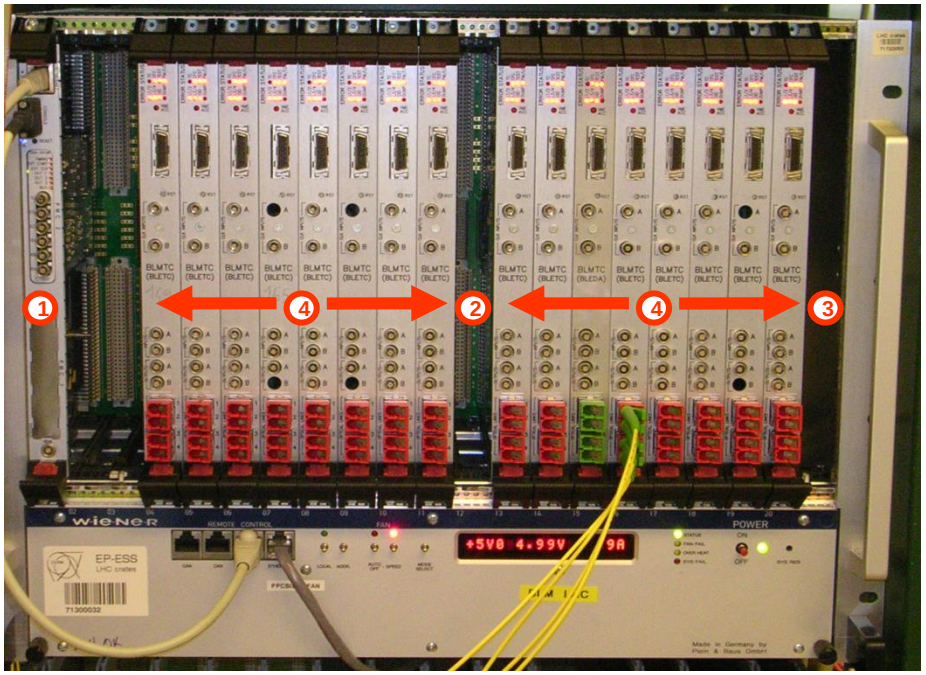
CURRENT ARCHITECTURE

System Overview



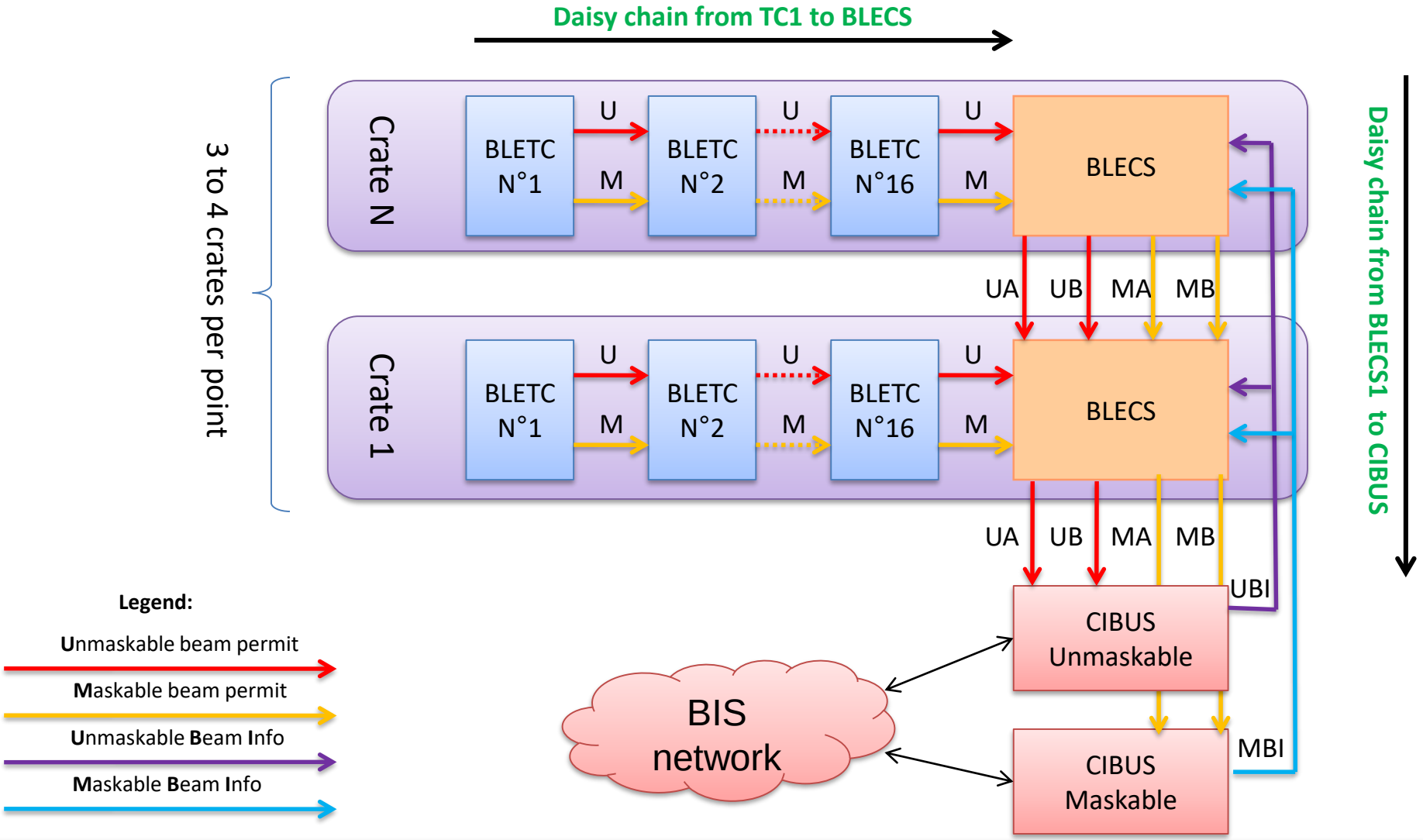
Processing Crates





1) **FEC/CTRP** – CPU / GMT timing
2) **BOBR** – BST timing
3) **BLECS** - Combiner & Survey
4) **BLETC** – Threshold Comparator

Beam Permit Signals Combination



MODIFICATION PROPOSALS

Overview of Proposals

1. Use LIC detectors and appropriate Threshold values where necessary

2. Use LIC detectors and modification in CS firmware

3. Move relevant monitors to separate crates and modify the CS firmware

4. Modify both TC and CS firmware; control logic with a new monitor flag

* Schemes 2-4 require external signal to notify for incoming injection

Scheme 1: Use of LIC detectors

- Replace the monitors getting the additional particle shower with LIC detectors
- Set ‘relaxed’ thresholds for the 450 GeV energy level on the replaced monitors.

Plus: no modification of the hardware

Minus: at 450 GeV, constantly higher thresholds

Scheme 2: Special Energy Level

- Replace the monitors getting the additional particle shower with LIC detectors
- Set ‘relaxed’ thresholds for the first energy level on the replaced monitors.
  - NOTE: currently 1st energy level is practically unused
- Modify Combiner card (BLECS) to receive inj. trigger and send to the BLETCs the energy level ‘0’ for a fixed time period after the injection.

Plus: no modification of the beam permit lines

Minus: energy monitoring by SIS will need a modification

Note: Energy Levels

This table is implemented in the BLECS FPGA.

It converts the energy received to 32 levels for the BLETCs.

```
-- Energy ranges definition :
  constant level_0 : natural :=  2047; --  1 * 65536/32 - 1 -> (x 120 Mev) =      0 to   245.64 Gev
  constant level_1 : natural :=  4095; --  2 * 65536/32 - 1 -> (x 120 Mev) = 245.64 to   491.40 Gev
  constant level_2 : natural :=  6143; --  3 * 65536/32 - 1 -> (x 120 Mev) = 491.40 to   737.16 Gev
  constant level_3 : natural :=  8191; --  4 * 65536/32 - 1 -> (x 120 Mev) = 737.16 to   982.92 Gev
  constant level_4 : natural := 10239; --  5 * 65536/32 - 1 -> (x 120 Mev) = 982.92 to 1,228.68 Gev
                                                          …
  constant level_31: natural := 65535; -- 32 * 65536/32 - 1 -> (x 120 Mev) = 7.61844 to  7.8642 Tev
```

http://www.cern.ch/blm/Acquisition_system/Energy_Conversion.htm

Scheme 3: Separate Crates

- Move relevant monitors to separate proc. Crates
  - Connect with the standard daisy chain rest of the crates
  - Note: current grouping of monitors **cannot** be broken.
- Modify the BLECS firmware to force the Beam Permit line for a fixed period of time when it receives the injection signal.

Plus: separation;

Minus:

- adding a new possible failure mode in the firmware
- more monitors than those needed will be moved
- Cost ~ 60K CHF (i.e. 2 crates populated with modules)

Scheme 4: Additional Monitor Flag

- Add a new flag per monitor in the LSA settings
  - Similar to current flags, e.g. IsConnectedtoBIS, IsMaskable, …
- Modify BLETC firmware
  - Append control logic with the new monitor flag

  e.g. IF flag is set AND inj. signal present THEN force true
- Modify BLECS firmware
  - Forward the inj. signal to the TC cards using the backplane

Plus: more fine and easier manipulation of monitor list

Minus:

- Adding a new flag requires changes in DB, Applications, settings generations and drive, MCS check, FESA, etc..
- TC FPGA has already high resource utilisation

Summarising

- Schemes 1 and 2: [the preferred choices]
  - The ideal choices from the safety point of view
  - Uncertainty if the LIC will give the needed margin
- Scheme 3: [our second choice]
  - Reasonable in complexity and additional workload
  - Some safety concerns
  - More monitors will be excluded from the machine protection than those necessary
- Scheme 4: [no-go at this point in time]
  - More inline to previous design choices
  - Uncertainty if it will fit/compile nicely in FPGA

THANK YOU