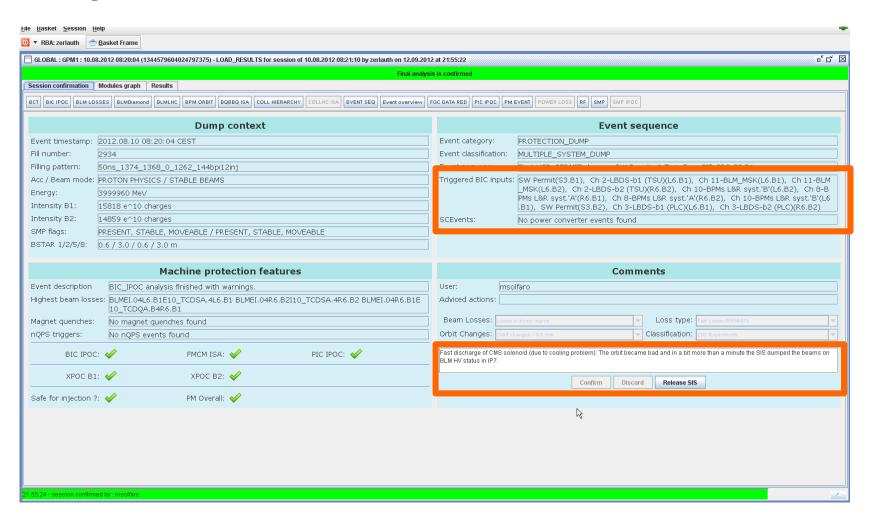


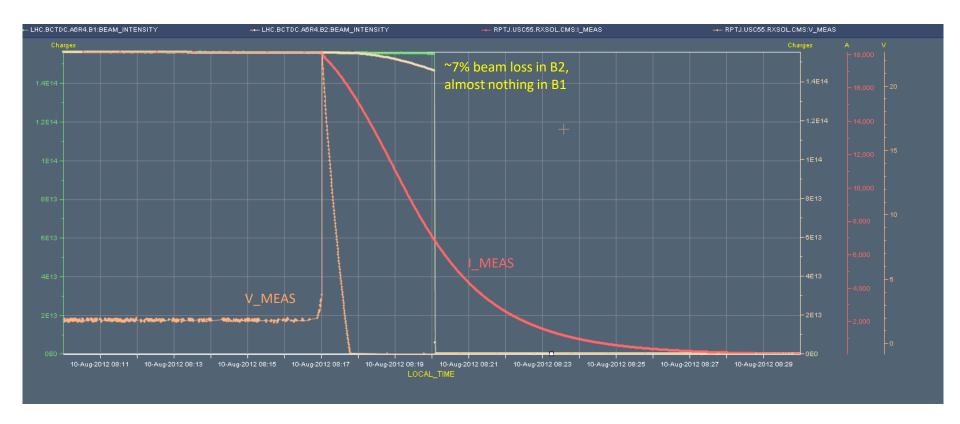
Beam dump on 10.08.2012

 LHC beams dumped on 10.08.2012 @ 08:20:04 by SIS, following a failing BLM HV check in IR7



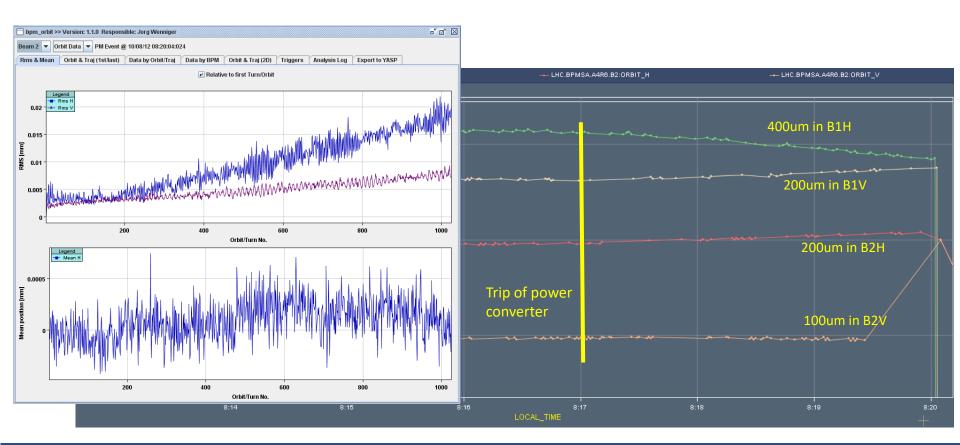
Event Sequence 10.08.2012

- Solenoid magnet actually trips 3 minutes prior to the beam dump (@ 08:17) due to cooling problem
- Solenoid current at time of dump already < 40% of I Nom



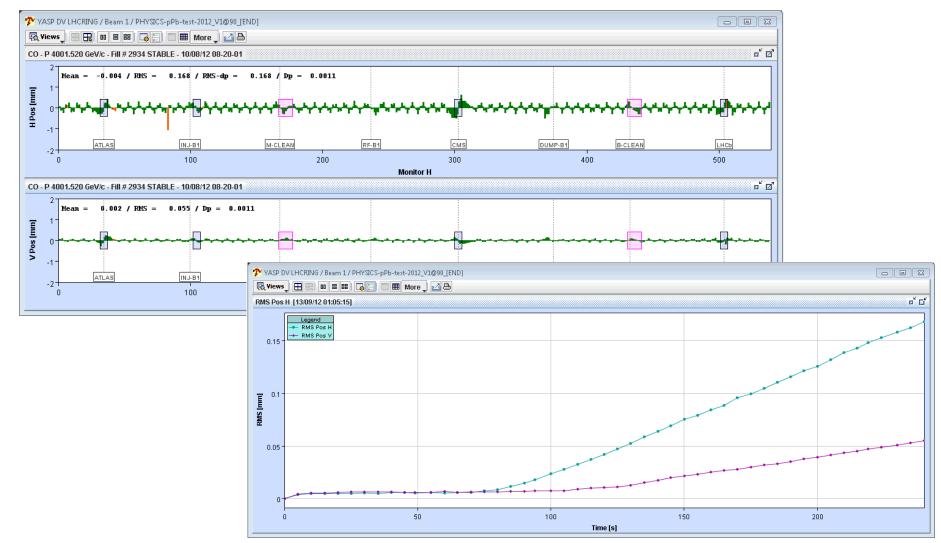
Orbit changes

- PM recordings did not show big orbit deviations (last ~25 seconds only), while LHC Logging shows orbit changes up to 400um (last 3 minutes) Note: Measured at interlocked BPMs
- OFB not active in Stable Beams!



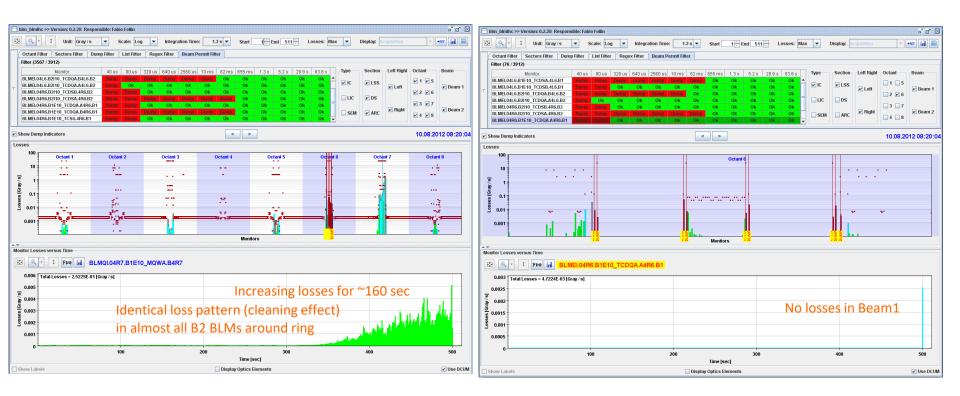
Orbit changes from YASP

rms change is ~ 150um in H, a factor of 2 below SIS limit



Beam Losses

- Clearly visible increase of beam losses in almost all B2 BLMs as of ~
 160 sec prior to the dump
- Despite bigger change of orbit almost no losses in B1

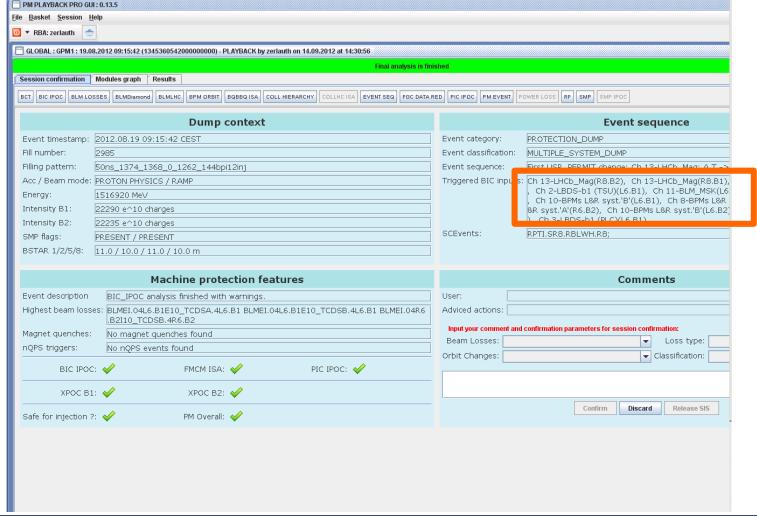


Follow-up

- Solenoid has a slow but non-negligible effect on the beams
- Very slow and distributed losses, not (yet) reaching BLM thresholds (set around 200kW), dump on known limitation of BLM HV (via SIS)
- Solenoid current at time of dump ~ 40% of I_nom
- Agreement with CMS: Provisions will be taken to provide an interlock in case of a Fast Discharge (new design of MSS already ongoing
- In parallel looking for > LS1 into slow OFB in Physics (needed for levelling) and SIS interlocking

Beam dump on 19.08.2012

• LHC beams dumped on 19.08.2012 @ 09:15 by LHCb magnet trip, interlock took some 25 ms to be generated....

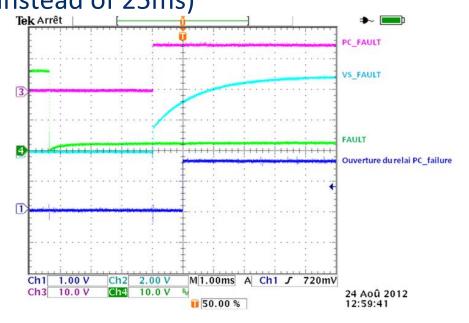


Follow-up

- Discussion with Hugues and Sylvain Ravat:
- MSS (Magnet Safety System) re-design ongoing (see previous discussion for CMS) – same MSS is used for all experiments
- Re-design based on NI Rio FPGA card already ongoing, replacing (obsolete) fuse programmable FPGA

 Will investigate to improve input filtering at output relay contact to bring down MSS transit time to 5 ms (instead of 25ms)



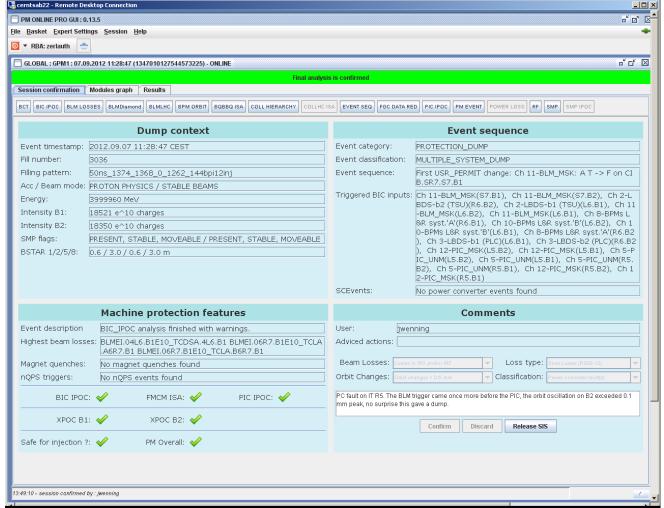




Beam dump @ 11:28:47



■ Beams were dumped while in STABLE_BEAMS at 11:28:47 on 7th of September due to Beam Losses in IR7



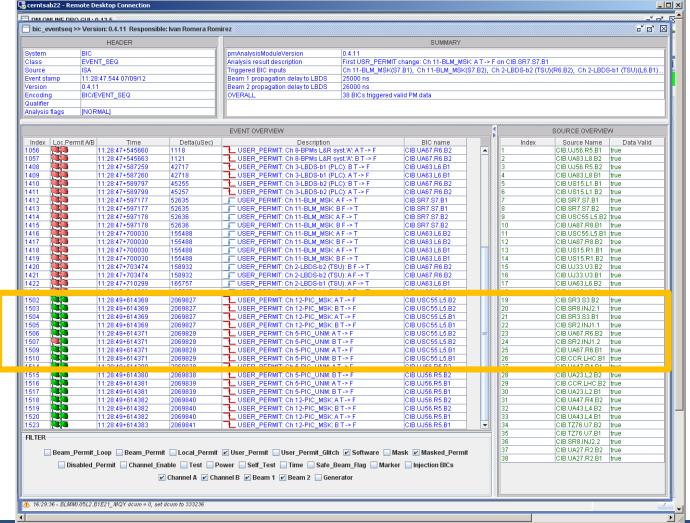
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Beam dump @ 11:28:47



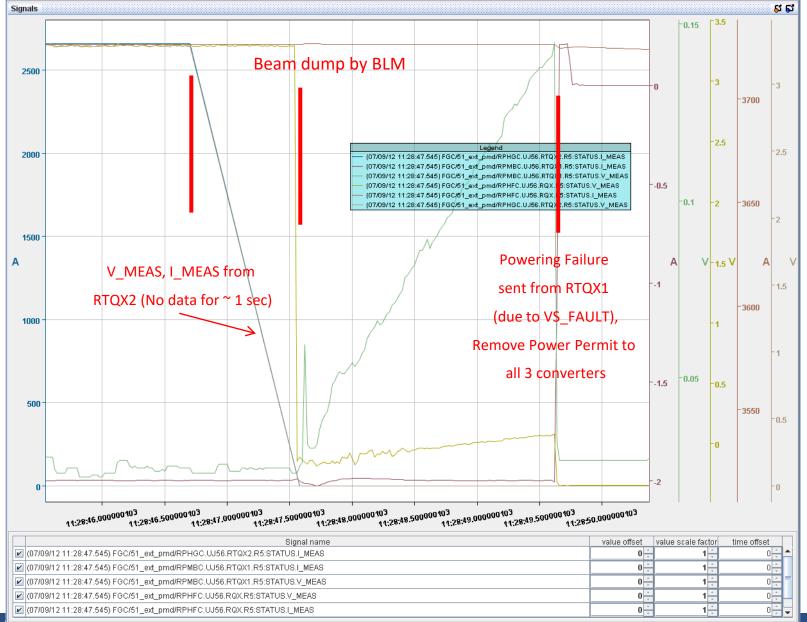
□ Actual cause was converter trip of RQX.R5, which however was reported to the interlock systems only 2.06s later!





Converter logs







Feedback from Q.King



- •This event seems to definitely be a radiation related latch-up, given that it was finally cleared by a power cycle.
- •The reason that the PIC wasn't informed about the failure relates to the design choice to keep the converter running for up to about 2s in the event of an FGC crash. This was included in the design to theoretically allow the FGC to reset and then to recover control of the converter. However, as you know, we never tried to implement this feature and now we see that both the last two events were SELs which require a power cycle anyway. So we were wise not to bother.
- •As a result, this 2s timeout before the CPLD switches off the converter and sends the PWR_FAILURE signal to the PIC is a feature that adds no value and in this case caused a problem.
- •In conclusion, I would recommend that during LS1, as part of an upgrade to the FGC2 CPLD programming, this 2s watchdog be overridden.

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